Design of High Gain Two stage Op-Amp using 90nm Technology

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Abstract - ***The present System on Chip (SOC) applications requires integration of both analog and digital components to meet the non functional constraints. The design of analog circuits can be done with the help of basic analog components like switched capacitors, Analog to Digital converters, filters etc. All these circuit components are targeted for performance metric parameters like area, speed, noise, power, gain etc. The design of less noise, high gain analog components can be designed by using fully differential circuit concepts with the help of Operational Amplifiers (Op-Amps). The Op-Amp can be designed by providing the amplification of input voltages at two stages to meet the design features. The two stage Op-Amp features can be improved by providing the concepts like compensation techniques, folded cascade etc.***

The Op-Amp design for high speed applications requires proper selection of biasing, logic style, and compensation techniques as the technology is scaling down. This paper deals with the design of basic two stage Op-Amps using 180nm for functional verification and gain calculations. This basic Op-Amp performance metrics can be improved by adding the compensation techniques. The Op-Amps are designed for both with compensation and compensation with gain improvement using Cadence full custom design suite for 90nm technology.

Index Terms—Op-Amp, Two stage, Compensation.

I. INTRODUCTION

The present day System On Chip (SOC) applications requires integration of both analog and digital components to meet the non functional constraints. The proper design of analog and digital circuits can be achieved with the help of best selected topology. The digital circuit components can be selected from gates, flip flops, inverters and amplifiers etc. Analog circuit design requires a good understanding of how the system and circuit is working. And the digital circuitry works with two distinct states, many parameters are under consideration for analog circuits which work with continuous values. Some of the analog components are switched capacitors, Analog to Digital converters, filters etc [3].

All these circuit components are targeted for performance metric parameters like area, speed, noise, power, gain etc. The design of less noise, high gain analog components can be designed by using fully differential circuit concepts with the help of Operational Amplifiers (Op-Amps).

The Operational Amplifiers (Op amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. Nowadays, Complementary Metal-Oxide Semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to meet the same constraints. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon.

The basic two stage Op-Amp can be designed by using MOS technology to meet the features and constraints. The basic Op-Amp features are gain, gain bandwidth, settling time, slew rate, Common Mode Input Range (ICMR), Common-Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR), output-voltage swing, output resistance, offset, noise etc. The open loop gain of CMOS based Op-Amp for a particular technology cannot match with the bipolar based Op-Amps. This is due to small transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes.

As a result, gain boosting schemes must be used to improve the gain. These gain enhancing methods often require more complicated circuit structures and higher power supply voltage, and may produce a limited output voltage swing. Hence multiple stage amplifiers may be used for higher gain analog circuit designs. But the multistage amplifiers generally are difficult to compensate. Many compensation schemes for multistage amplifiers are available where some of these are similar to those used in general feedback control systems which are adapted to use with electronic amplifiers. These methods include lead-lag networks, pole splitting and nested Miller compensation as well as signal level variable components. However, most compensation methods require more circuit area and more complex design than the dominant pole approach used in the

classic op amp architecture. Special problems of integrated circuit amplifiers which include lack of large sized capacitors, parasitic coupling, and package parasitic and on/off chip load problems make the compensation more difficult than discrete component amplifiers.

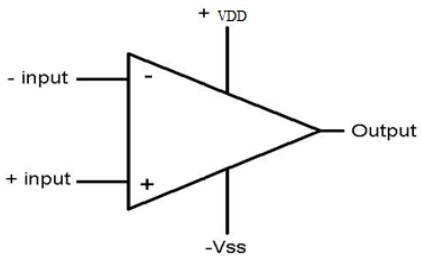
The main aim of this work is to design two stage op-amp with compensation techniques to improve the gain using 90nm technology and cadence full custom design suite.

This paper is organized such that the section II gives general background and information of Op-Amp basic theory. The section III describes the design specifications, requirements and design methodology. The chapter IV gives the details of full custom design of op amp using Cadence tools and also describes the simulation results to demonstrate the functional verification and performance improvements. The conclusion is presented in section V followed by references.

II. BASIC THEORY OF OP-AMP

The Op Amp (Operational Amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function. The gain produced by the op amp is higher than the gain produced by normal amplifiers. Thus it is a high gain amplifier. The basic symbol of Op-Amp is shown in Figure 1. The op amp symbol has two input terminals, one is positive terminal and other is negative terminal, voltage supplies to op amp as +VDD , –VSS and one output terminal.

Figure 1: Symbol of Op-amp



The basic block diagram of op-amp is shown in Figure 2.

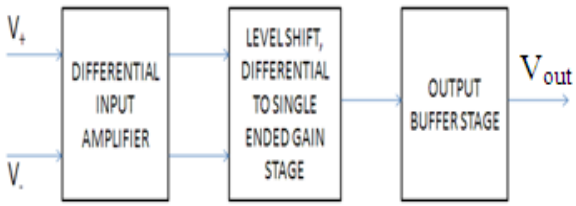


Figure 2: Block diagram of op-amp

The op-amps can be designed by using either two stage topology or folded cascode topology by modifying the stage-1.stage-2 or at any portion of the basic op-amp topology. The selection of the topology is based on the required non functional parameters and features of op-amp. The basic two stage opamp design is shown in Figure 3[6].

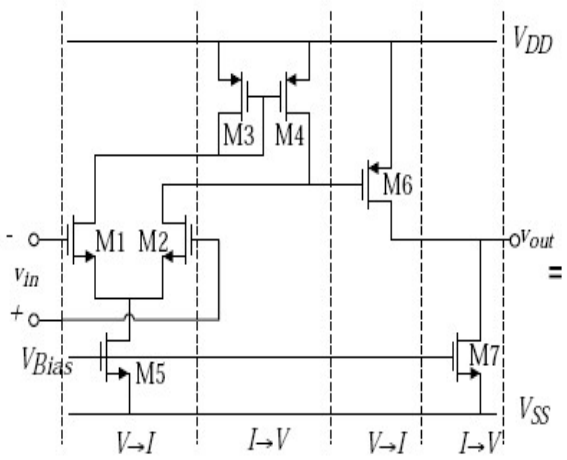


Figure 3:Basic two stage op-amp design

In Figure 3 the conversion of input signal V-I and again back to I-V is shown through different stages. The M1 and M2 transistors are used to accept the differential inputs. The M3 and M4 provides current mirror circuit. The biasing voltage is applied to the M5 transistor .

The basic op-amp design is unstable at higher frequencies. The stability of the op-amp can be improved by adding different compensation techniques with the help of capacitors at different stages or parts of the op-amp design [6]. There are various compensation techniques like miller capacitor compensation, self compensating, feed forward compensation and nulling resistor techniques etc.

III. DESIGN OF OP-AMP

The design of op-amp IC chip can be done by using the following steps [4, 6].
Step-1: Selection of the transistor logic style or logic family.
Step-2: Basic structure for the op-amp from the selected logic family.
Step-3: Selection of dc currents and transistor sizes.
Step-4: Physical verification and Chip fabrication.

The basic op-amp topology of Figure -3 can be modified by using the transistor selection according to the non functional parameters and features of the op-amp [6] as shown in Figure-4.

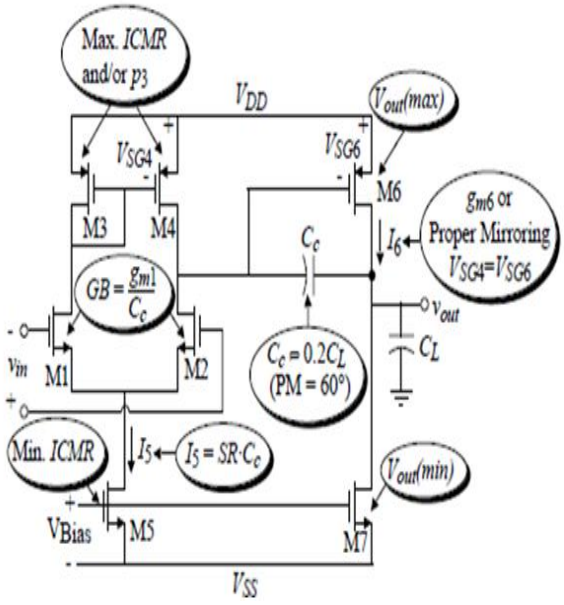


Figure 4: Transistors selection according to specifications

The input is a differential one for the current source, Transistors M5 and M7 are biasing transistors that ensure the circuit to operate always in saturation region.

The $V_{out\ (max)}$ and the gain can be increased by adding extra parallel transistors to M6 transistors. The design of compensated and compensated op-amp using gain improvement circuits are shown in Figure 5 [1, 6] and Figure 6. [2]

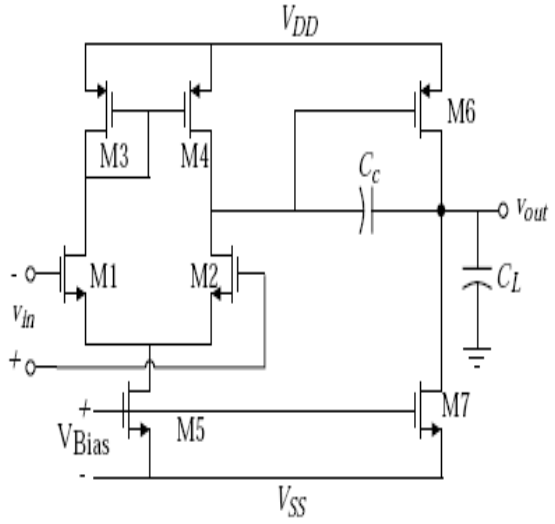


Figure 5: Basic compensated op-amp circuit

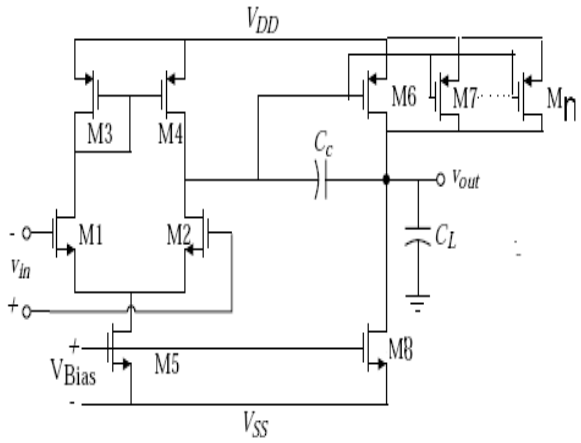


Figure 6: High gain compensated op-amp circuit

The M1, M2, M3 and M4 transistors provides the differential input pair circuitry and the capacitor Cc is used as compensation capacitor. The parallel combination of M6, M7 ……Mn transistors of Figure 6 is used to improve the gain performance parameter of opamp.

IV. FULL CUSTOM DESIGN OF OP-AMP

The two stage op amp circuits are designed by using the full custom design flow with the help of Cadence Design suite. The step wise Cadence tools for each design step are shown in Table 1.The targeted technologies are also mentioned.

Table1: Cadence tool mapping for Full custom design flow

Design Action	**Tool Name**
Schematic entry	Virtuoso schematic editor
Symbol creation	Virtuoso Symbol editor
Simulation	Analog Design Environment tool
Layout, DRC	Assura
Layout Vs Schematic	LVS tool
Post layout verification	GDSII or OA
Targeted Technology	180nm/90nm

The full custom design of basic two stage op-amp using Cadence tools and 180nm [5] is shown in Figure 7. This design is used for op-amp functional verification and the simulation result is shown in Figure 8.

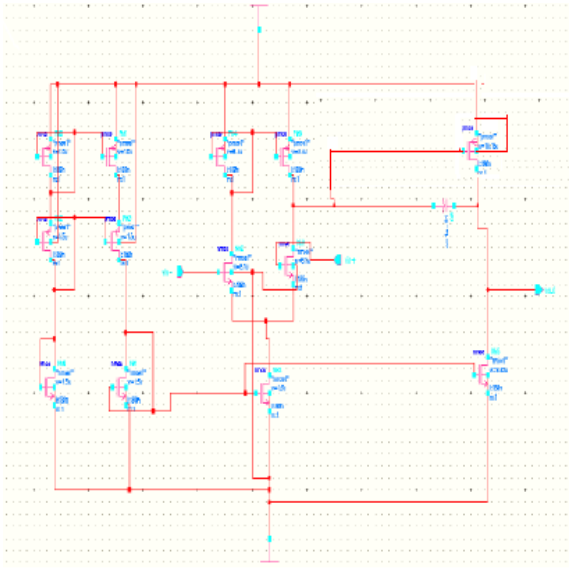


Figure 7: Two stage op-amp schematic in180nm

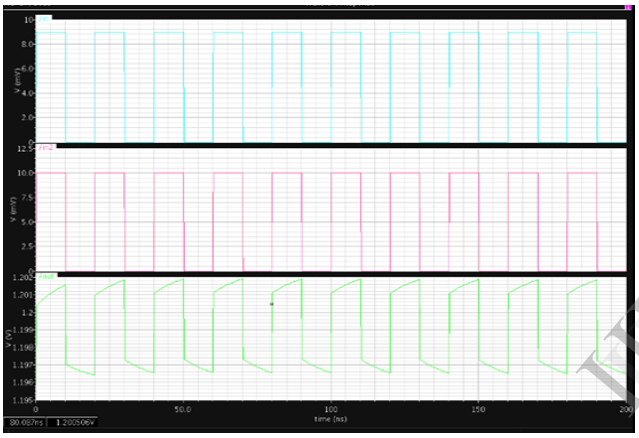


Figure 8: Simulated results for basic two stage opamp

The full custom design of basic op-amp with miller compensation using Cadence tools and 90nm technology is shown in Figure 9.The gain plot for this design is shown in Figure 10.

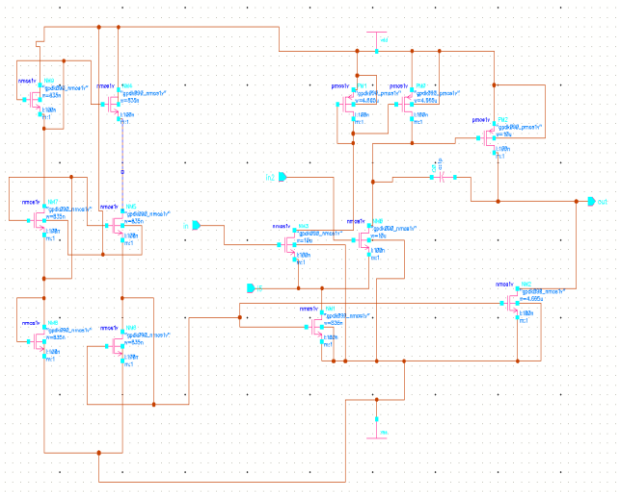


Figure 9: Two stage op-amp schematic in 90nm

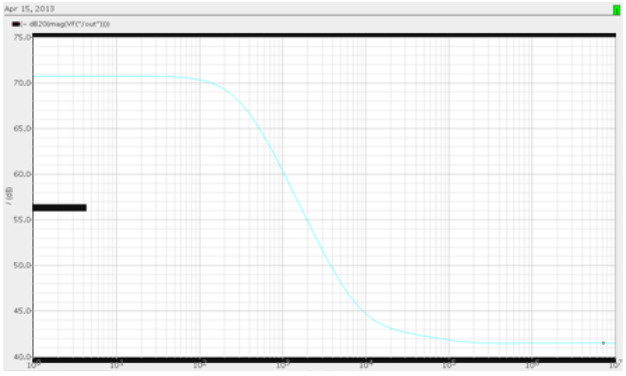


Figure 10: Gain Plot for basic two stage Op-amp

The Gain improvement in opamp design can be done by providing parallel transistors between Vdd and output lines [2]. The full custom design of op-amp with miller compensation and gain improvement circuit using Cadence tools and 90nm technology is shown in Figure 11.The gain plot for this design is shown in Figure 12.

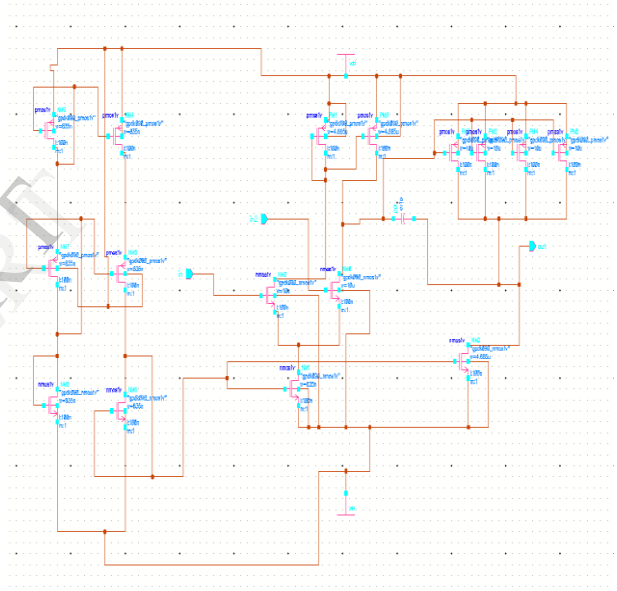


Figure 11: Two stage op-amp schematic in 90nm using gain improvement circuitry

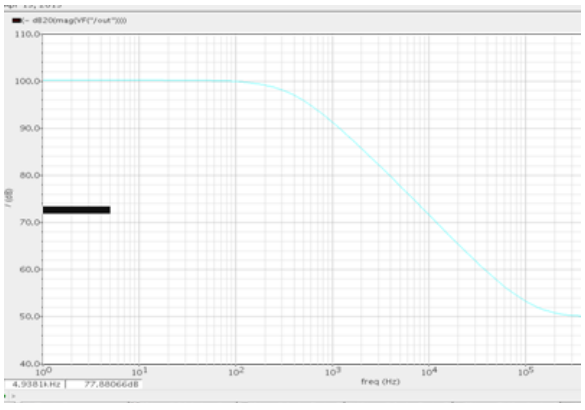


Figure 12: Gain Plot for two stage Op-amp including gain improvement circuitry

The gain comparison for both two stage compensated op-amp (Figure 9) and compensated op-amp with gain improvement circuitry (Figure 11) are shown in Table 2.

Table 2: Gain Results comparison

Parameters	Basic Compensated Op-amp	Op-amp with Gain improvement
Gain	72dB	100dB

V CONCLUSIONS

The Operational Amplifier (Op-Amp) is designed and analyzed by using Cadence ICFB full custom design suite using 90nm technology. The basic two stage op-amp is designed by using 180nm technology for functional verification.

The two stage op amp circuit is designed for simple compensated features using 90nm technology with L=100nm and achieved a gain of 72 db. This simple op-amp design can be improved in performance by adding gain improvement circuitry. This two stage compensated op amp is designed with 90nm technology and achieved a gain of 100db.

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