# Design of Higher Level Back-to-Back Stacked Multicell Converter with DMPG Control Technique to Improve the Power Quality 

Vijaya raju Vasipalli, PG scholar<br>Dept. of Electrical Engineering SATI, Vidisha, Madhya Pradesh, India

Ashok Kumar Patel,<br>PG scholar<br>Dept. of Electrical Engineering<br>SATI, Vidisha, Madhya Pradesh, India

Praveen Pateriya,<br>PG scholar<br>Dept. of Electrical Engineering<br>SATI, Vidisha, Madhya Pradesh, India


#### Abstract

This paper proposes the new Back-to-Back Stacked Multicell Converter with DMPG control technique. In this paper we designed 4-cell 17-Level BTB-SMC and 8-cell 49-Level BTB-SMC. Both converters are control by DMPG control technique only. Both converters are compared in their design and power quality. Whenever the number of output voltage levels are increase then the harmonics will decrease so that power quality is good. This paper also explains DMPG technique, which is very suitable technique to generate control pulses for any circuit. Circuits are designed in MATLAB/SIMULINK software.


Keywords-Back-to-Back Stacked Multicell Converter (BTBSMC), Degree Modulated Pulse Generation (DMPG).

## I. INTRODUCTION

In recent years the multilevel concept is widely using in high power high/medium voltage applications because when the levels of output waveform is increase then the harmonic content in the output waveform will decrease so the power quality will increase.

There are so many concepts on multilevel but flying capacitor Multicell (FCM) converter and stacked Multicell (SM) converters are advanced technologies for multilevel generation [1]. FCM converter can convert DC/AC or DC/DC [2].SM converter is more efficient than Hybrid FCM converter [3]. The word "Back-to-Back" is defined that two semiconductor switches are connected in back to back position.

## II. MULTICELL CONCEPT

One DC source and two semiconductor switches formed as one cell. Two semiconductor switches connected back to back with DC source.

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Fig.1. Block Diagram of SMC
As we seen in the Fig. 1 the circuit which is connected with Number of Cells is called as Multicell converter.

There are two types of cells in the SMC circuit one is P-cell another one is N -cell. The combinations of these cells are called as Multicell. Derivative of FCM converter is SM converter. To increase the output voltage levels we uses $m \times n$ cells array [1].

## III. THE PROPOSED CONVERTER

As shown in the bellow Fig. two SM converters are connected back to back each other in proposed BTB-SM converter. Both converters are separated with two switches $\mathrm{T}_{1}$ \& $\mathrm{T}_{2}[1]$

With the help of $\mathrm{T}_{1} \& \mathrm{~T}_{2}$ we can produce positive and negative half cycles respectively.
Number of cells and output voltage levels are calculated by:

$$
\begin{gather*}
\mathrm{N}_{\text {cell }}=2(\mathrm{n}+\mathrm{m}) \ldots \ldots . .  \tag{1}\\
\mathrm{N}_{\text {Level }}=2[(2 \mathrm{n}+1)(2 \mathrm{~m}+1)]-1 . \tag{2}
\end{gather*}
$$

The voltage values for proposed converter are calculated by:

$$
\begin{equation*}
E_{a}=[2 n(2 m+1) /((2 n+1)(2 m+1)-1)] \times E \tag{3}
\end{equation*}
$$

$$
\begin{equation*}
\mathrm{E}_{\mathrm{b}}=\mathrm{E}-\mathrm{E}_{\mathrm{a}} . \tag{4}
\end{equation*}
$$

Where " $E$ " is maximum output voltage.


Fig.2. 2( $n+m$ ) cell proposed converter block diagram


Fig.3. SIMULINK diagram of 4-cell, 17-Level converter


Fig.4. SIMULINK diagram of 8-cell, 49-Level converter

## A. Proposed 4-cell, 17-Level Converter

As shown in the Fig. BTB-SMC consists of two converters connected "back to back" with the help of two switches $\mathrm{T}_{1} \&$ $\mathrm{T}_{2}$. The SMC, which is right side to the $\mathrm{T}_{1} \& \mathrm{~T}_{2}$, consists of " $n$ " cells and The SMC, which is left side to the $T_{1} \& T_{2}$, consists of " $m$ " cells. Each cell in the both SMC's has two sub-cells one is P -cell and another one is N -cell. In each converter Number of P-cells is equal to number of N-cells.so right side converter has 2 n -cells and left side converter has 2 m -cells.

In 4-cell converter $\mathrm{n}=1$ and $\mathrm{m}=1$ so the number of cells and levels are calculated by:

$$
\begin{gather*}
\mathrm{N}_{\text {Cell }}=2(\mathrm{n}+\mathrm{m})=4 \text {-cell...... (5) } \\
\mathrm{N}_{\text {Level }}=2[(2 \mathrm{n}+1)(2 \mathrm{~m}+1)]-1=17 \text {-Level.... (6) } \tag{6}
\end{gather*}
$$

## B. Proposed 8-cell, 49-Level Converter

As explained in the above portion 49-Level converter has 8cells this is calculated from equations $1 \& 2$. In this converter $\mathrm{n}=2$ and $\mathrm{m}=2$. When the number of cells are increasing then the number of output voltage levels are increase. The converter which is for any Level has four voltage sources. When number of output voltage levels are increasing then the flying capacitors and switches will increase.

## IV. CONTROL TOPOLOGIES

A. DMPG Technique for 17-Level Converter

## B. DMPG Technique for 49-Level Converter

TABLE II. SWITCHING STATES FOR 49-LEVEL SMC


Calculate degree modulation or sector selection by using Equations 7 \& 8. With the comparison of ramp signal and degree modulated generated signal the control signal will generate. We will give this control signal to the multiport switch to select the suitable sector.


Fig.8. Control signal for the multiport switch

stla


521


sill

-


521


s12


Fig.9a. Switching pulses for 17-Level Converter


Fig.9b. Switching pulses for 49-Level Converter
V. SIMULATION RESULTS

## A. Proposed 4-cell, 17-Level Converter




Fig.10. Output Voltage and Current of 17-Level Converter without Filter


Fig.11a. FFT window of Output Voltage



Fig.12. Output Voltage and Current of 17-Level Converter with Filter



Fig.13. FFT window of Output Voltage and Current

## B. Proposed 8-cell, 49-Level Converter




Fig.14. Output Voltage and Current of 49-Level Converter without Filter

Fig.11b. FFT window of Output Current


Fig.15. FFT window of Output Voltage and Current without Filter


Fig.16. Output Voltage and Current of 49-Level Converter with Filter


Fig.17. FFT window of Output Voltage and Current with Filter

## V. COMPARISION OF 17 AND 49- LEVEL CONVERTERS

TABLE III. 17 Vs 49- LEVEL COMPARISION

| System Parameters | 17-Level | 49-Level |
| :---: | :---: | :---: |
| No. of switches | 4(back to back) | $8($ back to back) |
| ${\mathrm{E}, \mathrm{E}_{\mathrm{a}} \& \mathrm{E}_{\mathrm{b}}}^{200,150 \& 50 \mathrm{~V}}$ | $600,500 \& 100 \mathrm{~V}$ |  |
| DC Voltage sources | 4 | 4 |
| Flying Capacitors | 0 | 4 |
| Load Resistance | $10 \Omega$ | $10 \Omega$ |
| THD (\%) without Filter | $15.79 \%$ | $13.37 \%$ |
| Voltage Mag. at <br> fundamental freq. | 166 V | 490.7 V |
| Current Mag. at <br> fundamental freq. | 16.6 A | 49.07 A |
| THD (\%) with Filter | $6.12 \%$ | $5.15 \%$ |
| Voltage Mag. at <br> fundamental freq. | 215.3 V | 635.4 V |
|  | 21.53 A | 63.54 A |

## VI. CONCLUSSIONS

Multi level concept is very popular in recent years because "if the number of output voltage levels are increase then the harmonics of the converter will decrease" [5]. So that there are so many multi level concepts are there but the "back to back stacked Multicell converter" is very new proposed topic to improve the power quality. As we seen in the comparison of both 17 and 49- level converters we can say that 49-Level BTB-SMC is more better than 17-Level BTB-SMC. Results are analyzed in FFT Window.

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[^0]:    First I would like to Thank my guide Prof. S.P Phulambrikar (HOD) for his great guidance and motivation.
    I would like to thank my friends Vikalp Kulshrestha \& Ankur Chourasiya for their heartful help.
    I thank to all Faculty members who helped me. Especially to Mr. Rakesh Sagar sir who did software installation for me.

    Finally I thank to my loving family members who always supported me, encouraged me, and motivated me.

