Design of Low Power, High Speed ADC by using Submicron Technology

Ms. Kiran P. Kokate[1], Prof. A. O. Vyas[2]
[1]ME. student, Electronics & Telecommunication Engineering, G.H. Raisoni College of Engineering & Management,
[2]Assit. Professor, Electronics & Telecommunication Engineering, G.H. Raisoni College of Engineering & Management,
Amravati, (M.S.)
India.

***Abstract*— In modern era, VLSI design is one of the paradigms to have high speed, less power consumption, effective use of space, easily available productivity and mobility. Low power high speeds ADC can be design using VLSI.ADCs are key design blocks in modern microelectronic digital communication systems. With the fast advancement of CMOS technology, more & more signal processing functions are implemented in the digital domain for low cost, low power consumption, higher yield, & higher reconfigurability. Various example of ADC application can be found in data acquisition systems, measurement systems, digital communication systems also imaging, instrumentation systems. So, the proposed work is to design ADC in 90nm CMOS process.**

The proposed work is to design and implement a successive approximation register (SAR) analog to digital converter (ADC) for communication domain. Sample and Hold circuit, Comparator are the basic building blocks of SAR ADC. The efficient design of Sample and Hold circuit and Comparator is drawn by using DSCH 3.5 software. Then, CMOS layout and simulation is drawn by using Microwind 3.1 software.

I. INTRODUCTION

An Analog-to-Digital Converter (ADC) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

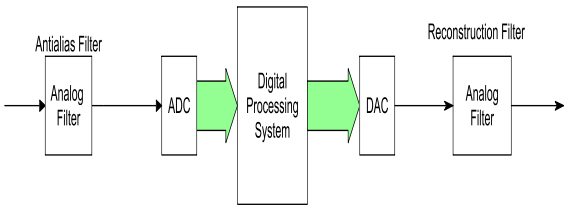

Fig.1.1: Analog to Digital Converter

The electronic filter placed before an ADC is called antialias filter. It is used to remove the frequency components above one half of the sampling rate that would alias during the sampling. The electronic filter placed after a DAC is called reconstruction filter. It also eliminates the frequency above the Nyquist rate.

In this, a brief overview of SAR ADC is provided to be effectively used in communication domain. Basically the objective of this project is to design the high speed ADC and which consume low power. So, the proposed work is to design such type of ADC.i.e.SAR ADC with high speed and low power consumption.

II. LITERATURE SURVEY

In [1] A 10-bit SAR ADC for biomedical application was presented. The proposed SAR ADC achieves rail-to-rail input range and low power consumption. A Digital-to-Analog Converter (DAC) using C-2C capacitor array and dynamic comparator was used for low power consumption. It was realized in 0.18um standard CMOS technology. In [2] the design and implementation of 4-bit time interleaved SAR ADC for UWB application. Major contribution was that they use two capacitive DAC instead of three capacitive DACs. They implemented the ADC in 0.18μm CMOS technology and had total power consumption of 23.3mw.In [3] SAR ADC implemented in a conventional 0.18um CMOS technology with low voltage. The SAR composite of sample-and-hold dummy switch compensation was employed, comparator is low voltage latched and realized based on current-mode approach, control logic circuit and digital to analog conversion consists of binary weighted capacitor arrays for differential inputs. In [5] A 10-bit dual-channel pipelined flash-successive approximation register (SAR) analog-to-digital converter (ADC) for high speed application was presented. The prototype ADC fabricated in a 45-nm CMOS process occupies 0.16 mm^2.

III. SYSTEM ARCHITECTURE

A. SAR ADC

In SAR ADC, it sets MSB. Then convert MSB to the corresponding analog output by using DAC. Then guess output will compare with the input. If Vin >1/2 ADC then it set the bit otherwise test the next bit. SAR ADC is capable of high speed and high resolution. They have low power consumption and low cost. They have medium accuracy and

good tradeoff between speed & cost. They have no pipeline delay.

Basically, the successive-approximation A/D converter consists of three main components an analog comparator, a DAC, and a successive-approximation register (SAR) all of which are connected in a feedback arrangement shown in Fig.3.1.

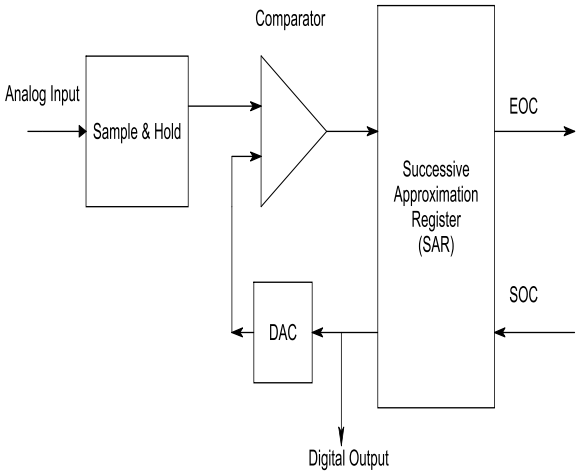

Fig.3.1: SAR ADC

B. *Sample and Hold Circuit*

In general, Sample and hold circuit (SHC) contains a switch and a capacitor. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value when the sampling signal turns to low in the hold mode.

Sample and hold circuit (SHC) mainly used in ADC. It samples analog input signal & holds value between clock cycles. Stable input is required in many ADC topologies, which is provided by sample and hold circuit. it reduces ADC-error caused by internal ADC delay variations. Sometimes, it referred as Track and Hold (T/H) .The important parameters of S/H circuit are: hold step, signal isolation in hold mode, input signal tracking speed in sample mode, droop rate in hold mode, aperture jitter. The basic schematic of sample and hold circuit is as shown in fig.6.8.

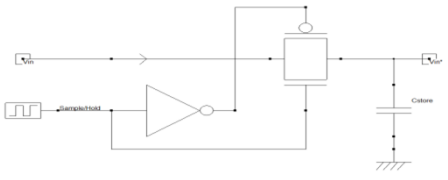

Fig.3.2: Sample and Hold Circuit

CMOS Layout of Sample and Hold Circuit

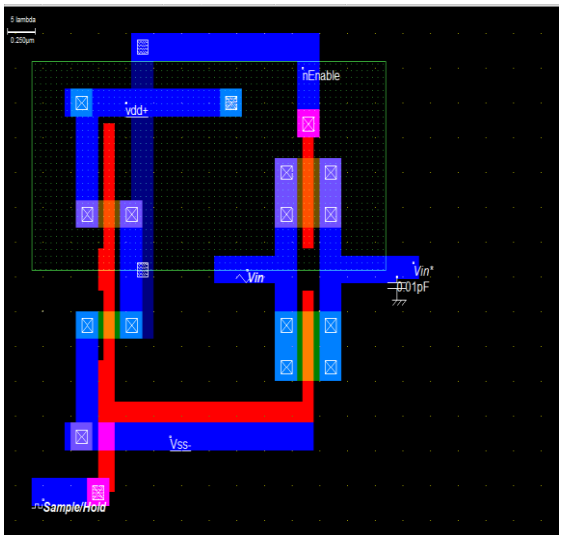

Fig.3.3: CMOS layout of Sample and Hold Circuit

C. *Comparator*

Comparator is the only analog block of a SAR ADC and performs the actual conversion. It compares the analog sampled input to the analog output of the DAC and generates digital output of '0' or '1' which will be used in the SAR logic. Accuracy and speed of the comparator are two important factors. The requirements of the comparator are speed and accuracy.

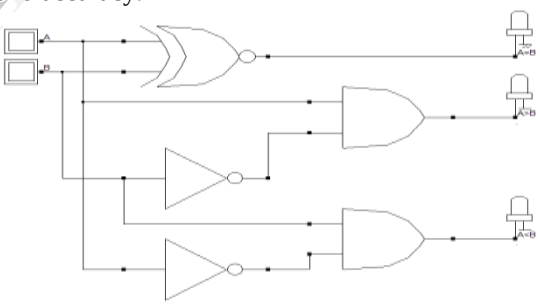

Fig.3.4: Basic schematic of Comparator

The basic Gates of comparator are

1. EX-OR with 6 transistor

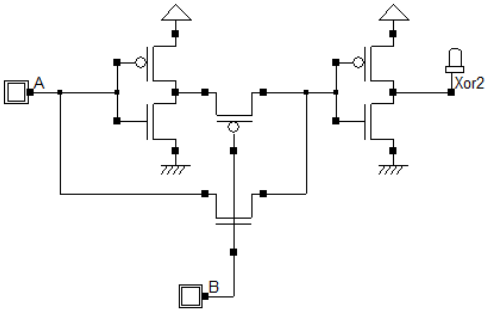

Fig.3.5: Basic schematic of EX-OR with 6 transistors

2. AND Gate

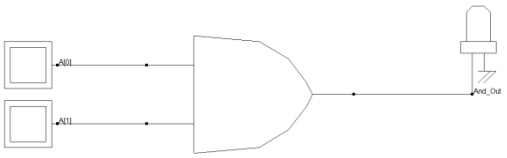

Fig.3.6: Basic AND Gate

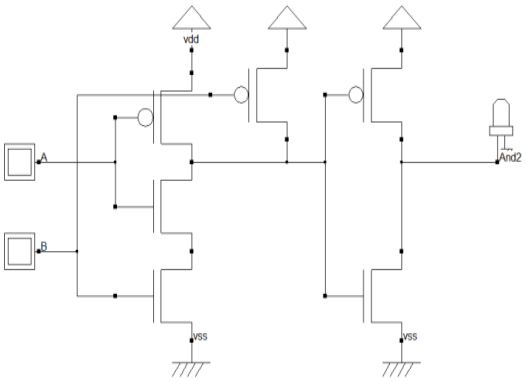

Fig.3.7: Basic schematic of AND Gate

CMOS layout of Comparator

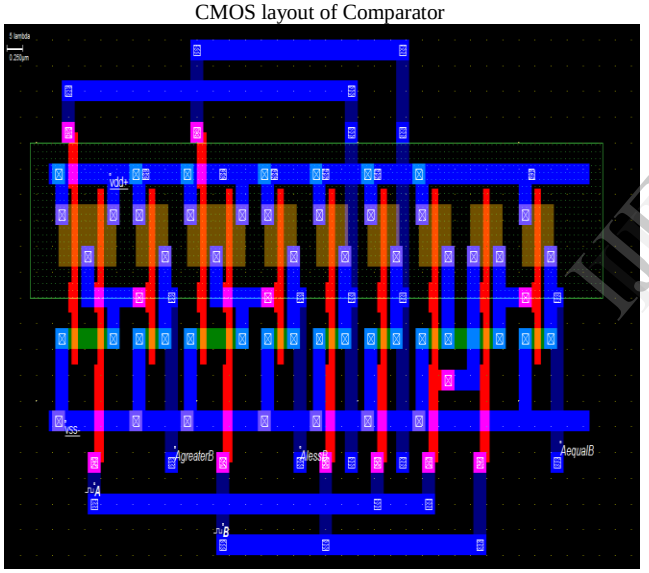

Fig.3.8: CMOS layout of Comparator

IV. FLOW CHART

The proposed work is to design SAR ADC by using CMOS technology. First of all the basic schematic is drawn by using DSCH 3.5 software. And it is verified by using this software. Then CMOS layout is drawn based on basic schematic design by using Microwind 3.1 software. And then verification is done for various parameters.

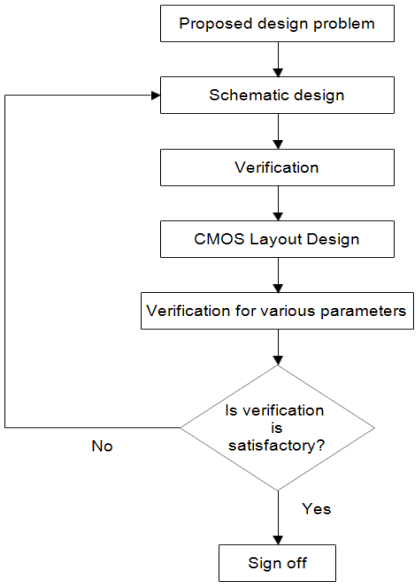

Fig.4.1: Proposed Model Flow

V. SIMULATION RESULT

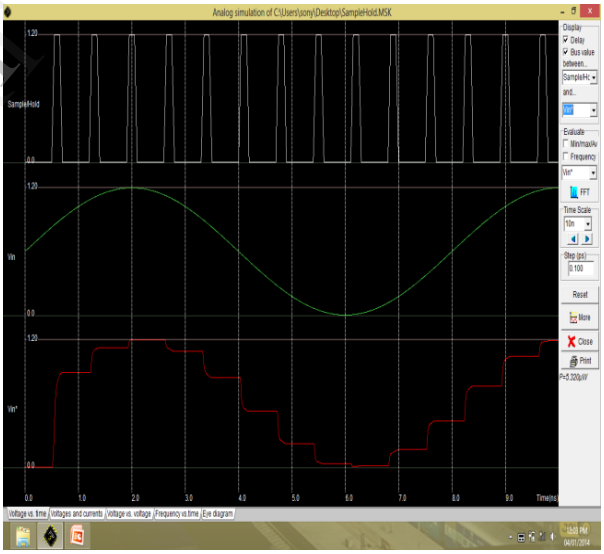

Fig.5.1: Simulation result for Sample and Hold circuit

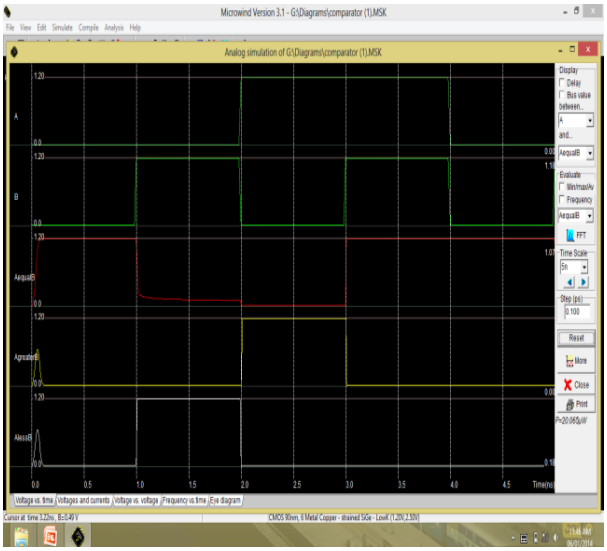

Fig.5.2: Simulation result for Comparator

VI. CONCLUSION

In this paper, we proposed the basic schematic and simulation result of Sample and Hold circuit and Comparator which are useful for the further processing of SAR ADC.

REFERENCES

[1] Hoonki kim, Youngjae min, Yonghwan kim and soowon kim "A low power consumption 10-bit rail-to-rail SAR ADC using a C-2C capacitor array" IEEE transaction 2008.

[2] Sanjay Talekar and S.Ramasamy "A low power 700 MSPS 4-bit Time Interleaved SAR ADC in 0.18um cmos" IEEE transaction 2009.

[3] Hur A. Hussam, Izhal abdul Halin "Design of 8-bit SAR ADC CMOS" Proceedings of 2009 IEEE Student Conference on research and development 16-19 Nov 2009, UPM Serdang, Malaysia.

[4] Saleh Abdel Hafeez "A new high-speed SAR ADC architecture." 2010 Xith international workshop on symbolic and numerical methods, modeling and application to circuit design.

[5] Young-deuk jeon, Jae–won Nam, Kwi-Dong Kim, Tae moon Roh, Jong-Kee Kwan "A Dual channel pipelined ADC with sub-ADC based on flash SAR architecture," IEEE transaction on circuits and systems-II:express brief, vol.59, no.11, November 2012.

[6] Ying-zu-lin, chung-cheng liu, Gaun-ying haung, ya-ting shyu, yen-ting liu, soon jyh chang "A 9-bit 150 Ms/s subrange ADC based on SAR architecure in 90-nm CMOS,"IEEE transaction on circuit and systems-I:regular papers, VOL.60, No.3, March 2013.

[7] Si-seng Wong, U-fat chio, Yan zhu, sai-weng sin, Seng-Pang U, Rui Paulo Martins "A 2.3mw 10-bit 170 MS/s two step binary search assisted time-interleaved SAR ADC," IEEE journal of solid-state circuits,vol.48, no.8, August 2013.

[8] Weibo Hu, Yen-Ting Liu, Tam Nauyen, Donald Y.C.Lie, Brian P.Ginsburg "An 8-bit single ended ultra low power SAR ADC with a novel DAC switching method and a counter based digital control circuitry," IEEE transactions on circuits and systems I: regular papers, vol 60, no.7, July 2013.

[9] Pierluigi Nuzzu, Claudio Nani, Costantino Armiento, Alberto Sangiovanni, Jan Craninckx and Geert Van der Plas "A 6-bit 50-MS/s Threshold Configuring SAR ADC in 90-nmDigital CMOS".

[10] Zhiheng Caol " A 32mw 1.25GS/s 6b 2b/step SAR ADCs for UWB applications".