Design of Low Power Novel Viterbi Decoder Using Pass Transistor Logic

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Abstract

In this paper a low power viterbi decoder based on pass transistor logic is presented. Viterbi decoder which consumes more power plays an important role in communication applications. Viterbi decoder is used to decode the received data which is encoded using convolutioncodes. In this paper in order to reduce the power consumption and to improve the performance of the decoder optimized pass transistor logic is proposed. As the multiplexer and flip flops are the major parts in the viterbi decoder circuit, pass transistor logic is used to reduce the complexity of the circuit. The proposed technique is simulated using tanner tool. The simulated result shows the speed of viterbi decoder using Pass Transistor Logic is high compared to the existing CMOS logic and the TG logic and also the number of transistors required to design the Viterbi decoder is reduced using PTL compared to both CMOS and TG logic.

Keywords: Viterbi decoder, pass transistor logic, NMOS only PTL, tanner tool

1. Introduction

Viterbidecoder is based on viterbi algorithm which was proposed by Viterbi in 1967.The algorithm is mainly used to decode the convolutioncodes in digital communication systems. The viterbi algorithm(VA) provides the most accurate way to find maximum likelihood sequence of transmitted signal. In order to transmit the analog signal through the digital communication system, the signal should be sampled and quantized before proceeding through the system. In this paper, it is assumed that the digital values are transmitted through channel. The Viterbi algorithm is used to find the signals which are corrupted by noise in the channel.

The viterbi decoder consists of three major blocks such as branch metric unit, add compare and select unit and survivor memory unit. The Viterbi algorithm is based on treills diagram and the encoder circuit is considered as a finite state machine. In order to find out the errors in the received sequence the hamming distance of that sequence is calculated. Viterbi decoders are widely used in wireless communication specifically it is widely used in third generation mobile terminals and the decoder circuit consumes more power in the transmission system

In present scenario reducing the power consumed by a device is a major factor in VLSI technology. Even though the CMOS logic design plays a major role in designing devices with low power consumption, the switching activity of the CMOS devices causes more power consumption. For low power consumption, different logic styles may be used. In this paper, the design based on pass transistor logic is proposed for low power consumption application.

2. Proposed Design

The proposed method is based on pass transistor logic[PTL]. The pass transistor is a simple NMOS or PMOS transistor which acts like a switch. In pass transistor logic, the input is applied to source terminal of the MOSFET instead of supply voltage. The input is passed to the output based on the control signal. The control signal is applied in the gate terminal.

The simple pass transistor logic using NMOS is given in the figure 1.When the control signal is at logic'1' the input is passed to the output and similarly when the control signal is at logic'0' the transistor does not conduct and makes the output as undefined state.

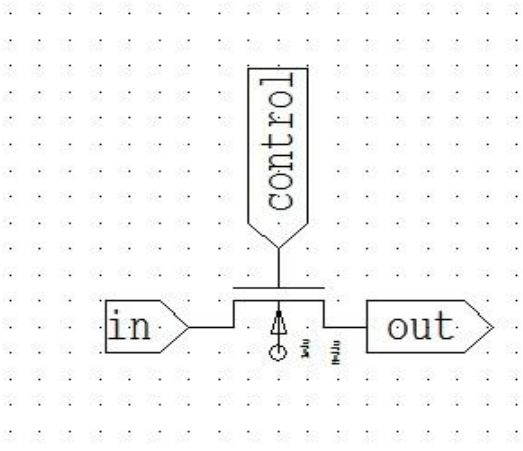

Figure1.A simple NMOS pass transistor

There are two different types of pass transistor logic design such as the NMOS only pass transistors and the combination of both NMOS and PMOS pass transistors where NMOS passes strong '0' and the PMOS passes strong '1'.The PTL requires minimum number of transistors to design a logic circuit and therefore the area required for the circuit is minimized and the speed of the circuit is increased.

3.Design of viterbi decoder using PTL

The Viterbi decoder consists of three major blocks such as Branch metric unit, Add compare and select unit and Survivor memory unit. In this chapter the blocks of viterbi decoder are explained using transmission gates.

3.1Branch Metric Unit

The Branch Metric Unit(BMU) is used to measure the Hamming Distance between the received sequences with the expected code sequence. The Hamming Distance is calculated simply by counting the number of bits at which the received sequence and the expected sequence are different.

The BMU consists of a two input EXOR gate and three bit asynchronous counter. The counter is designed using T flip-flops. The output of the EXOR gate is applied as the clock pulse to the first flip flop of the counter and output of one flip-flop is given as clock input for the next flip flop. The T input for all flip flops are tied to HIGH input. When the received sequence and the expected sequence are different then the output of the EXOR gate becomes high and the counter starts to count. The circuit diagram for BMU is given in the figure2.

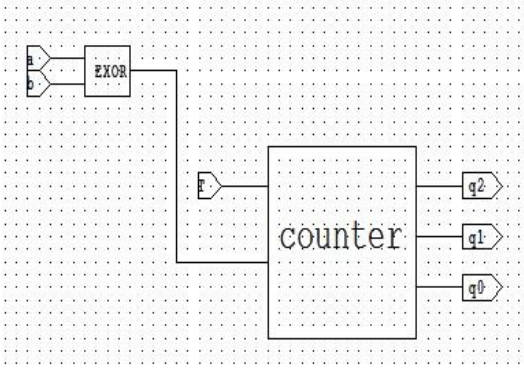

Figure 2.Block Diagram of BMU

The counter is designed by cascading T flip-flopsand the T flip-flop is designed by using D flip-flop and gates.The circuit diagram for D flip-flop using PTL is shown in figure 3.

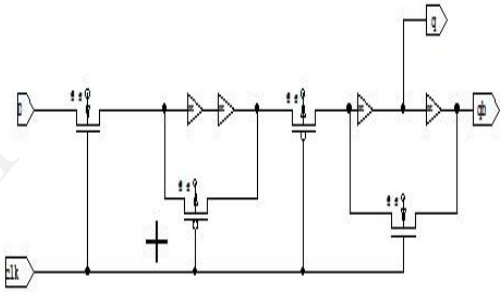

Fig 3.Circuit diagram of D flipflop using PTL

3.2 Add Compare and Select Unit

The Add Compare and Select unit (ACSU) consists of adder, comparator and selector. The adder unit adds the branch metric from the BMU with the corresponding path metric. The inputs to the adder are the output of BMU and the previous path metrics. The new resultant metrics are compared in comparator. The multiplexer is the major block in the selector. The circuit diagram for multiplexer using PTL is shown in figure4.While designing 2:1 multiplexer using PTL it requires only four transistors.

The selector selects the appropriate branch. The selector unit consists of four 2:1 multiplexers. The outputs of adder unit are given as inputs to the selector unit. The output (less than bit) of the comparator is given as selection line for the selector.

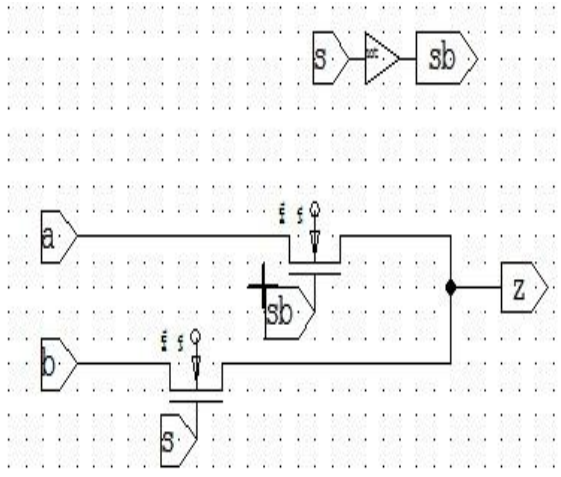

Fig 4.Circuit diagram for 2 to 1 multiplexer using PTL

3.3 Survivor memory unit

The important step in the decoding process is finding the survivor path. The output of the selector is the survivor path and that path is stored in the survivor memory unit. The survivor memory unit (SMU) is designed by cascading serial in serial out (SISO) shiftregisters. The length of the shift registers depends on the length of the encoder. The SMU unit consists of four SISO shift registers. When the positive clock pulse is applied, the data D is transferred to the output of the flip-flop and for each positive clock cycle the value stored in one register is shifted to another register.

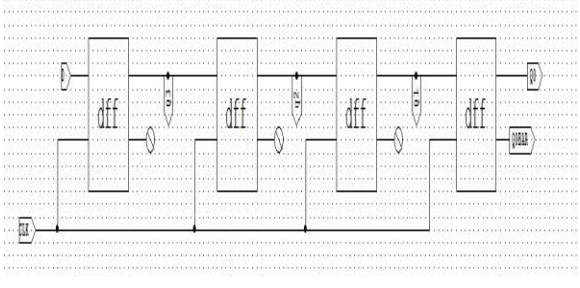

Figure 5 :Block diagram of single stage of SMU

3.4 Block diagram of viterbi decoder

The block diagram of viterbi decoder with PTL is shown in figure 6.The circuit is designed using Tanner tool. in this circuit two BMU units are used since there are two possible state changes from one state to another state. The BMU unit calculates the Branch metric. The ACSU adds the branch metric with the previous path metric using adder.

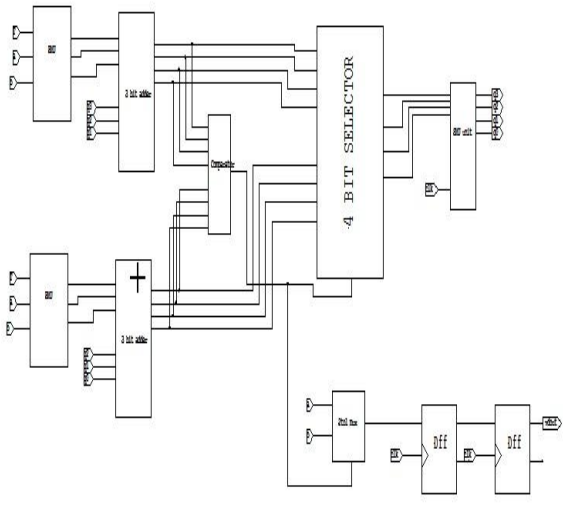

Fig 6.Block diagram of viterbi decoder

The comparator adds two paths from two adders and the selector selects the path with minimum hamming distance .The SMU stores the new path metric value and the corresponding states. The 2:1multiplexer and two bit shift registers are used to get the decoded output.

4. Results and Discussion

The viterbi decoder designed using Pass Transistor logic was simulated using Tanner tool (TSPICE). The output waveform of the viterbi decoder is shown in the figure7.When the select input is logic 1, then the 'a' input value is transferred to the output. In the BMU the clock signal for the counter is applied from the output of EXOR gate.

There are two BMUs since each state has two branches in treills. The output of the EXOR gate is the Hamming distance between the expected sequence and the received sequence that can be counted by using the counter. The output of the BMU denotes the branch metric value. In ACSU the branch metric values are added with the Path metric value and the appropriate path is selected in selector unit using the control signal from the comparator unit. The Less than(LT) output of the comparator is used as a selection line of the selector unit and the multiplexor. When the select input is logic '0', then the 'b' input value is transferred to the output.

4.1 Comparison of performance

The Viterbi decoder is designed using Pass Transistor logic in circuit level. The performance of viterbi decoder is analyzed using the simulated output in

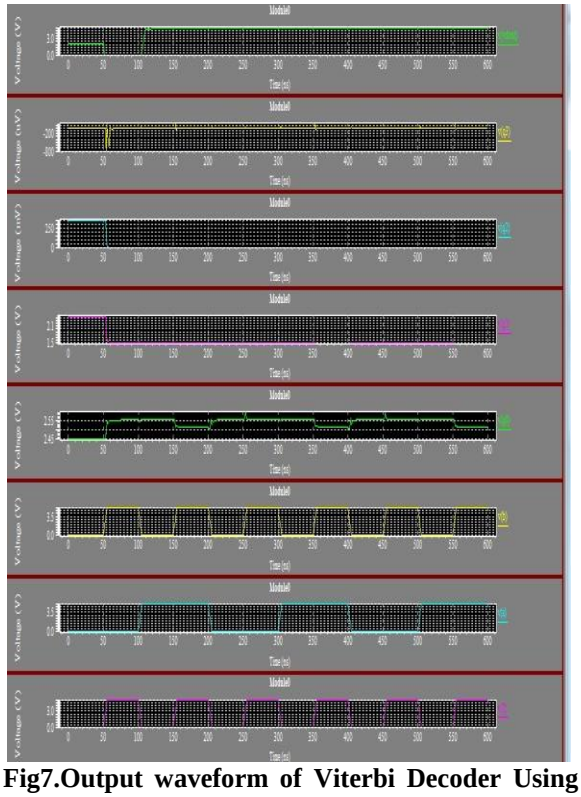

Fig7.Output waveform of Viterbi Decoder Using PTL

Tanner tool. The simulation results show that the, the number of transistors of the Viterbi decoder using PTL is reduc

ed compared to the existing CMOS logic. Hence the results prove that the proposed PTL has low power, high speed and low area. The performance comparison table for Viterbi decoder with 5V vdd is given in Table1. The performance comparison table for Viterbi decoder with 3V vdd is given in Table2.The performance comparison table for Viterbi decoder with 1.5V vdd is given in Table3.

6.Conclusion

The major blocks of Viterbi decoder are simulated by using Tanner's s-edit VLSI CAD tools and Parameters values are analyzed by using same tool. The circuits were compared with existing CMOS circuits. The circuit based on Transmission Gate gives better performance than existing circuits in term of power dissipation and Area. The proposed circuits can be used in the low power wireless communication.

S.no	Viterbi decoder	Power (mW)	Transistor count	Area μm^2	Speed (Ghz)	Delay (ns)	PDP(10^{-12} W-s)
1	CMOS	0.058	982	0.043208	5.157	193.21	11.20
2	TG	0.041	838	0.036872	13.33	74.98	3.074
3	PTL	0.35	478	0.021032	46.18	21.65	7.57

TABLE.1. VITERBI DECODER WITH Vdd = 5.0Volts

S.no	Viterbi decoder	Power (mW)	Transist or count	Area μm^2	Speed (Ghz)	Delay (ns)	PDP(10^{-12} W-s)
1	CMOS	0.95	982	0.043208	6.456	154.6	146.87
2	TG	0.71	838	0.036872	18.55	53.90	38.269
3	PTL	1.043	478	0.021032	55.27	18.09	18.86

TABLE.2. VITERBI DECODER WITH Vdd = 3.0Volt

TABLE.3. VITERBI DECODER WITH Vdd = 1.5 Volts

S.no	Viterbi decoder	Power (mW)	Transist or count	Area μm^2	Speed (Ghz)	Delay (ns)	PDP(10^{-12} W-s)
1	CMOS	5.467	982	0.043208	9.22	108.45	592.45
2	TG	3.291	838	0.036872	26.61	37.57	123.64
3	PTL	4.538	478	0.021032	15.71	63.65	288.84

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