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Design of Low Power Reduced Area Cyclic DAC

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***Abstract*— A novel circuit for cyclic Digital to Analog Converter (DAC) is discussed in the paper. The DAC process is insensitive to the offset voltages of op-amps and to parasitic capacitances. The capacitance error is minimized in this method, since only a limited number of capacitances are used. The circuit is beneficial when we go for higher input bits as it takes only a small amount of chip area and also reduces total power consumption. The DAC is designed for 0.18um CMOS technology. A modified version of cyclic DAC is done, which reduces the total number of transistors. This method is applicable to DACs with any number of input bits. Even if the number of bits is increased, the area remains constant in this method. A comparative study of cyclic DAC and R-2R ladder DAC and also modified cyclic DAC and R-2R ladder DAC is explained here and the parameters such as power and area are analyzed. Cadence tool is used for the simulation.**

Keywords — SoCs, Weighted resistor DAC, R-2R ladder DAC, Cyclic DAC, Modified cyclic DAC.

I. INTRODUCTION

One of the booming areas in integrated circuit is SoC design. SoCs becoming highly complex, have digital, analog, and mixed component to satisfy the growing demands of communication application. With technology, developing at a fast rate and increasing usage of electronic devices, there is an inevitable need for lowering the power in these devices. Developing low power technique has become the active area of research in various fields of electronics.

SoCs refer to the integration of various electronic devices of diverse functions into a single chip. SoC act as complete electronic devices which perform complex functions. SoCs consists of millions of transistors. Lowering the power consumption and reducing the area are the requirements of SoC design. The circuits which are integrated in a single chip need less area and low power consumption designs. Here cyclic digital to analog converter is discussed. Cyclic DAC is modified to satisfy the requirement for SoC design.

Digital to Analog Converter is a device used to convert binary code into an analog voltage. DAC act as an interface between the digital world and analog real life. Unlike analog signals, digital data can be transmitted, manipulated and stored without degradation. But a DAC need to convert digital data to an analog signal to drive the analog devices. So the DAC is a necessary component of the communication field.

Cyclic DAC has many benefits over other types of DACs. It requires less area than that of R-2R ladder DAC[1]. The binary weighted DAC is constructed from digital switches and set of weighted resistors connected to an operational amplifier. The opamp creates an inverting amplifier that sums input resistance through feedback loop.The switches and resistors act together as a digitally controlled resistor that can take one of the digital values of resistance.This essentially provides a digitally controlled current source. Each new binary code applied to the input produces new discrete current levels that are summed by the feedback resistor to provide analog voltage. The main disadvantage of this type of DAC is inaccuracy. As the number of bits increases it requires a large value of resistors. For 8bit DAC it requires 256R valued resistor. In the case of R-2R ladder DAC, it requires only two valued resistors such as R and 2R. But the problem with this type of DAC is, it takes a large area as the number of bits increases and also causes inaccuracy[3].

II. CYCLIC DAC

Cyclic DAC is a serial DAC. In a serial DAC, the conversion is done sequentially. One clock is required to convert one bit. The input bits are fed one at a time. For the first bit it produces an analog voltage and for the second bit the analog voltage is summed with the previous one. So for n bit DAC the final analog voltage will obtain at the n_{th} clock.

III. CONVERSION ALGORITHM

The DAC conversion is a process of transforming a binary number b into an analog voltage as given by

$$V_a = (-1)^{b_0} \sum_{i=1}^{n} 2^{-i} b_i V_r \qquad \text{-----(1)}$$

Where b_0 is the sign bit which assumes zero if b is positive or 1 if negative. And b_1 and b_n are the most significant bit and least significant bit[2].The conversion starts with b_n and the analog voltage can be obtained by iterating the following sequence.

$$V(i) = \frac{\{V(i-1) + b_{n+1-i} V_r\}}{2} \qquad \text{----(2)}$$

IV. WORKING

Cyclic DAC consists of two blocks. Control block and conversion block.

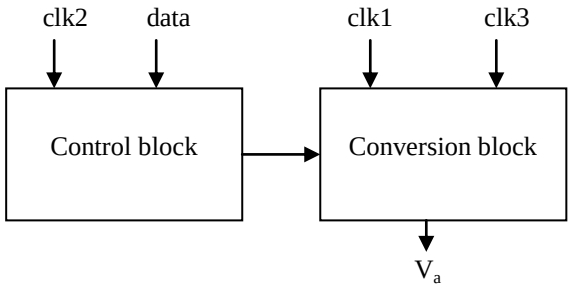

Fig.1: Block diagram of cyclic DAC

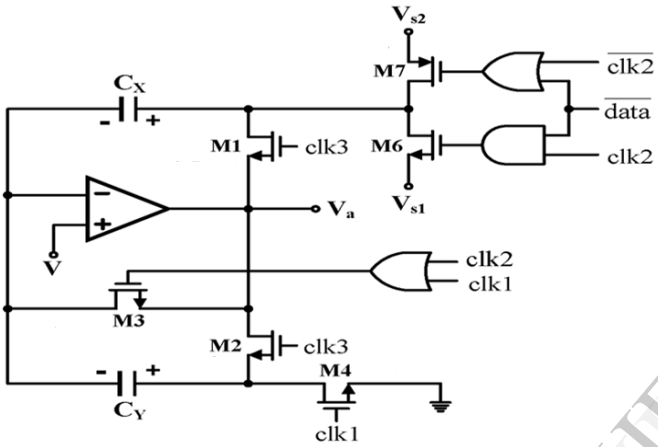

Fig.2:Circuit of cyclic DAC

It requires three clocks which are non overlapping. V is the offset voltage of opamp.Vs2 is the reference voltage and Vs1 is zero. Clock signals are shown below.

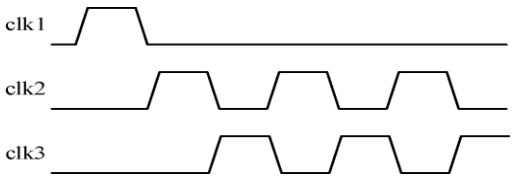

Fig.3:Clock signals

Figure 2 shows the circuit of a cyclic DAC. It consists of an opamp and two capacitors of equal value which forms a parasitic insensitive integrator and a voltage divider.When clk1 becomes high, the transistors M3 and M4 turns ON and the capacitor C_Y gets charged to V. The voltage V is also stored to C_X in clk2 phase, immediately after clk1.These capacitors practically cancel the offset voltage of the opamp.

After the clk1, clk2 becomes high and depends upon the input data bit and either M7 or M6 becomes ON. The capacitor C_X will either get charged to Vs2 or discharged to ground. If the data is high, then C_X get charged upto Vs2, otherwise gets discharged to ground.After clk2, clk3 becomes high.This makes the transistors M1 and M2 ON. Therefore the capacitors C_X and C_Y are in parallel. So division by 2 occurs and produces the analog voltage. For the second bit, the corresponding voltage will be stored on C_X and the previous analog voltage will be stored at C_Y. And the final analog voltage is obtained at the i^{th} clock.

V. MODIFIED CYCLIC DAC

The control block consists of 16 transistors which consists of logic gates. The modified control block is shown below which consist of 8 transistors. This circuit can reduce half of the number of transistors. Thereby area and power consumption is reduced. The circuit of control block is shown below.

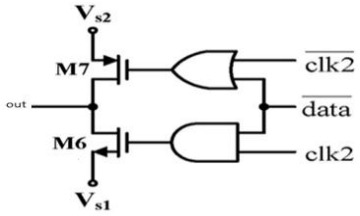

Fig.4:Control block

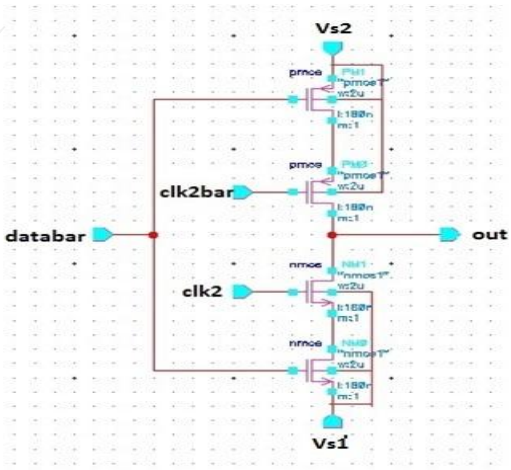

Fig.5:Modified control block

VI. SIMULATION

A. Operational amplifier

Operational amplifier is the main building block of cyclic DAC. Two stages of opamps are used. The first stage is the differential amplifier and the second stage is the common source amplifier. Schematic and the output waveforms are shown in figure 6,7,8,9.

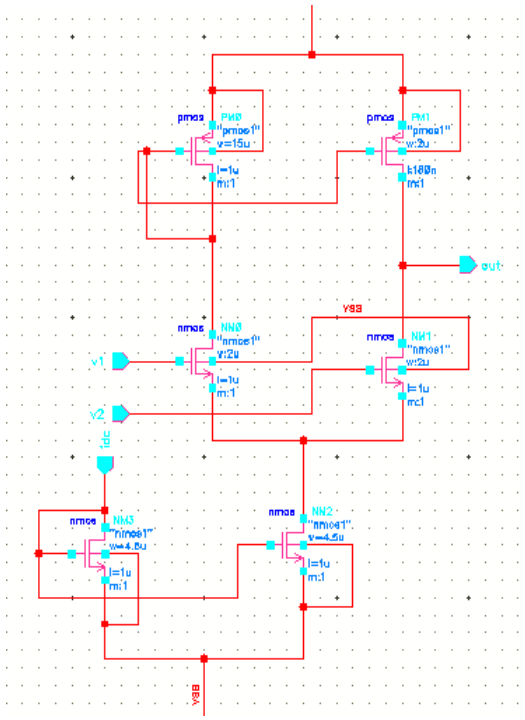

Fig.6:Differential amplifier

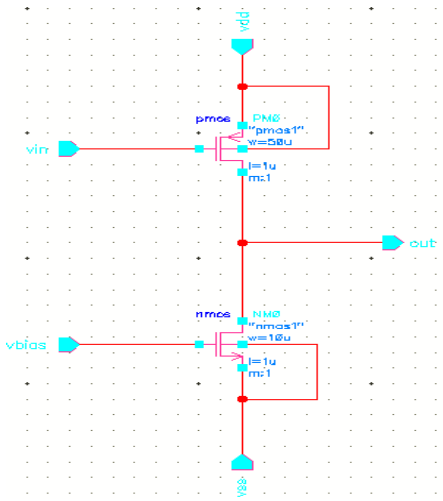

Fig.7:CS amplifier

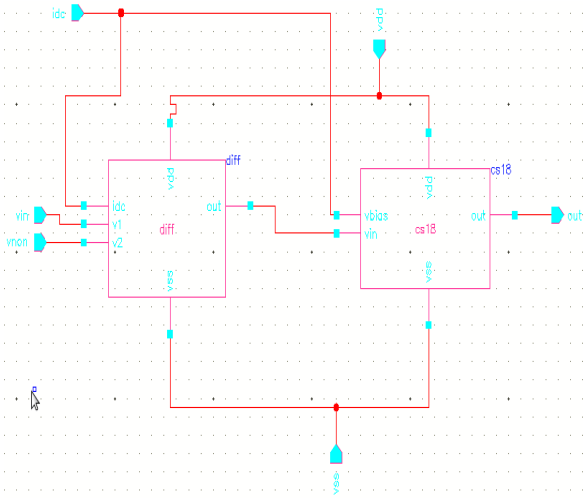

Fig.8: Operational amplifier

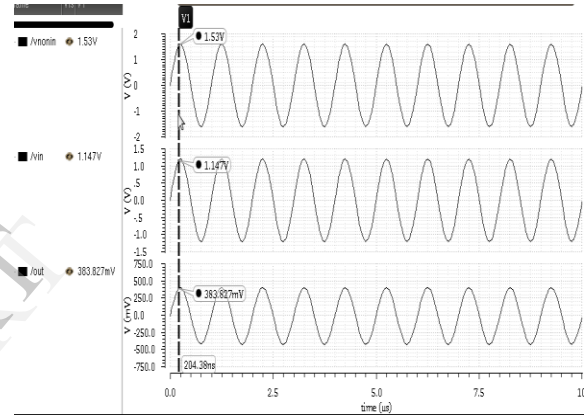

Fig.9:Output

The parameters of opamp are shown below.

TABLE I. ANALYSIS OF OPAMP

Parameter	Value
No.of transistor	8
Gain	46.8dB
Bandwidth	0.496GHz
Gain Bandwidth product	4.96GHz
Slew rate at 1MHz	345.6V/uS

B. Cyclic DAC

Output waveform of cyclic DAC is shown below. 8 bit data 11111110 is fed to the DAC and got 892mV as the analog voltage.

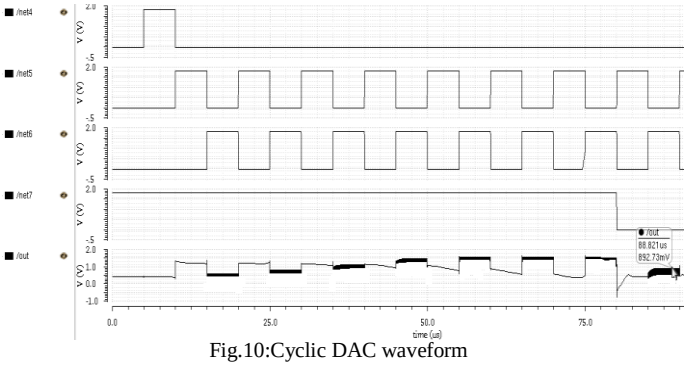

Fig.10:Cyclic DAC waveform

C. *Modified cyclic DAC*

Figure 9 shows the output of the cyclic DAC with modified control block. Input 111111 is fed to the DAC and analag voltage for this input is 1.5V.

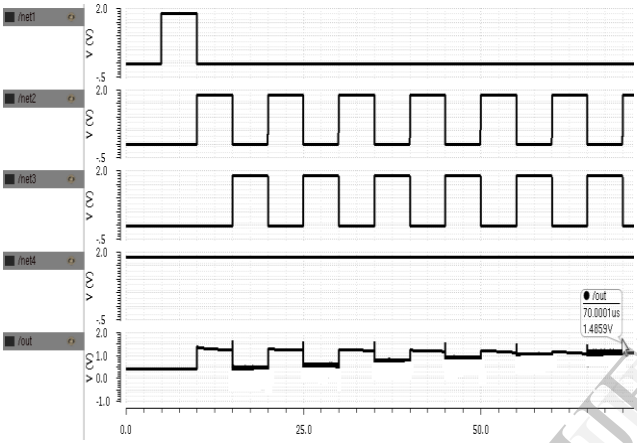

Fig.11:Modified cyclic DAC

D. *R-2R ladder DAC*

In order to compare the modified cyclic DAC and the conventional DAC, a 6 bit R-2R ladder DAC is implemented.The schematic and the output is shown below.

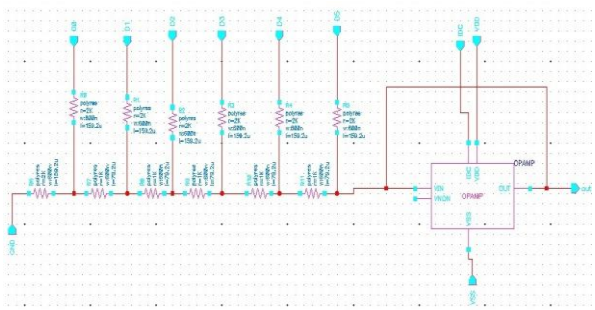

Fig.12:R-2R ladder DAC

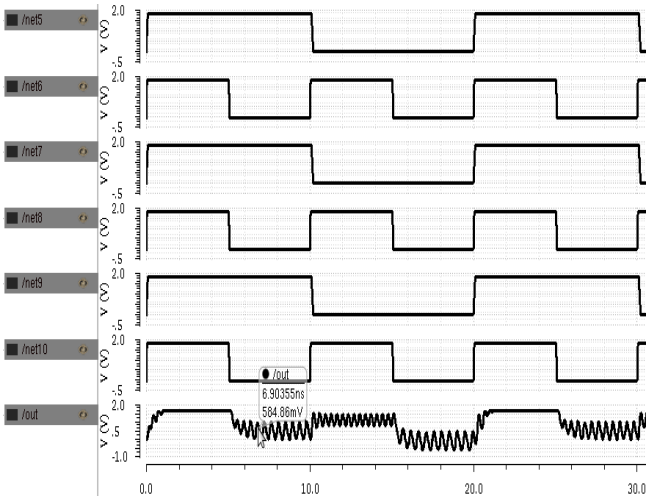

Fig.13:Waveform of R-2R ladder DAC

Figure 13 shows the output of 6bit R-2R ladder DAC. For the input 111111 the output is 1.8V.For 101010 the output is 584mV.

TABLE II. COMPARISON

Parameter	R-2R ladder	Cyclic DAC	Modified cyclic
No.of transistor	8	36	25
Static power	-	201.09 pWatt	155.925pWatt
Dynamic power	-	210.09uWatt	146.29uWatt
Total power	223.9uWatt	210.1uWatt	146.3uWatt

Table 2 shows the comparison of R-2R ladder,Cyclic and Modified cyclic DAC in terms of power and area. Total power consumption of Modified cyclic DAC is smaller than that of the other two. And also have less number of transistors than that of Cyclic DAC.

The main advantage of a cyclic DAC is that it can convert any number of input bits to its analog voltage without any degradation. In the case of R-2R ladder DAC, the accuracy will get decreased as the number of bits increases. The figure 14 shows the output of 13 bit Cyclic DAC. The input is 1111111111110 and the obtained analog voltage is 481mV.

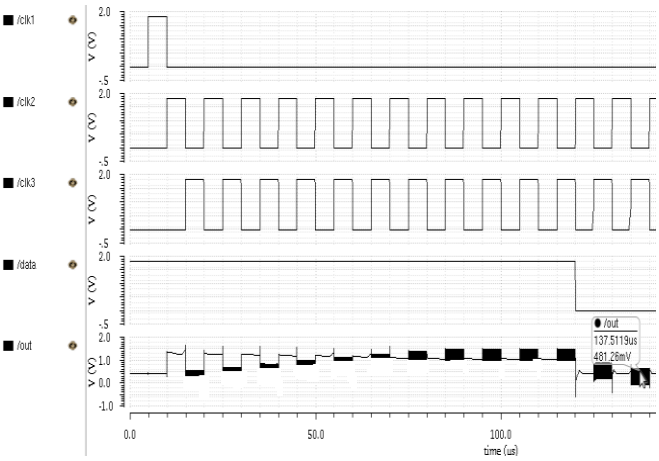

Fig.14:13bit Cyclic DAC

VII. CONCLUSION

An improved cyclic DAC and a comparative study of cyclic DAC as well as R-2R ladder DAC is discussed. The DAC circuit has been simulated in cadence tool. According to the performance evaluation results, it has been proven that the circuit is capable of converting any higher input bits. Modified cyclic DAC occupies less area and also reduces total power consumption.

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