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Design of Low Power Universal Asynchronous Receiver and Transmitter

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***Abstract* - Power dissipation is one of the key challenges in Electronic Circuit design and their performance in portable applications. Among high performance and high-density chips for example processors, high power dissipation restricts the amount of on chip transistors and increases the demand of essential heat removal, and that lessen the performance and increases the cost and size of the system. Consequently, analysis, power estimation along with optimization are vital challenges for CMOS Circuit design. Dynamic power dissipation is occurred when there is switching activity at some nodes in a CMOS circuit. Dynamic power dissipation is directly proportional to activity switching rate. In this paper, precise and simple method has been proposed to minimize the dynamic power dissipation in UART.**

Keywords – Dynamic power, switching activity rate, counter, protocol, data communication

I. INTRODUCTION

Speed, power consumption and area are some of the major quality matrix of any digital system. [1]. In CMOS circuit there are three kinds of power consumptions. Dynamic power consumption which occurs because of charging and discharging of the circuit capacitance, short circuit power intake results from the direct current flows from supply to ground while gate switching, lastly static power consumption which happens due to leakage current[2,3,4]. However dynamic power analysis of UART has not been given much attention by researchers [5,6,7,8]. UART which stands for Universal Asynchronous Receiver and Transmitter is the electronic circuit which has been used for serial data communication using serial data communication protocol. The most important characteristics of UART are that it is used for short distance and consumes very low amount of energy[7]. There are multiple transmission modes in UART such as Simplex mode in which one way transmission is done ,Half Duplex where at a time either it transmits or it receives and Full Duplex where both transmission and reception works simultaneously .This paper presents practical analysis technique of gate switching activity factor power consumption in UART. [2]

UART Design comprises three major block as shown in figure 1- transmitter, receiver and baud Rate generator. In UART transmission, transmitter takes the data in parallel form and transfers the data in serial form and on the other end receiver process the data serially and converts it into parallel from. In order to get successful transmission in UART, baud rate for both transmission and receiving should be the same[7].

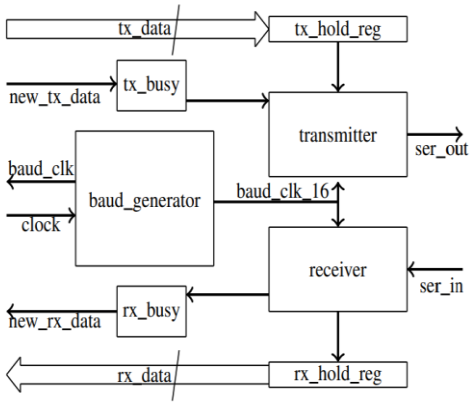

Fig. 1 UART Block Diagram [11]

In UART starting bit is fixed to LOW and that initiates bit synchronization of the word and at the receiver end it is followed by data word which signifies the data that will be transmitted. The least significant bit (LSB) is sent out first followed by next bit till the most significant bit (MSB) is transmitted .If parity is enabled it could be either odd parity or even parity. Stop bit is fixed to HIGH to provide word-framing which is used in bit synchronization at the receiver .Transmission is initiated with start bit – 0 tailed by data bit and an optional parity bit which finally finishes with stop bit – 1.[14]

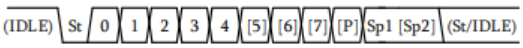

Fig.2 UART Packet Configuration [9]

. Baud rate generator is a Pulse generator that generates a tick pulse or also known as frequency divider circuit. The standard baud rates at which UART operates are 1200, 4800, 9600, 19200, 38400 bps. Baud rate of receiver and transmitter must be same in order to ensure that the transmitter and receiver are synchronized and excluding the necessity of the clock. This module has a clock signal, reset signal as Input and tick signal as Output.[14]

II. PRINCIPLE OF SWITCHING RATE ACTIVITY

Since the value of input and output constantly changes, and circuit which comprises of capacitive loads at different points are charged and discharged, leads to power dissipation. This phenomenon is called switching power dissipation. A model of dynamic power dissipation analysis is shown in figure 3[13].

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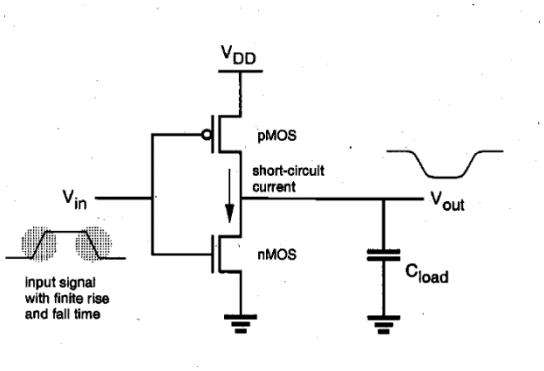

Fig 3. Dynamic power dissipation model [12]

Where C_{load} is the total output load capacitance and V_{DD} is the supply voltage, f is a clock frequency. Power dissipation in CMOS inverter is

$$P_d = C_{load} * V_{DD}^2 * f \quad (1)$$

We know that dynamic power expression of an inverter whose load capacitance is C_{load} can be calculated with expression $C_{load} * V_{DD}^2 * f$. In current scenario we have assumed that output is switching in rail to rail format and input is also switching in each clock cycle [12].

But in case of a complex circuit, for example in NAND gate apart from the output load we also have to consider the capacitance present at the other node of the gate.

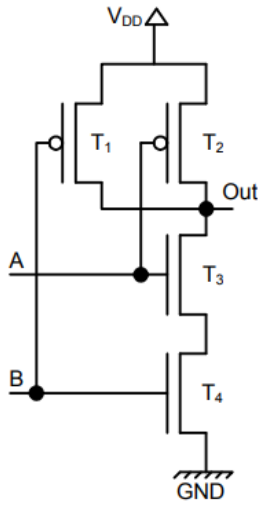

Fig 4. Schematic of NAND gate[15]

Now this capacitance in the nodes is getting charged and discharged simultaneously and its also possible that while switching the clock the capacitance node of the gate is not switching so in this scenario concept of switching activity is introduced. switching activity factor determines actual number of power-consuming voltage transitions faced by the output capacitance in each clock cycle

For the complex logic gate, average power dissipation is [13]

$$P_{avg} = \left(\lim_{N \to \infty} \frac{n(N)}{N} \right) C_L V_{dd}^2 f. \quad (2)$$

Where, f is a clock frequency and $n(N)$ is the number of 0-to-Vdd output transitions in the time interval $[0,N]$, C_L is the total output load capacitance V_{DD} is the supply voltage.[13]

$$\alpha_{0 \to 1} = \lim_{N \to \infty} \frac{n(N)}{N}. \quad (3)$$

α is the switching activity factor This provides the expected (average) value of the number of transitions in each clock cycle, which is known as the switching activity. Dynamic power consumption in complex logic gates is

$$P_d = \alpha_0 C_L V_{dd}^2 f + \sum_{i=1}^{k} \alpha_i C_i V_i V_{dd} f \quad (4)$$

where α_i is the switching activity at the ith internal node and α_0 is the switching activity on the output node, f is clock frequency . Here, it is presumed that there are k internal nodes. Algorithmic optimization can be used to minimize the switching activity in CMOS digital integrated circuits along with circuit level optimization. Due to transient switching activity of the CMOS device, dynamic component of power dissipation arises.

III. PROPOSED METHODLOGY

As we are aware that Baud rate Generator works as frequency divider circuit which consists of binary counter. One major characteristic of binary counter is that half of all sequential binary increment action requires that two or more counter bits must change. But this way of functioning has huge effect on switching activity at architectural level. We have applications where data modifies sequentially.
In order to lessen the number of transitions we have used Gray code counter instead of binary counter in the baud rate generator. We can see the grey counter logic in figure 4 .

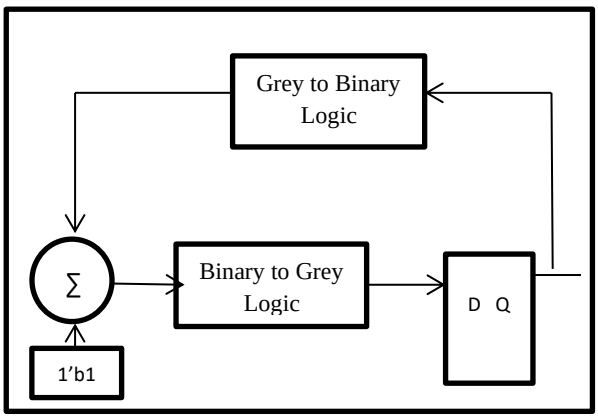

Fig 4 . RTL Design of Grey Co

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IV . SIMULATION RESULTS

Simulation and synthesis has been done using Xilinx Vivado. In this simulation the baud rate generator which is one of the block of an UART protocol has been designed by both binary counter and Gray counter as shown in figure 5 and 6 .

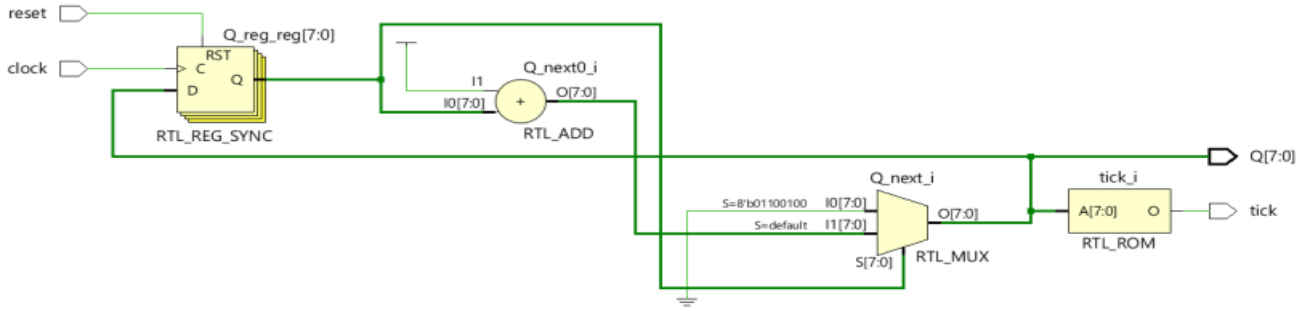

Fig. 5. Proposed Design of Grey Counter

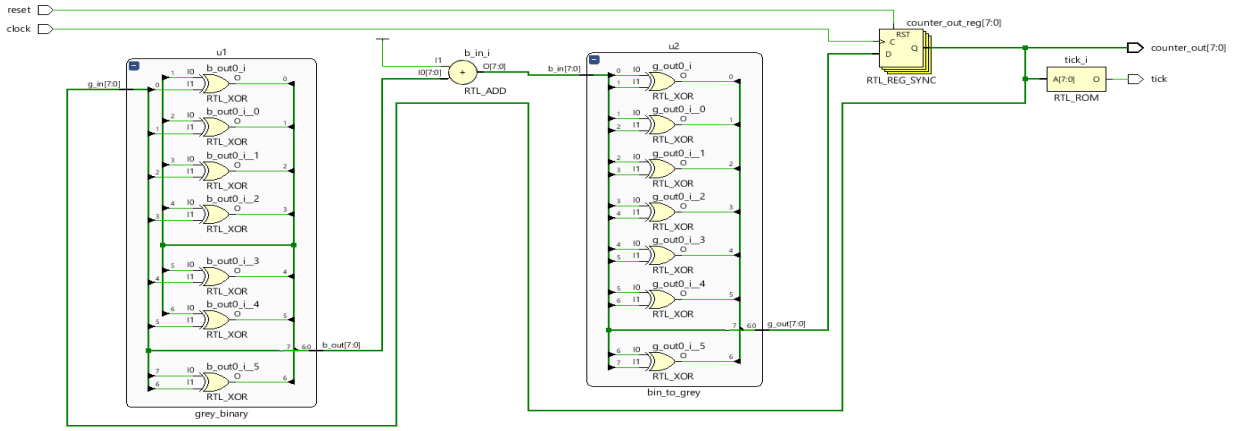

Fig.6 RTL Schematic of Baud Rate Generator using Grey Counter

The total on chip power , dynamic power and static power of UART which we have designed from binary counter is illustrated in Table 1 below.

TABLE I. Result Of UART Blocks Using Binary Counter

	Total On Chip Power(W)	Dynamic Power(W)	Static Power(W)
Baud Rate Generator	4.100	4.010	0.090
UART Transmitter	0.550	0.468	0.082
UART Receiver	0.381	0.299	0.081

And the total on chip power , dynamic power and static power of UART which we have designed from grey counter is illustrated in Table 2 below.

TABLE II. Result Of UART Blocks Using Grey Counter

	Total On Chip Power(W)	Dynamic Power(W)	Static Power(W)
Baud Rate Generator	1.505	1.421	0.084
UART Transmitter	0.351	0.269	0.082
UART Receiver	0.151	0.070	0.081

V. CONCLUSION

As per the simulation results comparing the binary coding with Gray coding we can come to the conclusion that it helps in reducing the state switching considerably and Power optimization is up to 36.1 % for transmitter and 61.6 % for Receiver .

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