Design of Low Voltage High Speed Operational Amplifier for Pipelined ADC in 90 nm Standard CMOS Process

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Abstract

This paper presents the low voltage high speed operational amplifier for pipelined ADC in 90nm standard CMOS process. The designed Opamp can operate at a supply voltage of 1V and provides a gain of 81.11 dB, unity gain frequency of 485.2MHz and slew rate of 239.62V/µs with 12ns settling time. The schematic is captured using Cadence Virtuoso and simulated using Cadence Spectre simulator in 90nm CMOS technology. The designed Opamp satisfies the requirements of a pipelined ADC and can be utilized in the S/H block of pipelined ADC.

1. Introduction

In the past few years, mobile phones have become a very common thing for every individual and the number of subscribers is increasing day by day which requires the base station of a cell to be very fast. Analog to digital converters are very basic part to any base station receiver .So high speed ADC architecture like pipelined ADC is used in UMTS base station receivers [1-3]. The most important part in a pipelined ADC is the operational amplifier which is used in Sample and Hold (S/H) circuit. In this paper, design of a high speed operational amplifier for pipelined ADC is presented which can provide a d.c. gain of 81.11dB, unity gain frequency of 485.2MHz, slew rate of 239.62V/µs and settling time of 12ns. The Speed of an operational amplifier is determined by the rate of change of output voltage with time. The change in output voltage occurs in two manners which are linear and non-linear settling (or slewing).Linear settling depends on Unity Gain Frequency and the non-linear settling depends on slew rate [4]. Slewing is a large signal phenomenon which occurs when one of the input signals is much larger than the other. In this situation one of the input transistors turns off and the Opamp behaves as non-linear device and the output capacitor charges with a constant current [5].When the output decreases, the transistor turns ON and linear settling occurs. The Opamp used in S/H circuit of pipelined ADC also requires a very high gain so some sort of gain enhancement technique [6-7] is required which is discussed in section 3.

2. Basic Opamp topologies

A number of Opamp topologies exist in literature, each having its own advantages and disadvantages, some topologies have a very high gain but less swing and speed, some have well speed but the gain is not adequate, some topologies are a mixture of more than one basic topologies. So an appropriate blend of these topologies is required which can provide very high gain, swing, speed and UGF but less power dissipation. The different topologies are discussed in this section.

A. Simple differential amplifier

A simple differential amplifier is simply two single ended amplifiers which are given differential inputs and the differential output is taken. A tail current source provides a constant current to make the sum of two currents independent of the input common mode level. A fully differential configuration [8] provides a good swing as compared to single ended amplifier and supresses the supply noise. A simple differential amplifier is shown in Fig. 1.

The gain of a simple differential amplifier is

$$A_v = g_{m1}\,(r_{o1} || r_{o3})$$

The swing of differential amplifier is twice as compared to the swing of a simple common source amplifier.

$$V_{out} = 2(V_{dd} - V_{od3} - V_{od1} - V_{Iss})$$

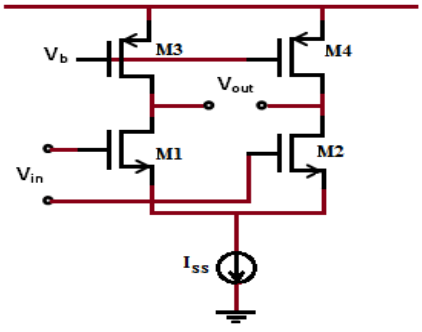

Fig. 1 Simple differential amplifier

B. Telescopic amplifier

A telescopic amplifier [9-11] is simply the extension of amplifier shown in Fig. 1 where the input and load transistors are replaced by cascode pairs so as to increase their output resistance which increases the gain of the amplifier given as

$$A_v = g_{m1} [(g_{m3}.r_{o3}.r_{o1}) \,||\, (g_{m5}.r_{o5}.r_{o7})]$$

The detailed schematic of telescopic amplifier is shown in Fig. 2.

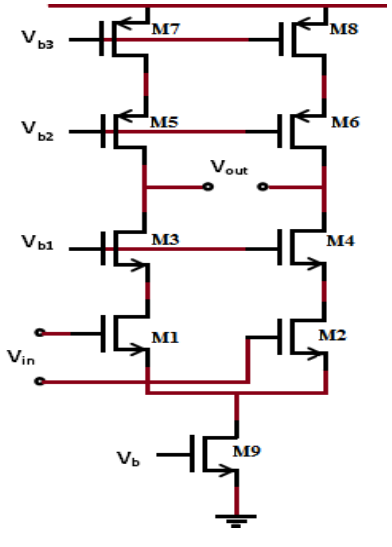

Fig. 2 Telescopic amplifier

Besides its high gain, this topology is not used because of small voltage swing which is limited by the overdrive voltage of five cascode transistors. The minimum and maximum value of single ended swing is given by

$$V_{out,\,min} = V_{od1} + V_{od3} + V_{od9}$$
$$V_{out,\,max} = V_{dd} - V_{od5} - V_{od7}$$

The overall swing at one end of output is given as the difference of maximum and minimum swings.

$$V_{out} = V_{out,\,max} - V_{out,\,min}$$

C. Folded cascode amplifier

Folded cascode is used to increase the output swing of cascode amplifier. As shown in Fig. 3, this amplifier folds the input transistors to either V_{dd} or ground and two tail current sources are applied at the point of folding. The gain of this type of amplifier is slightly less than the gain of telescopic amplifier (r_{o1} comes in parallel with r_{05}) but the swing is higher by the overdrive voltage of tail current source.

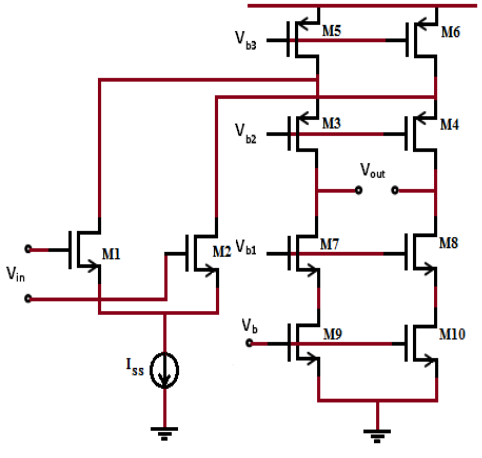

Fig. 3 Folded Cascode amplifier

The gain of folded cascode amplifier is

$$A_v = g_{m1} \{[g_{m3}.r_{o3}.\,(r_{o1}||r_{o5})] \;||\; [g_{m7}.r_{o7}.r_{o9}]\}$$

The swing of folded cascode amplifier is higher than the swing of telescopic amplifier by the overdrive voltage of tail current source .The minimum and maximum values of single ended swing are

$$V_{out,\,min} = V_{od7} + V_{od9}$$
$$V_{out,\,max} = V_{dd} - V_{od3} - V_{od5}$$

D. Two stage amplifier

As a single stage telescopic amplifier can provide good gain but swing is less, a simple differential amplifier have good swing but less gain. So, the gain and swing requirements trade with each other [12] but a two stage amplifier can be designed in such a way

that the gain and swing are independent. So the first stage can provide a high gain and second stage can provide a high swing and each can be controlled independent of each other. As shown in Fig. 4, first stage uses a telescopic amplifier which provides good gain while the second stage uses common source amplifier which consumes very less voltage headroom and hence provides a high output swing. The amplifier shown in Fig. 4 can be a combination of any of basic amplifier configurations e.g. it can be a simple differential amplifier or a folded cascode amplifier in first stage but the second stage is generally common source stage due to its high swing. Three stage amplifiers are also possible but rarely used because of speed limitations.

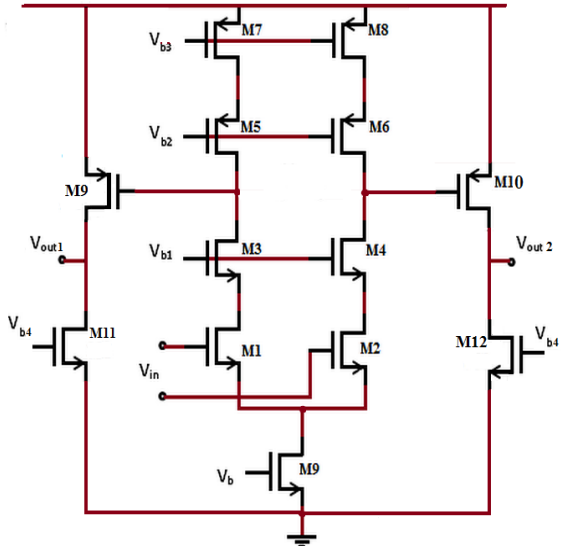

Fig. 4 Two stage amplifier

3. Proposed Design technique

A. Proposed design topology

The proposed design topology uses a folded cascode amplifier for high speed and swing and the gain boosting technique to increase the gain. The auxiliary amplifiers used in Fig. 5 for gain boosting are simple differential amplifiers which enhances the output resistance of cascode transistor pairs $M_{3,5}$ and $M_{7,9}$ resulting an increase in overall gain of amplifier.

B. Gain boosting

Gain boosting is a technique to increase the gain of operational amplifiers using auxiliary amplifiers to increase the output impedance of cascode transistor pairs [13-14]. Because the gain of an amplifier depends directly on the output impedance, so the gain of the overall configuration increases. Fig. 5 illustrates the gain boosting technique applied to folded cascode differential amplifier.

$$A_v = g_{m1}\{[A2.g_{m3}.r_{o3}.(r_{o1}||r_{o5})] \;||\; [A1.g_{m7}.r_{o7}.r_{o9}]\}$$

Here A1 and A2 are the gain of lower and upper auxiliary amplifiers respectively.

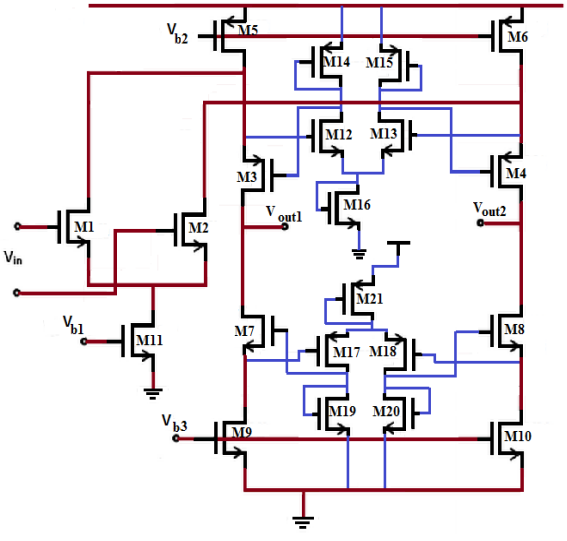

Fig. 5 Folded cascode amplifier with gain boosting

The aspect ratios of all the transistors are shown in Table 1.

TABLE I
ASPECT RATIOS OF TRANSISTORS

PARAMETER	VALUE
$(W/L)_{1-2}$	1.44µ/200n
$(W/L)_{3-4}$	1.08µ/800n
$(W/L)_{5-6}$	12.48µ/800n
$(W/L)_{7-8}$	480n/800n
$(W/L)_{9-10}$	600n/800n
$(W/L)_{11}$	960n/100n
$(W/L)_{12-13}$	1.8µ/800n
$(W/L)_{14-15}$	720n/800n
$(W/L)_{16}$	3.96µ/800n
$(W/L)_{17-18}$	120n/800n
$(W/L)_{19-20}$	120n/800n
$(W/L)_{21}$	480n/800n

4. Simulation results

The designed Opamp was simulated with Cadence Spectre simulator using 90nm CMOS technology. The aspect ratios of all the transistors are shown in Table 1.The gain and phase plot of Opamp are shown in Fig. 6, which exhibits a d.c. gain of 11362 i.e. 81.11dB which is sufficient enough for S/H circuit of pipelined ADC. It shows a unity gain bandwidth of 485.2MHz and the phase margin is 19.07 degrees.

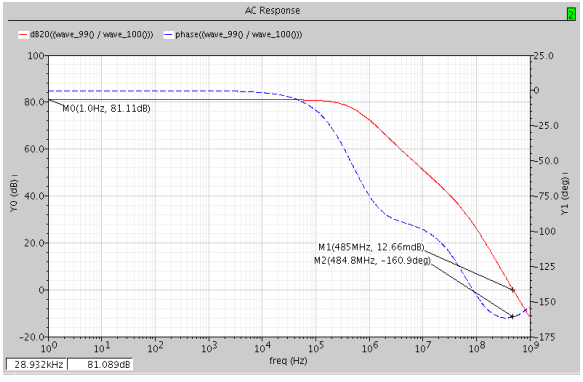

Fig. 6 Gain and phase plot of Opamp

A transient analysis was performed with a unit step input of 0.4V applied at one end and -0.4 V at another end with a very small rise and fall time (1ps) and the differential output is plotted against time, the slope of which shows the rate of change of output with time i.e. slew rate of 239.62V/µs indicating a steep increase in the output with time for large signals. The differential output reaches 99% of its final value within 12ns indicating a fast settling as shown in Fig. 7.

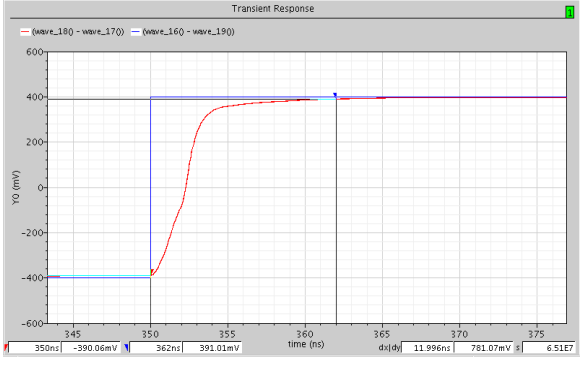

Fig. 7 Settling behaviour of Opamp

The designed Opamp is applied with a common mode sinusoidal input signal of 10mV, 10MHz and the CM gain is plotted with frequency as shown in Fig. 8 which shows a common mode gain of $7.582X10^{-6}$ i.e. -102.4 dB.

The CMRR can thus be calculated as

$CMRR=A_{v,\ diff}/A_{v,\ CM}$

The value of CMRR comes out to be 183.51dB.

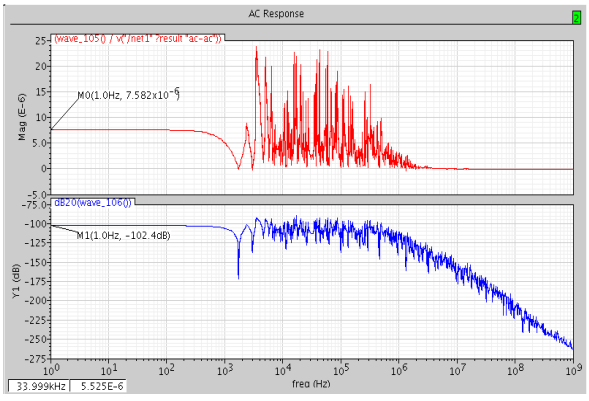

Fig. 8 CM gain as a function of frequency

To calculate the PSRR, an a.c. signal of 10mV, 50Hz is superimposed on Vdd with no input applied at inverting and non-inverting terminals and the gain w.r.t. supply voltage ($A_{v,\ PS}$) is plotted with frequency as shown in Fig. 9.The power supply gain is $3.94X\ 10^{-8}$ i.e. -148.1dB.

The PSRR is given by

$PSRR= A_{v,\ diff}/A_{v,\ PS}$

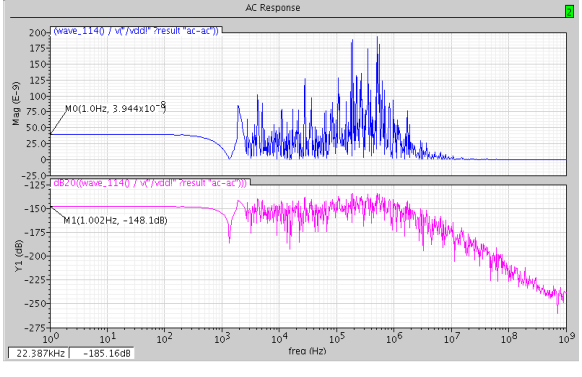

Fig. 9 Gain w.r.t. power supply plotted with frequency

The simulation results are summarised in Table 2.

TABLE II
SIMULATION RESULTS

PARAMETER	VALUE
Gain	81.11dB
Gain crossover frequency	485.2MHz
Phase margin	19.07°
Differential Output Swing	+/-0.8V

Slew Rate	+239.62 V/µs -239.41 V/µs
Settling time	12ns
Power Dissipation	73.72 µW
Technology	90nm
CMRR	183.51dB
PSRR	229.19dB

5. Conclusion

The designed Opamp achieved a gain of 81.11dB with a unity gain frequency of 485.20 MHz at a power supply voltage of 1V which meets the specifications of S/H circuit for a pipelined ADC. The designed Opamp achieved a high slew rate of +239.62V/µs and -239.41V/µs and settling time of 12ns which is in accordance with our specifications of high speed ADC.However it suffers from a low phase margin which can lead to instability in closed loop configurations of Opamp.

6. References

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