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Design of Multilevel Inverter to Improve the Power Quality by Reducing the Harmonics

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***Abstract*—Multilevel output voltage source converters are emerging as a new methodology of power converter options for high-power and medium power. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of dc Source .this paper present a new method multilevel inverters ,which has the less number of switching devices used and no any capacitor and inductor dependency to smooth output current wave. it comprises input dc source alternatively connected in opposite polarity with an another switching devices' and the design has been fully investigated with the help of theoretical analysis, simulations with the MATLAB / SIIMULINK and reduced THD result are shown through the FFT window, comparison with the proposed topology is made against the typical commercial available inverter topology.**

Keywords—Multilevel inverters, MLI, hybrid topologies, asymmetric and symmetric source configuration, CHB, THD.

I. INTRODUCTION

In recent years , multilevel inverter dependency has been increasing, it provides lowest harmonic distortion profile, lower switching losses and conduction losses even multilevel provide higher staircase voltage level this output voltage level increased power rating, reduced dv/dt stress of load possibilities, capability of high efficiency and low electromagnetic interference [2-3]. Even Industrial and domestic power demand increasing, also desired for adjusting the requirement of power, moved to renewal energy recourses, multilevel voltage source have vital role to help in convert high power dc to ac, this high power is reached in megawatt range, it is typical to direct connection of high power and medium power to electronics devices, multilevel methodology helps to withstand devices with the high power [1] .

MLI has given better Total harmonic Distortion (THD) profile and the improve the efficiency instead of increased the system complexity as the gate driver circuit and the large number of electronics devices, capacitor, inductor used hence the system increase the effective cost and reduce the system liability and efficiency. The solution of the above problem is reduction in the number of switches and gate driver circuit. [7]

The three different type of topology has been seen in commercial used as the 1. Diode clamped MLI (DC-MLI), this method use higher number of clamping diode are required when the number of level increased also typical to control of real power flow 2. flying capacitor MLI (FC-MLI),this topology need higher number of bulky capacitor and required to balance charging and discharging of capacitor, and 3.Cascaded H-Bridge MLI (CHB-MLI), Diode clamped MLI (DC-MLI), a with these methods mostly have to use large number of power electronics switches, as the number of switches increases the switching power loss increases with the electronics devices. Researchers are working on to reduce the component used in the MLI topologies. Asymmetrical voltage sources uses less number of components [1-2].

In this paper present comparative study among three circuit as 5-level, 7-level, 9-level and classically present topology, gives the performance study mainly focused on the 9-level and give comparison between THD. This proposed method is used less number of power switching devices that's help to reduce switching losses and improve the performance related to the complexity and reliability comparison to the classical present methods, this topology can be say the family of cascaded hybrid bridge (CHB) there reason to say (i)it used the separated DC voltage source from the renewal energy sources where we get the large number of separated DC sources ,(ii)it offers the voltage additive value to increase the voltage level as the asymmetric voltage sources. It shows the opposite polarities DC voltage Sources are connected to the power switching devices, every power switching device shows the work under different switching frequency and voltage stress.

II. MODIFIED MLI TOPOLOGY

A. Structure

Nine level inverter shown below in fig.1. It has the three voltage sources $\mathbf{E_1=12v, E_2=24, E3=12}$, which use the adding phenomena, gives the different nine level voltage, this voltage source are connected opposite potential with the power switches. and four pair of active power switches which used as main and complementary switch, switch ($\mathbf{S_i, G_i}$) **i=1,2,3,4**

. Where S main switch and G is used as complementary switch. Power switch can be as IGBT or MOSFET with anti parallel diode, there is MOSFET has the higher switching losses so that's why prefer IGBT as switching device.

TABLE I.SYSTEM PARAMETERS

System Parameters	Value		
Reference frequency	50 Hz		
Carrier frequency	1200 Hz		
Load resistance	1Ω		
Load inductance	3 mH		
DC Source	E_1=12v	E_2=24v	E_3=12v

II. DESIGNED MATLAB/SIMULINK CIRCUITE

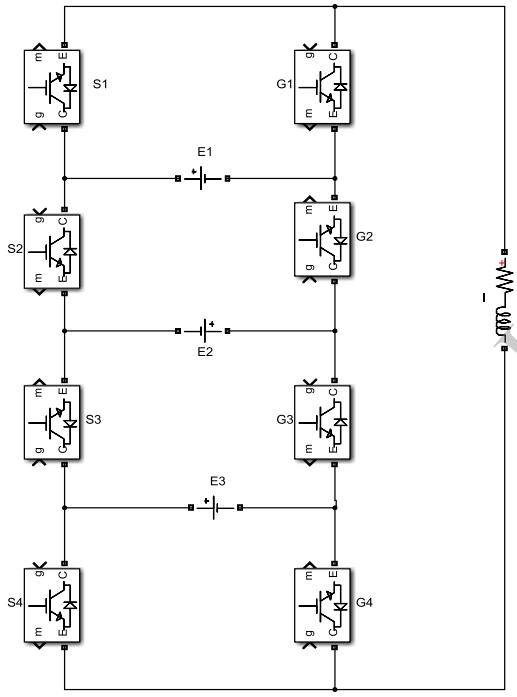

Fig.1. Main circuit

B. Working

The working states shows of nine level inverter table no.1 which shows the nine different voltage levels **+/-V, +/-2V, +/-3V, +/-4V, 0V .** We have seen that two zero states and remaining eight non zero states after adding build the different nine level voltage, and also four switch conduct continuously in every different state and remaining switches working as in blocking mode. Switch pair showing as main complementary switch and this switch pair has the different switching frequency and voltage stress, for examples **V_4=12+24+12= 48v** gives when **S_1, S3, G_2, G_4** conduct simultaneously remaining switch **S_2, S_4, G_1, G_3** work as in blocking mode.

TABLE II.MODES AND SWITCHING STATES

Level Of Voltage	Modes	Load Voltage[V]	ON State Switches
0	1	0	G_1,G_2,G_3,G_4
E1	2	12	S_1,G_2,G_3,G_4
E2	3	24	S_3,S_4,G_1,G_2
E1+E2	4	36	S_1,S_2,S_3,G_2
E1+E2+E3	5	48	S_1,S_3,G_2,G_4
0	6	0	S_1,S_2,S_3,S_4
-E1	7	-12	G_1,S_2,S_3,S_4
-E2	8	-24	G_1,S_2,S_3,S_4
-(E1+E2)	9	-36	G_3,G_4,G_1,S_2
-(E1+E2+E3)	10	-48	G_1,S_4,G_3,S_2

III. UNIPOLAR SWITCHING SCHEME

Improvement of power quality moved to high frequency switching scheme as the available high switching frequency scheme SPWM and SPACE VECTOR PWM, SPWM scheme is easy produce, multicarrier level shift phase disposition pulse width modulation switching scheme used in nine level topology. the scheme is produce different pulse width and higher number of voltage level help to make closer current sine pulse so that produce less THD with least voltage stress ,where S_2,G_2 has higher voltage stress and used fundamental frequency(50hz) , S1,G1 has the least voltage stress,

Voltage stress of different power switch

$$S_2, G_2 > S_3, G_3 > S_4, G_4 > S_1, G_1$$

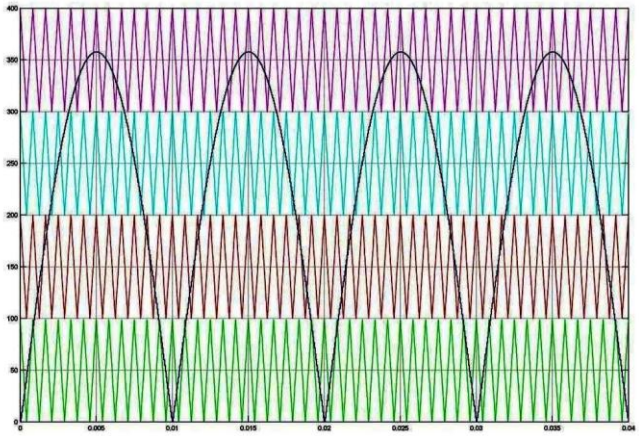

Fig.2.Refrance and carrier waveform for nine level inverter

used reference wave (sinusoidal) frequency 50hz and triangle carrier wave (triangle) frequency 1200hz compare with the relational operator result of shows in fig.2 and fig.3.comparsion with the reference gives '1' when reference

is greater than triangle wave otherwise gives ‘o’ .this switching pulses added to each other get the aggregated signal, aggregated signal compare with the constant its output shows the different switching signal.

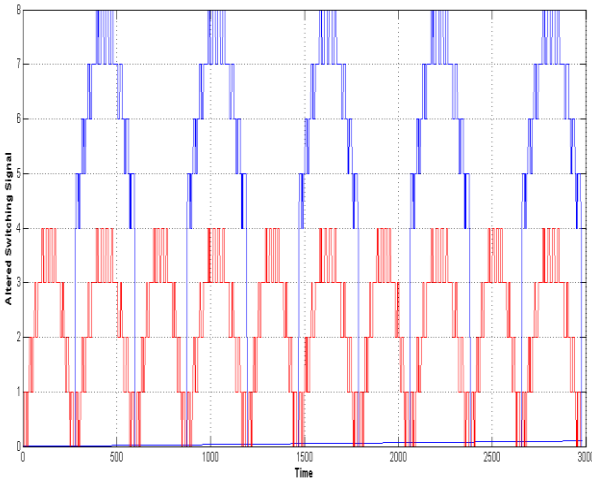

Fig.3. Altered signal

The different gate driver signal for different power Switches, shown in Fig.4

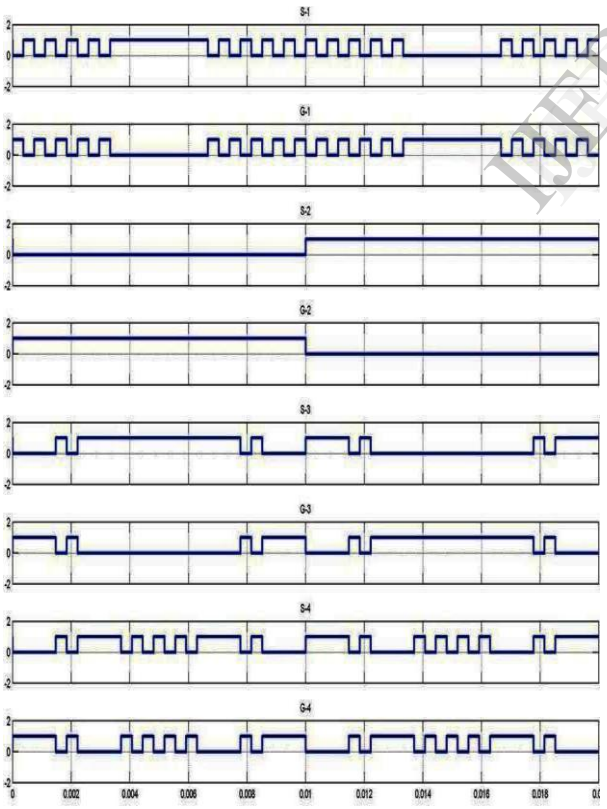

Fig.4.Switching Pulses for the nine level inverter.

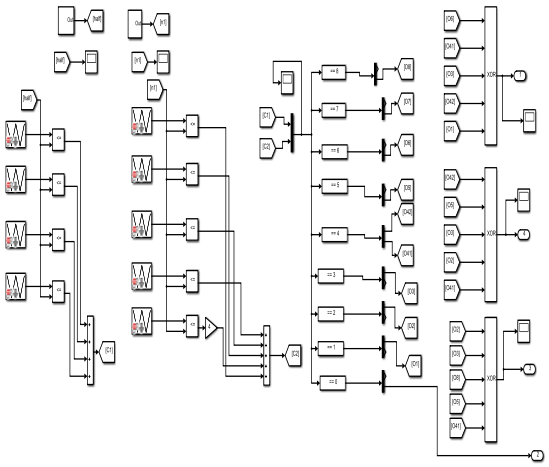

Fig.5. Switching Scheme in MATLAB canvas.

IV. SIMULATION RESULTS

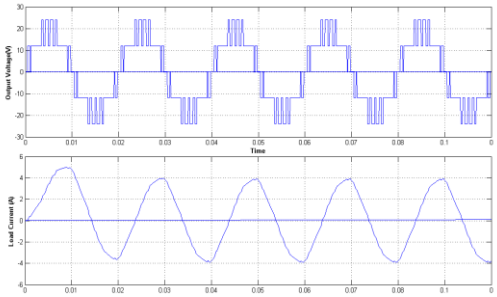

Fig.6. Voltage and Current waves of 5 level MLI

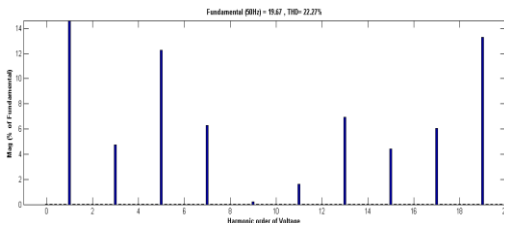

Fig.7. Voltage FFT window of 5 levels MLI

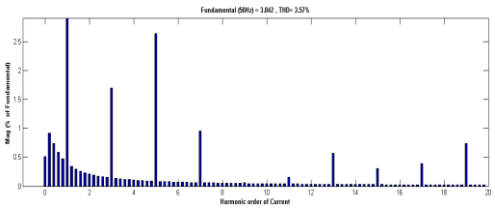

Fig.8. Current FFT window of 5 levels MLI

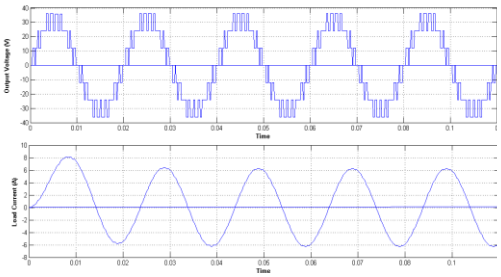

Fig.9. Voltage and Current waves of 7 level MLI

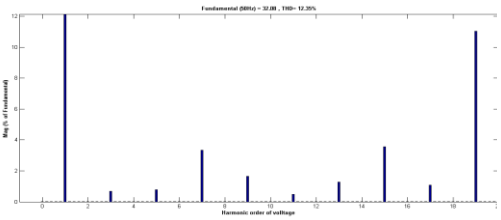

Fig.10. Voltage FFT window of 7 levels MLI

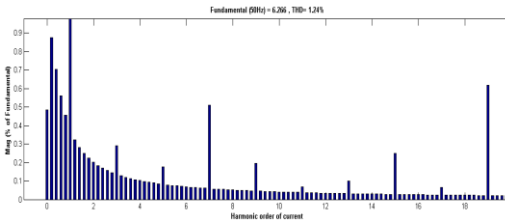

Fig.11. Current FFT window of 7 levels MLI

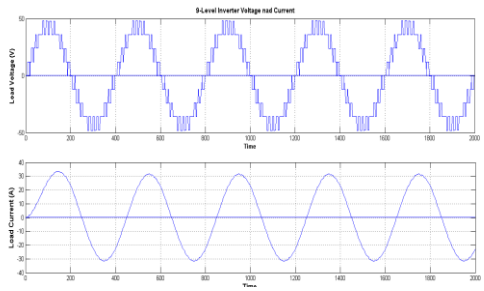

Fig.12. Voltage and Current waves of 9 level MLI

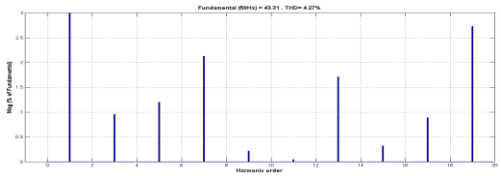

Fig.13. Voltage FFT window of 9 levels MLI

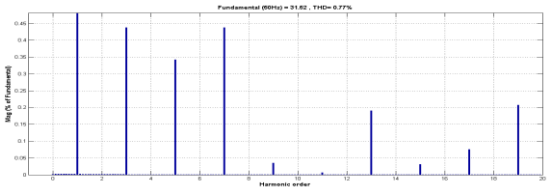

Fig.14. Current FFT window of 9 levels MLI

V. COMPARATIVE STUDY

In comparisons of traditional available multi level inverter, and new multi level hybrid inverter, as the number of voltage level increases the simultaneously the power electronics switches and other components also increases such as IGBT, capacitor, inductors and diodes. In case of flying capacitor MLI's are need capacitor balancing which increases the system complexity, even diode clamping MLI's needs higher number of diodes which increases the system cost and Cascaded H-bridge needs higher number of DC source. Overall comparative study shown in the table no.III and table no. IV respectively.

TABLE III. COMPARISON BETWEEN DIFFERENT LEVELS

Inverter	Fundamental voltage[V]			Frequency [Hz]	Voltage (THD) %	Current (THD) %
	E_1	E_2	E_3			
5-level Inverter	12v	12v	NO	50	22.27%	3.53%
7-level Inverter	12v	24	NO	50	12.35%	1.12%
9-level Inverter	12v	24v	12v	50	4.27%	0.77%

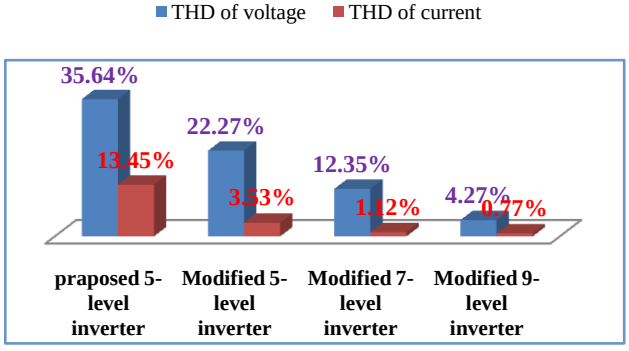

Fig.15. comparison between present classical topology its component.

TABLE IV. COMPARISON OF ELEMENTS, BETWEEN DIFFERENT COMMERCIAL AVAILABLE INVERTER WITH HYBRID MULTILEVEL INVERTER

Inverter Configuration	Diode-Clamp	Flying-Capacitors	Cascaded inverters	New Hybrid MLI
Main switching devices	2(m-1)	2(m-1)	2(m-1)	m-1
Main diodes	2(m-1)	2(m-1)	2(m-1)	0
Clamping diodes	(m-1) (m-2)	0	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2	0
Balancing capacitors	0	(m-1) (m-2)/2	0	0

VI. CONCLUSION

The nine levels inverter reduce the number of elements such as the capacitor, inductor, and diode and increase output voltage level, it helps to reduces the system cost and also improve the total harmonic distortion profile compared with other present classical topology. This configuration of nine level topology uses the asymmetric voltage, that's why it needs less number of DC sources by which reduce number of power switches and its gate driver circuit. even advantage of reduction in requirement of DC sources in system it help to increases fault tolerant capability. This paper present comparative study with in term of effective cost, THD and shows the all analytical comparison. Over all reduce the THD and increase the efficiency.

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