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Design of Pass Transistor based Phase Frequency Detector for PLL Applications

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***Abstract*— The phase frequency comes under the phase locked loop system. PLL assures the output signal with same phase and frequency as that of the input signal. The main propose of this phase frequency detector is to reach low power consumption, fast frequency acquisition in the PLL, mainly for synchronization, clock generation ,skew jitter reduction, clock recovery. With growing technology, there is a requirement of PLL circuit with faster locking ability. This paper is about redesign of phase frequency detector for PLL system using 180nm technology (GPDK180) in CADENCE VIRTUSO Analog design with 1.0v supply voltage. For designing this circuit it requires only 6 transistors and operating frequency 8GHz**

Key Words: Phase locked loop, Pass transistor, Tri-state machine, CADENCE.

I. INTRODUCTION

In recent few years, the design of low power and low jitter PLL for application has become big task in VLSI design; many came with different technology to reduce the power consumption and reduction in jitter in VLSI circuits. For many communications like applications PLL generates on-chip clocks. PLL is a feedback system that fixes phase relationship between its output clock and input reference clock. PLL generates a signal with the same phase as that of a reference signal, for achieving this we have to see many iteration of comparison of the input Vref signal and output signal (feedback signal). The components of PLL are loop filter (LP) phase frequency detector (PFD), voltage controlled oscillator (VCO), charge pump (CP), and Frequency divider as in Fig 1.

Heart of the PLL circuit is the phase frequency detector (PFD) .The concept under lying behind PFD is to compare two input signal's phase and frequency. Depending upon the phase and frequency deviation it gives two non-complimentary outputs which are Vup and Vdown. The both outputs of PFD are combined by using charge pump circuit to give single output. This output intern given to a low pass filter whose output is DC control voltage.DC control voltage controls the phase frequency of VCO. If the PFD out is Vup signal, the error voltage increases at the output of LPF, that causes the VCO output frequency to increase. For DOWN signal, the VCO output signal frequency decreases. The work concentrates on design of non-linear device PFD. Only 6 transistors are used by pass transistor based PFD design. Phase noise, output noise and jitter are calculated for this PFD.

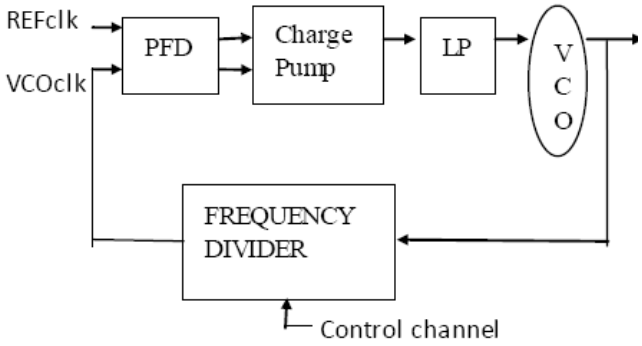

Fig -1: Block diagram of PLL

2. CONVENTIONAL PFD

PFD is heart of the PLL system for generating clock signal. PFD is better than phase detector and frequency detector because PFD detects phase and frequency at a time. Observing the phase deviations is important in PFD because it affects overall performance of PLL, for example dead zone, jitter, lock -time and phase noise. Phase detector is implemented by using NOR gate latches for D Flip-Flop. Traditional PFD architecture is implemented using finite state machine having four states. Fig 2 describes the overall functionality of PFD using state transition diagram.

The two non-complementary outputs Vup and Vdown are generated by Finite State machine. The generated output depends on the response of their inputs Vref clock and Vvco clock .PFD will have one state out of the four stste at any point of time. The states are as fallows.

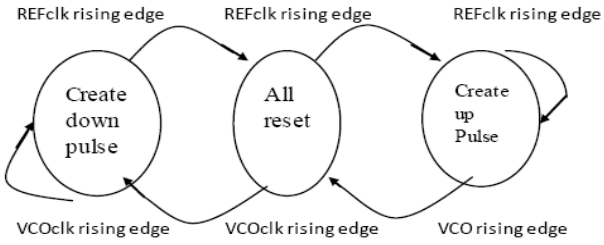

Fig 2.Tri-state finite state machine diagram

Vup= logic 0 and Vdown= logic 0
Vup= logic 1 and Vdown= logic 0
Vup= logic 0 and Vdown= logic 1
Vup= logic 1 and Vdown= logic 1
Both REFclk and VCOclk having same frequency ,Vup pulse leads the Vdown by difference in the phase of two input signals when REFclk leads the VCOclk in phase i,e Vup=logic 1,Vdown= logic 0,otherwise Vup=logic 0 and Vdown =logic 1.If the frequency and phase of both signals are same, then Vup = "0"and Vdown = "0". Operation of sequential circuits mainly depends on either raising or falling times of triggering edge.

2.1 DESIGN ISSUES WITH PFD

Some of issues like: a) Blind zone, this is due to when PFD is unable to identify the small phase difference in their inputs, it gives a region of small gain i,e zero gain near the phase lock. The region with low gain is known as dead zone. the wrong polarity in the output of PFD caused by blind zone due to the frequency insensitivity of the PFD. The frequency insensitivity of the PFD to any transitions in the input signals in known as blind zone. Blind zone causes wrong polarity in the PFD output, which effects the behavior and increasing the acquisition time, which in turn alters the frequency. At high frequency, particularly in the PLLs used for optical communication, this is a major problem. Phase detection range is degraded by blind zone. b) Variations in the supply and substrate interference of output is because of deviation of threshold from the ideal case called Jitter. c) Trade-off between Power consumption and phase noise .To measure the PFD performance noise is the main parameter. The power consumed by the device increases with decrease in the phase noise performance, they are inversely proportional to each other.

3. PRESENT PFD ARCHITECTURES

Many used the concept of state diagram and came up with several design topologies. The D-FlipFlop and reset path using NAND gate are used in the conventional PFD architecture. Due to the delay caused by the internal components of flipflop .i,e delay because of gates and reset time.Because of this D-PFD was unable to detect the phase error,when it is in dead zone region and this was the major drawback. Due to complex design it features static power dissipation, phase.There is trade-off between power consumed and phase noise performance i.e the power consumed by the device increases with decrease in the phase noise performance, they are inversely proportional to each other. Due to this at a higher rate noise performance is lowered.By taking the concept of tri-state PFD using 16 transistors the modified PFD came with new architecture and it over comes the complexity. Architecture using AND gate and a NOR gate called fully differential PFD topology came with much better phase noise than modified and D-FF based PFD, and it is free from dead zone problem. Due to circuit complexity it draws more power. Falling edge topology came with only12 transistor; it operates only on the negative edge of the inputs and with high voltage levels, but at high levels device will not function as that of traditional. New topology called GDI cell based PFD with high operating frequency, less power consumption came with using only 4 transistors, and less power is due to its simple and small area.

4. PROPOSED ARCHITECTURE OF PASS TRANSISTOR BASED PFD

To improve the performance of design in low power digital circuit we used the pass transistor logic (PTL).Pass transistor it is like electronic switch with properties like non-mechanical relay, uses CMOS technology. Some of merits of PTL over standard CMOS design are: a) Low power dissipation, as it uses less number of transistor. b) It requires less area hence low interconnection. c) High speed because of small node capacitances. However most of PLL implementations incur with two main basic problems. First, Reduces the current driving capability due to the threshold drop at single-channel pass transistors, due to this at reduced supply voltages the circuit operation gets slower, Second, high input voltage level is not regenerative at inverter pass transistor gate. The PMOS transistor of inverter is not possible to turn off with reduced voltage level, thereby causing power dissipation to be significant factor.

Pass transistor logic(PTL) will not use fixed power supply value, they are single FETs and pass the signal from source to drain or from drain to source with less area, but cannot pass entire voltage range. Mobility of PFETs is less than that of NFTs. So NFTs are used for this application. High mobility NFETs increases the switching operation than PFETs with same area. In the proposed circuit design a set of controlled signals are applied through the gate of NFETs.

Proposed design is by taking both the concept of tri-state machine and pass transistor gate concept. Finally called as the pass transistor PFD (PT _ PFD) as show in below figure 3. It works much closure to conventional PFD. For generating qualitative clock the PT-PFD is a better architecture. This circuit designed with less complication. From study research methods it was found that all types of PFDs uses more number of transistors, but proposed PT-PFD circuit is designed with only six transistors.

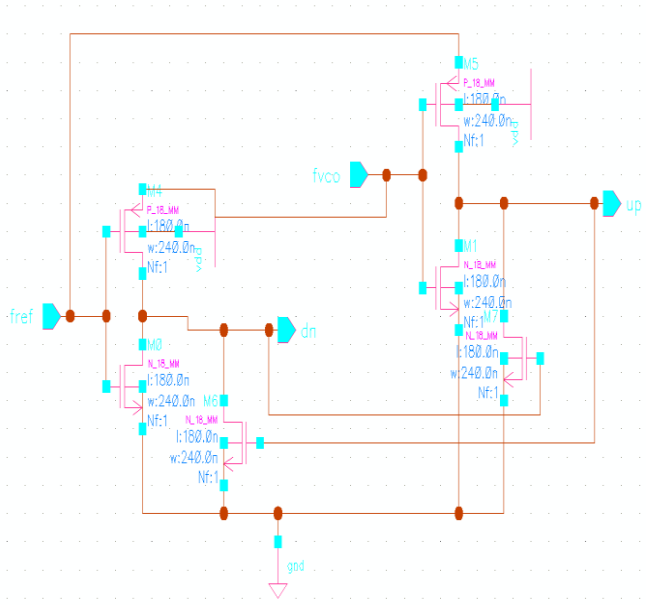

Fig 3.Circuit diagram of PT-PFD

The performance is calculated on many parameters for example, phase noise, power consumption, jitter, maximum operating frequency, output noise.

The quality of clock signal is known from the how much percentage of jitter and phase noise is in the signal or clock, jitter in the PFD will show noisy operation. Jitter in PFD represents the noise. Substrate interfaces, supply noise and variation in supply presents the two major problems i.e Jitter, noise. Thermal noise from NMOS and PMOS channel causes the output noise to vary.
The fluctuation of threshold crossing occurs because of substrate coupling with a clock and also due to the susceptibility to the supply. Propagation delay time at Vth changes due to supply variations with respect to time. Phase noise increases the with operating frequency but inversely proportional to power consumed by device, hence there us trade-off between power consumption and phase noise. So select off-set frequency such that phase noise and power consumption will have optimal trade-off.

5. SIMULATION RESULTS

This paper presents a PFD design for PLL; we have designed and implemented the PFD circuit using pass transistor and tri-state state machine concept. The circuit is implemented using GPDK 180nm CMOS technology VDD is chosen to be 1V.With 50MHz several parameter are measured for example jitter, phase error, phase noise, power consumption and maximum operating frequency. Fig 4 describes PFD operation with both inputs having same duty.

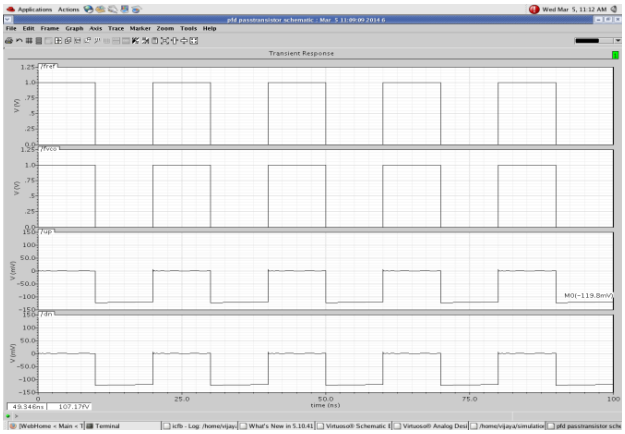

Fig 4. Output wave of PT-PFD with their inputs having same same duty cycle

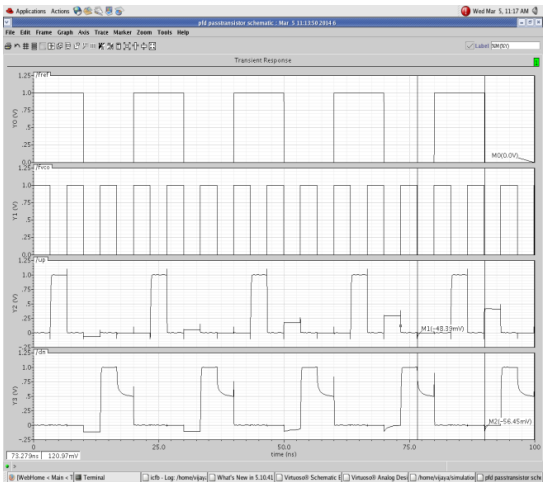

Fig 5.Output wave of PT-PFD with VCOclk frequency is 3times higher than REFclk frequency

After having look at the graph in Fig 4 and Fig 5,it is well understood that PFD functionality depends on the duty cycle. Fig 4 represents that the both inputs have 50% duty cycle, here there is no phase shift. From Fig 5 we can observe that the frequency of VCO is 3 times greater than frequency of reference signal, with inputs having different frequencies will introduce problem of phase shift and causes jitter, phase noise and dead zone on the circuit.

Fig 6 represents the phase noise and output noise of PT-PFD

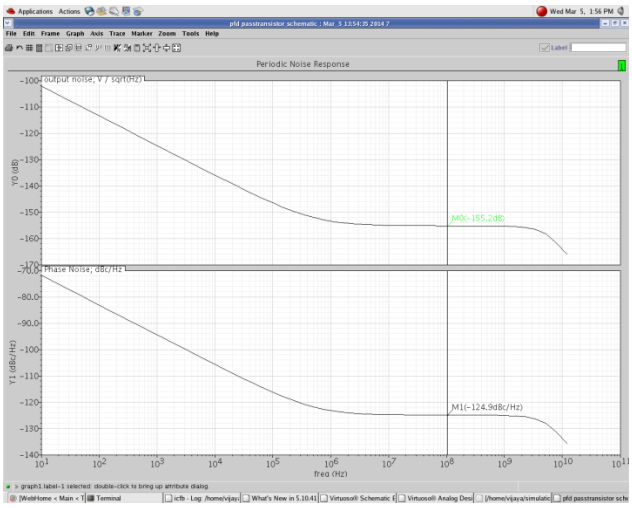

Fig 6. -126.9dBc/Hz is phase noise at 100MHz offset and -157.2dB output noise

Fig 7 Ploting graph between voltage Vs and time at 8GHz from Fig 8.

5.4 is the average power consumption of PT-PFD shown in Fig 9.PT-PFD finds application in low power, high speed and low jitter.

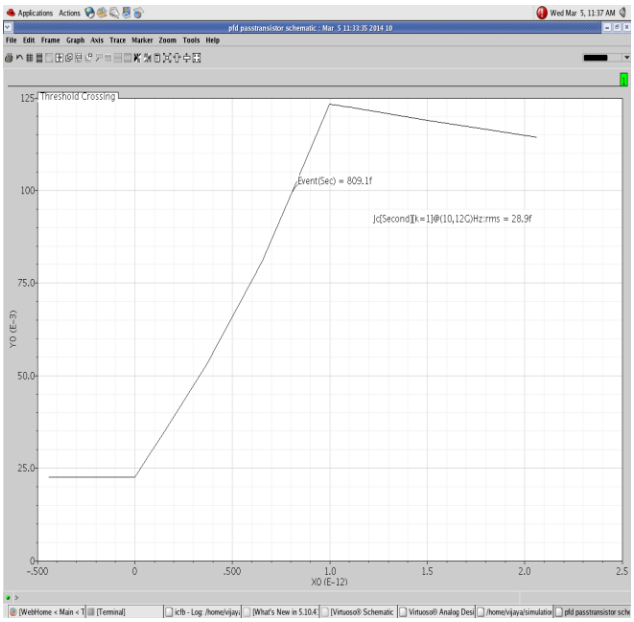

Fig 7.PT-PFD Jitter is 0.8ps at 8GHz

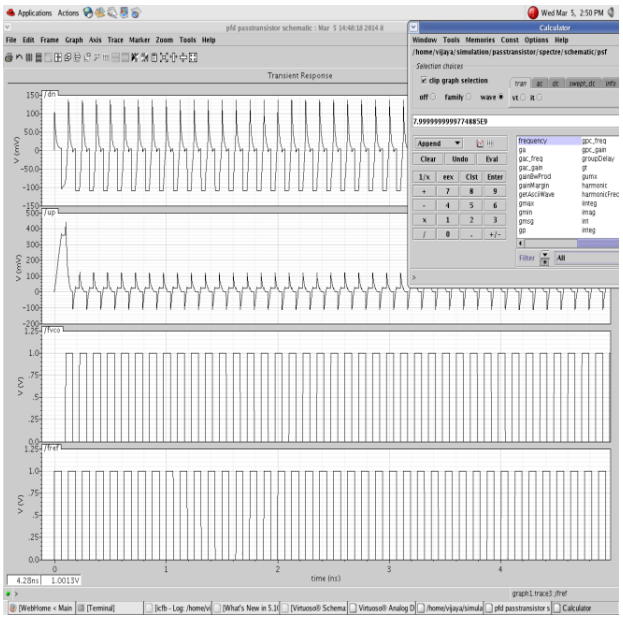

Fig 8.PT-PFD maximum operating frequency is 8GHz.

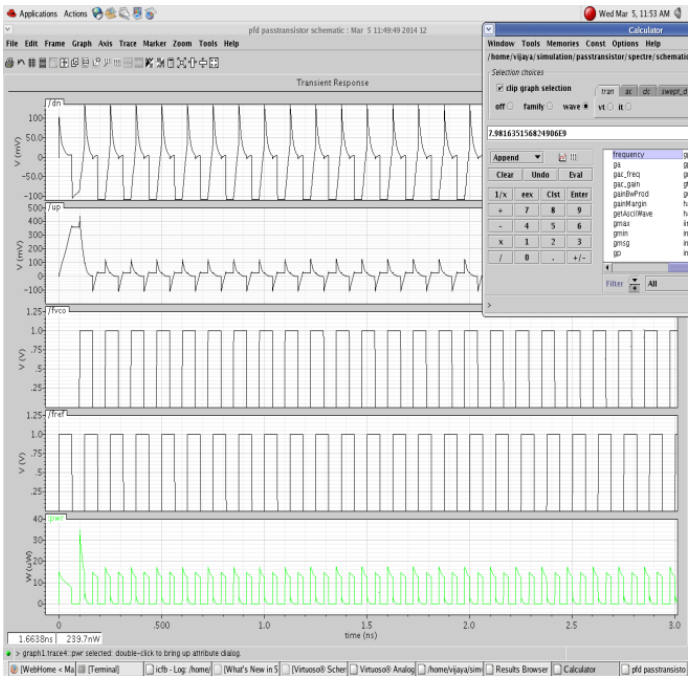

Fig 9.PT-PFD power consumption is 5.4µw

6. CONCLUSION

From the simulation results obtained, following conclusion are first, the circuit can successfully operates for the desired frequency range 8GHz with 0.8ps jitter. Second, results in low power consumption, low voltage utilization and with small area as it uses only 6 transistor in the circuit design .At 100MHz the output noise is -157.2Db and phase noise -126.9Db/Hz. The average power consumption 5.4µw.On observing all these performance parameters it is well understood that PT-PFD has an outstanding performance.

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