"Design of Process Variation Tolerant 3T1D-Based Cache Architectures Using VLSI Approach"

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***Abstract*— A Memory architecture using three-transistor, one-diode DRAM (3T1D) cells in The L1 data cache tolerates wide process variations with little performance Degradation, making it a promising choice for on-chip cache structures for Next-generation microprocessors. Process variations will greatly impact the stability, leakage power consumption, and performance of future microprocessors. These variations are especially detrimental to 6T SRAM (6-transistor static memory) structures and will become critical with continued technology scaling. In this paper, we study the working of DRAM on different technology for experiment we use .18µ, .13µ, .09µ. and find the conclusion regarding power variation, area required , and current. Because of increasing device-to-device mismatch and variation, however, stability, performance, and leakage power will become major hurdles for the continued scaling of traditional implemented in aggressive nanoscale technologies.**

***Keywords*—0.18micro, 0.13micro, 0.09micro, 3T1D DRAM,**

"1. Introduction"

In recent years, process variation has been identified as one of the key threats to continued Moore's Law scaling, with projections that a technology generation of performance can be lost due to process variations [5]. Also, there are serious concerns about the continue scalability of SRAM-based memories [3]. Several groups have propose solutions to patch stability issues due to process variations in memory designs that use 6T SRAM cells . Recently, researchers have begun to explore the system-level impact of variations on power, Performance, and reliability. Initial work in this area has focused on the modeling of process variations. Researchers have shown that the selection of pipeline depth [4] and other micro architectural parameters.

"2. About 3t1d dram"

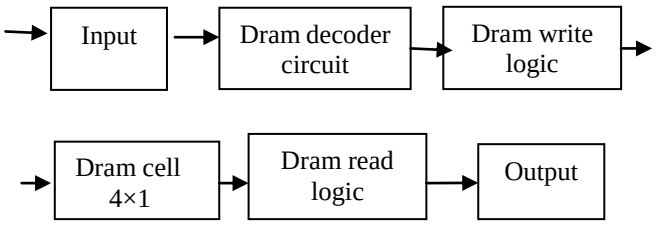

Fig. 1: Block diagram of Dram

Block diagram consist of above blocks DRAM decoder circuit is used to select the appropriate location which is followed by write logic to transfer the data then the main part of the circuit, that is DRAM cell which is actually responsible to hold the data , once it has been soared with the help of read logic we can read it. Lets we will concentrate on DRAN cell structure comparison with SRAM.

Recent circuit innovations in memory design provide an interesting alternative to 6T cells. Luk et al. proposed a novel 3T1D DRAM cell, which offers speed comparable to a 6T SRAM cell for a limited period of time after writing the data [18, 19]. Published results from chips fabricated in 130nm and 90nm technologies verify high-speed operation for dynamic 3T1D memories. In contrast, widely used 1T DRAM cells have slower access times and suffer from destructive reads. Hence, 3T1D cells are well-suited for latency-critical structures while 1T cells may be more appropriate for slower L2 caches. The proposed memory architecture in this paper can scale more effectively with technology under increasing process variations by employing intelligent data retention schemes for these dynamic memories.

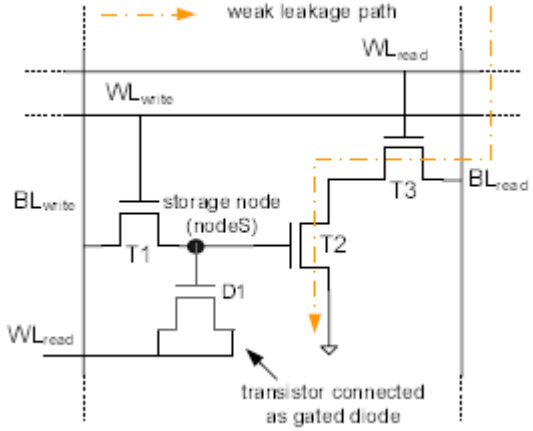

Fig 2: 3T1D DRAM cell design

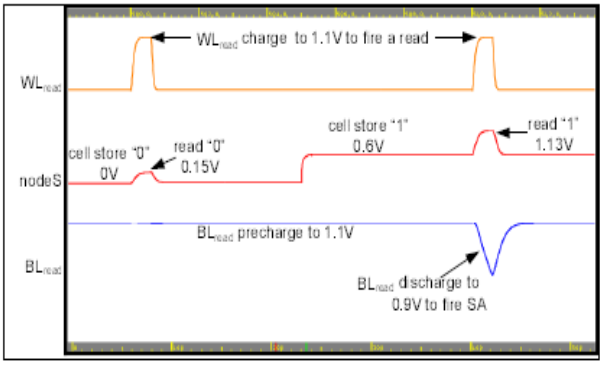

Fig 3: 3T1D DRAM cell operation

Figure 3 presents a schematic of the 3T1D (3-transistor, 1-diode) DRAM cell. Due to the threshold voltage of T1, there is a degraded level on the storage node when storing a "1". Hence, it relies on a "gated diode" (D1) to improve array access speed. This diode can be thought of as being a voltage-controlled capacitor with larger capacitance when storing a "1" and a smaller capacitance when storing a "0." Each time the cell is read, the bottom side of this capacitor is also raised to VDD. If the cell stores a "1" and it is read, the charge stored on the big capacitor of D1 boosts up the turn-on voltage of T2, rapidly discharging the bit line. As a result, the access speed can match the speed of 6T SRAM cells. Conversely, when a "0" is stored, the capacitance of D1 is smaller and there is almost no voltage boosting, which keeps T2 off during the read. Hspice simulation results, shown in Figure 3(b), illustrate the operation of the 3T1D cell. The gate voltage of T2 is boosted by about 1.5-2.5 times (1.13V) the originally stored voltage (0.6V) if a "1" is stored when being read.

Although the speed of a 3T1D cell can be fast, this high-speed access is only valid for a limited time period after each write to the cell. This is because the charge on D1 leaks away over time. Figure 4 shows the relationship traditionally, the word "retention time" is defined as the time a DRAM cell can no longer hold the stored value.
Here DRAM decoder circuit is used to select appropriate location of DRAM which consist of 6 NMOS devices which work with the help of driver circuit which again consist of 20 MOS devices, these are compact design which lead in to minimum area requirement. To load the data in to memory there is a write logic which consist of 24 MOS devices, and also read logic consist of same devices. In order to check the performance of circuit when technology is change we are using different technology and find the certain conclusion regarding power consumption, area requirement and current consumption . This section compares the speed, power, and area of the novel 3T1D DRAM to the traditional SRAM to demonstrate how the 3T1D DRAMs can be a suitable replacement for future on-chip memory designs.

1) Speed*:*
Generally speaking, SRAMs are believed to be faster than DRAMs. DRAMs are traditionally comprised of 1T1C (1-transistor, 1-capacitor) cells with emphasis placed on density at the expense of speed. Furthermore, the destructive read of a 1T1C cell requires a write back that immediately follows each read access. A 3T1C (3-transistor, 1-capacitor) DRAM cell does not suffer from destructive reads, obviating data write back after each read access. However, the speed of a 3T1C cell is slower than a 6T SRAM cell. In comparison, the novel 3T1D (3-transistor, 1-diode) DRAM cell replaces the capacitor with a gated diode to solve this speed problem. This diode can be thought of as being a voltage-controlled capacitor with higher capacitance when storing a "1" and a lower capacitance when storing a "0." Each time the cell is read, the bottom side of this capacitor is also raised to VDD. Hspice simulation results, shown in Figure 2b, illustrate the

operation of the 3T1D cell. By exploring the "amplification effect" of the diode [15], the voltage on the storage node is boosted by about 1.5-2.5 times the originally stored value if a "1" is stored when being read. Although the voltage on the storage node is only about 0.6V (degraded value), it is boosted to 1.13V when reading. This boosting strongly turns on the pull-down transistor (T2) and rapidly discharges the bitline.

2) Stability*:* The 3T1D DRAM cell does not suffer the cell stability issues previously seen in 6T SRAM cells, because there is no inherent fighting. Read operation occurs by simply discharging or charging the bitline, and write operation occurs by charging or discharging a dynamic storage node within the 3T1D cell. Except for the finite data retention time, a 3T1D DRAM cell is inherently stable.

3) Power*:* The 3T1D DRAM cell does not suffer the multitude of strong leakage paths previously seen in 6T SRAM cells. Hence, leakage power associated with 3T1Dbased memories can be much smaller. If there is a "0" stored in the cell, there is only one weak leakage path given two stacked off transistors, While a 3T1D cell saves dynamic power for writes, there is additional power during reads. The power overhead comes from the diode. If there is a memory read, the source voltage of the diode is raised, which consumes additional dynamic power.

4) Area: A 3T1D cell is much more area efficient compared to 6T SRAM cells, because the wire connection in a 3T1D cell is much simpler and there are no PMOS devices. This means the 3T1D cell can be smaller or, for the same area, the devices in a 3T1D cell can be larger to mitigate process variation. We emphasis here that most of the variation tolerance advantage of a 3T1D memory is not from the sized up devices, but by the ability to absorb retention time variation in the microarchitecture.

"3. Working of dram with different technology"

As in this paper we have given the complete realization of DRAM 4×1 cell so it consist of different circuits which consist of many transistor, in order to find the requirement of area as the technology is changing the table indicate the total PMOS and NMOS required, hence the total area required. As per experiment total area required in 0.18µ technology is 60.84 μm^2 .

Table 1: Analysis of DRAM with 0.18micro technology

Technology	Circuits	PMOS	Area (µm2)	NMOS	Area (µm)
0.18µ	Decoder	0	0	6	2.16
0.18µ	Decoder driver circuit	8	5.76	12	4.32
0.18µ	Write logic	12	8.64	12	4.32
0.18µ	DRAM cell (4×1)	0	0	16	17.28
0.18µ	Read logic	12	8.86	12	4.32
0.18µ	Buffer logic	2	3.6	2	1.8

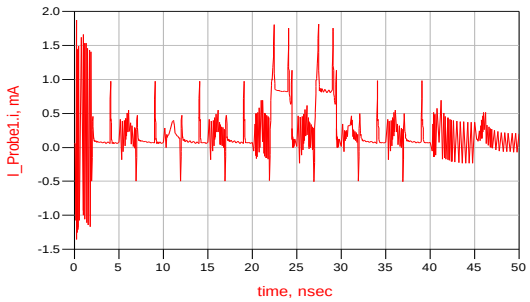

Fig 4: Current Output of DRAM with 0.18micro technology

For the power requirement of the same circuit we have to take the current in to consideration , the fig shows the current in 0.18µ technology from given fig the average current is 0.5mA hence power required is .5 mV.

Now similarly for the 0.13µ, and 0.09µ technology the Table and Table shows area requirement for respective technology, also fig and fig shows the current requirement

Table 2: Analysis of DRAM with 0.13micro technology

Technology	Circuits	PMOS	Area (µm2)	NMOS	Area (µm2)
0.13µ	Decoder	0	0	6	1.17
0.13µ	Decoder driver circuit	8	3.12	12	2.34
0.13µ	Write logic	12	4.68	12	2.34
0.13µ	DRAM cell (4×1)	0	0	16	8.84
0.13µ	Read logic	12	4.68	12	2.34
0.13µ	Buffer logic	2	1.82	2	0.91

Table 3: Analysis of DRAM with 0.09micro technology

Technology	Circuits	PMOS	Area (µm2)	NMOS	Area (µm2)
0.09µ	Decoder	0	0	6	1.08
0.09µ	Decoder driver circuit	8	2.88	12	2.16
0.09µ	Write logic	12	4.32	12	2.16
0.09µ	DRAM cell (4×1)	0	0	16	8.64
0.09µ	Read logic	12	4.32	12	2.16
0.09µ	Buffer logic	2	1.8	2	0.9

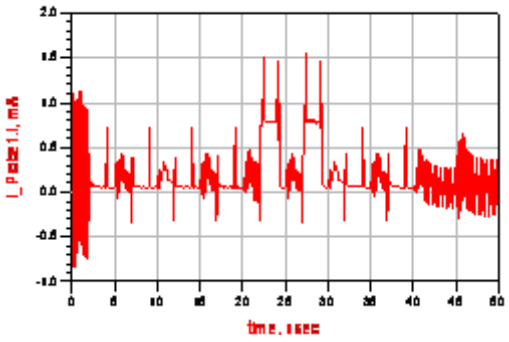

Fig 5: Current Output of DRAM with 0.18micro technology

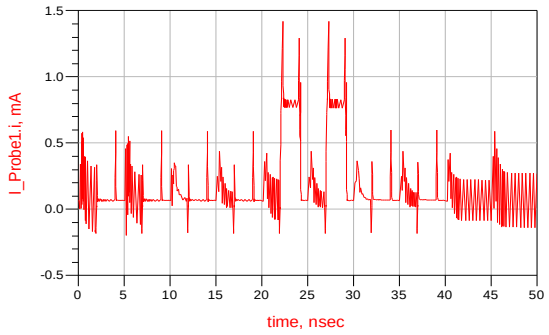

Fig 6: Current Output of DRAM with 0.09micro technology

From Table and Table total area required in 0.13µ and 0.0.09 µm technology are 32.24 µm2 and 30.42 µm2. From fig and fig current required in 0.13µ and 0.0.09 µm technology are 0.4mA and 0.3mA respectively, hence power required are 0.4mW and 0.3mW.

Conclusion

Microprocessors tolerant to process variations in future nanoscale technologies will be at the forefront of innovation for years to come. This paper proposes novel process variation tolerant on-chip memory architectures based on a 3T1D dynamic memory cell. The 3T1D DRAM cell is an attractive alternative to conventional 6T cells for next-generation on-chip memory designs since they offer better tolerance to process variations that impact performance, cell stability, and leakage power. Also it is conclude that when technology reduces the area and power also reduces .

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