International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 8, August - 2013

Design Of S/H And Coarse ADC For 6 Bit100mhz Folding ADC

Vishnu D
Asst.Professor Dept.of Electronics and Communication Engg, Younus college of Engg and tech ,Kollam,Kerala,India.

***Abstract*- This thesis describes the design of SAMPLE AND HOLD and COARSEADC for 6 bit 100MHz folding A/D converter in CMOS technology. This A/D converter is derived from ash A/D converter and has many advantages over ash A/D converter. The advantage of folding A/D converters is that the reduced number of comparators for analog to digital conversion which in turn reduces the complexity of the circuit, the total power consumption of the circuit and input capacitance of the circuit. This is achieved by making use of an analog preprocessing circuit called as the folding circuit. In folding ADC the entire bits is divided into Coarse bits and Fine bits. Coarse bits is generated by ash ADC and we are placing Sample and Hold at the front end to reduce errors. Folding A/D converter is widely used in high speed signal processing such as digitalization of video signals. In this thesis detailed design of positive feedback fully differential comparator for ADC and two stage telescopic op amp based sample and hold is given. All the simulations are done in Cadence Virtuoso Analog Design Environment using TSMC 90nmtechnology.**

I. INTRODUCTION

Digital signal processing (DSP) plays a very important role in modern technology. In digital signal processing ADCs and DACs plays very important role. Most of the signals existing in nature are analog in nature it has to be converted to digital before using in a digital system and similarly aback transformation is also needed in many cases. Thus the need for an interfacing circuit between the analog world and digital world is necessary. The integration of analog and digital(mixed signals)systems on a single chip leading to the demand of data converters, such as Analog-to-Digital Converters(ADC) and Digital-to-Analog Converters (DAC). ADCs and its application in communication field, medical field etc. Flash ADC, Folding ADC, Pipelined ADCs , SAR ADC are some of the commonly used ADCs. Now a days researches are going on for developing new ADC with greater resolution, speed and less power consumption.

II. FOLDING A/D CONVERTER

In folding A/D converter we are dividing the entire bits into coarse bits and fine bits coarse bits corresponds to the MSB and fine bits corresponds to the LSB. Coarse bits are generated by flash A/D converter and fine bits by fine flash

converter whose input is the residue generated by analog pre processing circuit called the folding circuit. The basic block diagram of folding A/D converter is shown in Fig.1

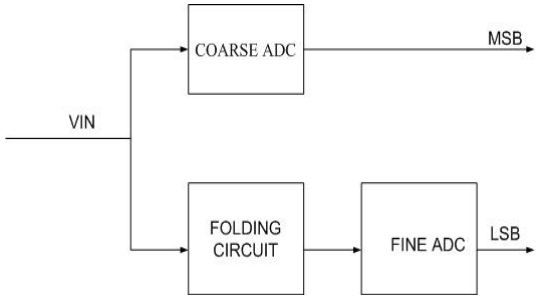


Fig.1.Block diagram of folding ADC.

Signal Folding - Folding means how many times the output goes from minimum to maximum, when the input changes from minimum to maximum once. The output change is determined by the folding factor. Folding factor defines how many times the output change when the input changes from minimum to maximum once. Folding factor 'n' means the output changes 'n' times when the input changes from minimum to maximum once.

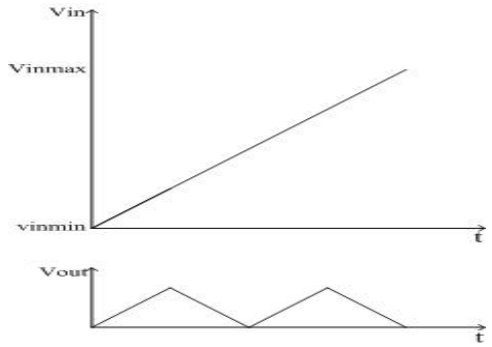


Fig.2. The folding output for folding factor four

From Fig.2 we can see that, as input goes from minimum to maximum once the output changes from minimum to maximum and maximum to minimum four times. So the folding factor is four. An N-bit folding ADC operates in a similar manner to a two-step ADC by quantizing the incoming signal through a coarse quantizer flash ADC and by generating a residue signal which is further quantized by a fine quantizer flash ADC . Coarse ADC converts the analog input to MSB bits and the LSB bits are generated using _ne ADC. The analog preprocessing circuit converts a full scale range and divides it into sub-ranges, the number of sub-ranges is defined as folding factor. Fine ADC converts this

sub-range into LSB bits. The residue signal is generated by an analog folding block which reduces the dynamic range of the input signal by the folding factor F, thus resulting in the reduced number of comparators. The coarse quantizer generates M bits while the fine quantizer generates the remaining (N-M) bits. The (N-M) bits fine ADC require 2^n/ F comparators.

III. SAMPLE AND HOLD

The Sample and Hold circuit is a main part of most discrete-time systems such as ADCs. In many cases, use of an S/H (at the front of the data converter) can greatly minimize errors due to slightly different delay times in the internal operation of the converter

A. Need for S/H

If we are directly feeding an analog signal to an ADC, the ADC cannot make correct decision because the analog input is changing the value instantaneously, so we are sampling the value of an analog input and holding the value for sometime so that ADC get enough time to take decision. For this we are making use of sample and hold circuitry.

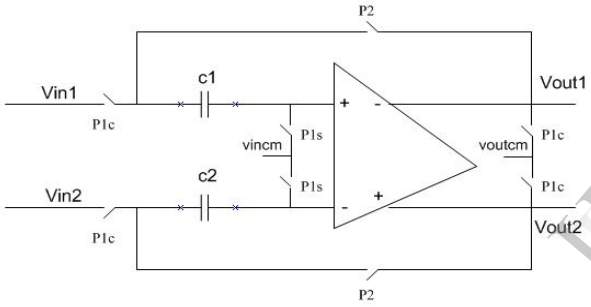


Fig.3.: Sample and Hold Circuit

Here we are providing two common modes, input common mode and output common mode. During the sample mode the switches p_{1c} and p_{1s} gets closed and switch p_2 is opened and the capacitors c_1 and c_2 gets charged to V_{in} - Vi_{ncm}. During the hold mode the switches p_{1c} and p_{1s} gets opened and switch p_2 gets closed. During this time the output gets charged to V_{outcm}- (V_{in}-V_{incm}).

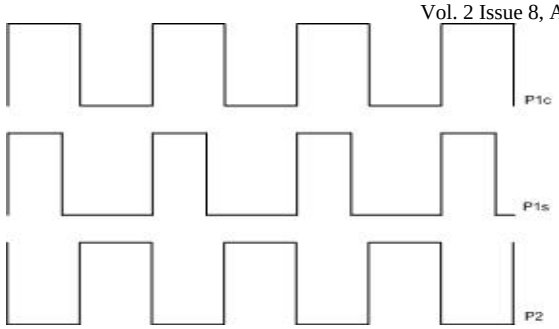


Fig .4 Clock for sample and hold

From Fig. 4 during the sample phase the switches p_{1c} and p_{1s} gets closed at the same time. During the hold phase p_{1s} gets opened earlier in order to avoid charge injection. That is during the starting of hold mode there is a chance that a charge packet will move from input to the capacitor and causes a change in the stored charge. But if the switch p_{1s} opens earlier there is no path for the capacitor to get charge so charge injection effect can be avoided.

Sampling Frequency = 100MHz Clock period = 1/100MHz = 10nsec, i.e., 10ns is available for sampling and holding operation.

B. Factors which affect the performance of the S/H circuit

i. Sampling pedestal (hold step)

This error occurs when the circuit switches from sample mode to the hold mode. During this change in operation, there is always a change in voltage being held that makes it different from the input voltage at the time of sampling. It is important to know that this error must be independent from input signal. This error may cause nonlinear distortion

ii. Slew Rate and 3db bandwidth

The speed at which a sample and hold can track an input signal in sample mode. This parameter is limited by the slew rate and the 3db bandwidth in both small signals and large signals. It is necessary to maximize SR and 3db bandwidth for high speed performance.

ii. Aperture jitter (aperture uncertainty)

This error is the result of effective sampling time changing from one sampling instance to the next and becomes more pronounced for high speed signals. Specifically, when high speed signals are being sampled, the input signal changes rapidly, resulting in small amounts of aperture uncertainty causing the held voltage to be significantly different from the ideal held voltage.

iv. Droop rate

This error is a slow change in output voltage when in hold mode, caused by effects such as leakage current due to the finite base currents of bipolar transistors and reverse biased junction. In CMOS design, droop rate is small and can be ignored. There are also other factors such as dynamic range, linearity, gain, noise and offset error which affect the performance of S/H circuit.

C. Design Issues In CMOS S/H

Some of the design issues in CMOS sample and hold is listed below.

1. Sampling Moment Distortion

Finite Clock rising/falling time results in distortion
$\Delta ts = 2a / V_{clock} \times t_{rise}$

2. Clock Feed-through

Overlap capacitance of MOS Switch creates a sampling error during clock transition time.

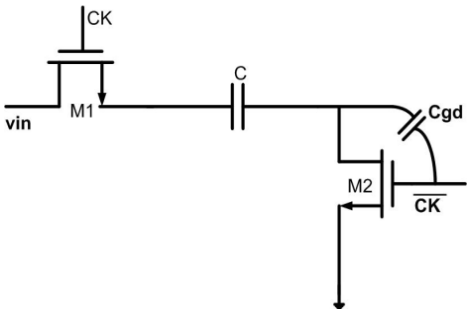


Fig.5 Clock Feedthrough

3. MOS Switch Charge Injection

Some charge in the MOS channel ow to Source and Drain that results in an error.

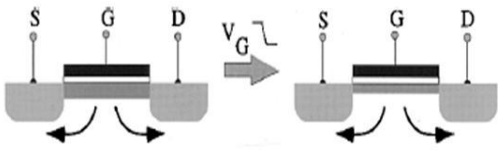


Fig.6 MOS Switch Charge Injection

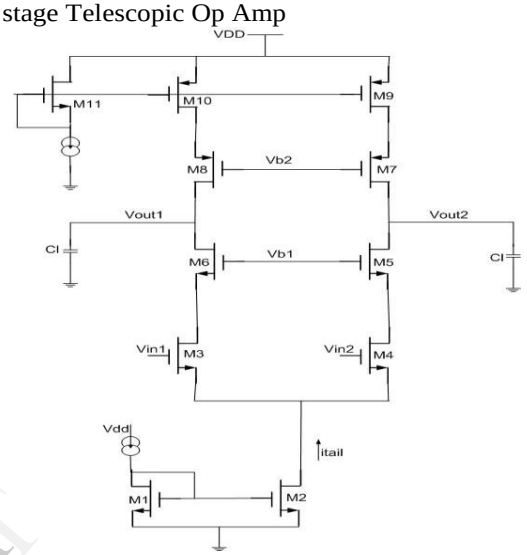
D. OP AMPS

For choosing the appropriate architecture for op amp, one should first notice the requirements of the system. For S/H the op amp gain should be high. For getting high gain two stage Op Amp is selected. In two stage op amps, the first stage provides a high gain but the output swing is small. So we went for second stage, and the second stage gives largen swing.

For the first stage of the two stage opamp fully differential telescopic op amp is selected. This provides high gain because its Rout is high, so Gain = Gm ×Rout is high, and the second stage is configured as common source stage so as to allow maximum output swing.

E. Design Procedure

1 First stage Telescopic Op Amp



Power(P) = 5mW, Vdd(V) = 1.2V P=V×I ie,I = P/V ie, 5mW/1.2V =4mA ie, tail current is 4mA

Required swing at each output node is .15V
A marginal value of 50mV is applied to each transistor on each side, 50mV×5= .25V
Total voltage available for V_{dsat}
1.2-0.15-.25 = .8V = 800mV
$V_{dsatM9} + V_{dsatM7} + V_{dsatM5} + V_{dsatM4} + V_{dsatM2} = 800mV$
$V_{dsatM2} = 200mV$
$V_{dsatofpmos} = 2\times V_{dsatofnmos}$
So, $2\times V_{dsatM4} + 2\times V_{dsatM5} + V_{dsatM5} + V_{dsatM4} = 600mV$
$6\times V_{dsat} = 600mV$

Therefore $V_{dsat} = 100mV$ for nmos
For pmos $V_{dsat} = 2\times V_{dsat}$ of nmos = 200

From this, we can calculate the bias voltages, width and the length of transistors so that each transistor operates in saturation region. The Width and length is calculated with the help of current equation in saturation region.

$$I_D = 1/2\mu nCoxW/L(V_{GS}-V_{TH})^2$$

2 Two stage Op Amp without compensation

The disadvantage of telescopic op amp is that the low voltage swing because five overdrive voltages have to be subtracted from the power supply voltage. So common source

amplifier is added at the output of the first stage to obtain high swing . The transistors are properly biased to work in saturation and the output common mode is set at 600mV to obtain the maximum swing.

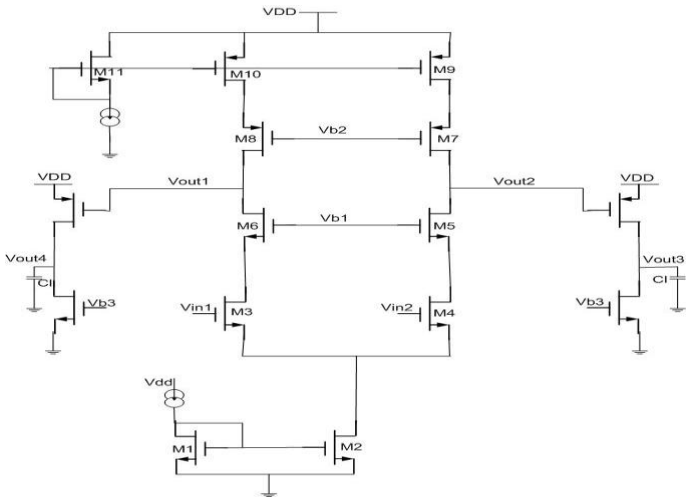


Fig.7. Two stage opamp without compensation

F. Miller Compensation and CMFB

Miller compensation with series resistance is used to eliminate zero. The value of the resistance is equal to 1=gm of the input transistor (M12 or M13)

Value of resistane = 300
Value of capacitance = 4Pf

This is done to improve the phase margin and newely obtained phase margin is 62.1265. The phase margin above 60 will reduce the overshoot considerably

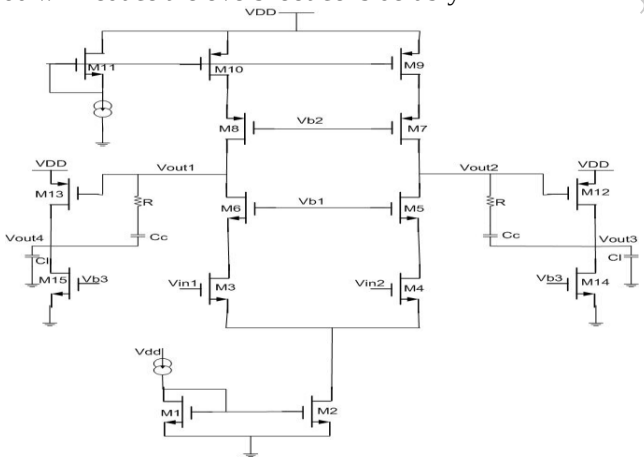


Fig.8 Second stage with compensation

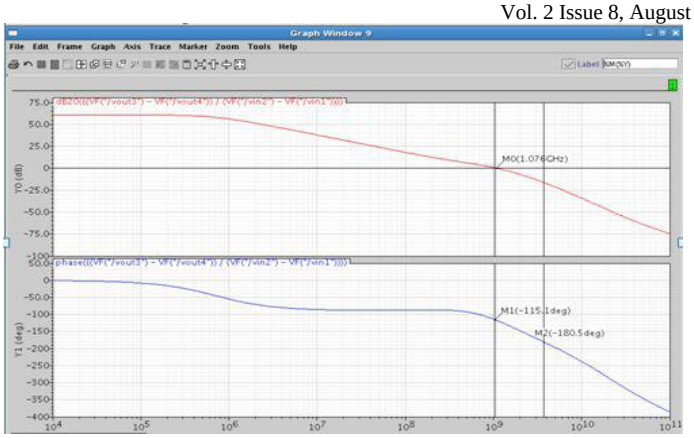


Fig.9 Cadence simulation result after compensation and CMFB

From Fig.9, gain crossover frequency (GX) lies inside the phase cross over frequency (PX), i.e., we get a stable response.
Total gain of the op amp is 61.021dB
Phase Margin is 60.37
Unity gain bandwidth is 1.0718GH

D. Design of DMP

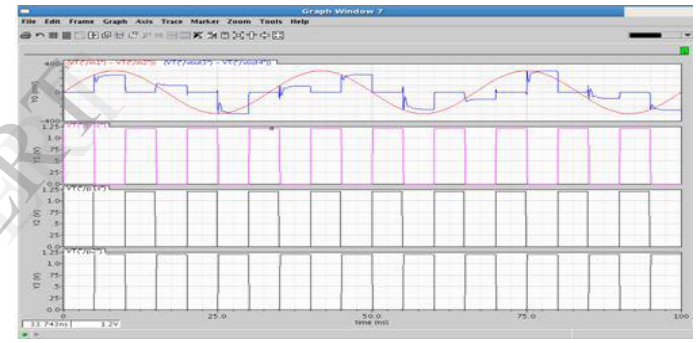


Fig.10 Cadence Simulation result of sample and

IV. COARSE ADC SIMULATION RESULTS

We are using coarse ADC for generating the 2 MSB bits. For 2 bit generation we need 3 comparators. The sample and hold output is the input to the differential comparator of the coarse ADC. Since the comparator used is differential a differential ladder is required for generating the reference voltages. The reference voltages are generated using a reference ladder consisting of 4 resistors. The references V_{r1}, V_{r2}, V_{r3} are used as the references for the comparators. V1 and V_2 are the output swings of the sample and hold output. C_0 C_1 and C_2 are the comparator outputs. This thermometer code is converted to 2 bit binary code using a decoder.

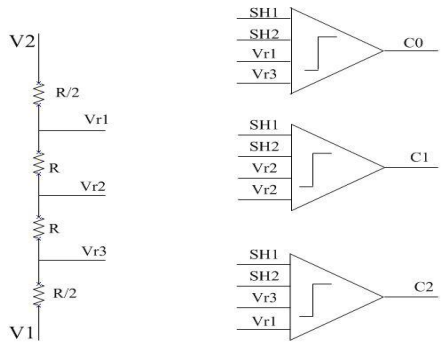


Fig.11 Schematic of Coarse ADC

In Fig.11 three reference values are generated using an R-2R ladder .Maximum and minimum values of the reference ladder is V_1 and V_2. These values is obtained from the swing of the Sample and Hold circuit. In ourdesign the Sample and Hold is designed for a swing of 350mV-750mV, soV_1 will be 350mV and V_2 will be 750mV and an R-2R resistor ladder derives 3 reference voltages in this range. This reference voltages are the reference voltages of the comparator. Comparator used is a differential comparator with inputs as differential reference voltages and differential output of the Sample and Hold. At any instant if the value of the reference is larger than the output from sample and hold for a particular comparator that comparator outputs a logic low value. Similarly if the value of the reference is smaller output from sample and hold for a particular comparator that comparator outputs a logic high value.

The output of the comparator is a thermometer code. It has to be converted to binary. We are converting the thermometer code to binary by making use of 3-2 compressor. A 3-2 compressor is basically a full adder. The equations of a full adder are shown as follows:

S = (a xor b xor c) (1)
C =(ab + bc + ac) (2)

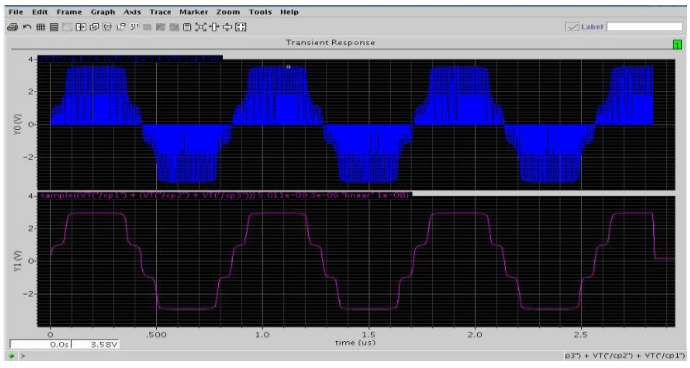


Fig.12 Cadence simulation result of Coarse ADC when a sine wave is given at the input of sample and hold and the result shows the Coarse ADC is resolving 2 bits.

V. FOLDING AND FINE ADC

Fine bits are generated by fine ADC preceded by a folding circuit. The folding circuit folds the input signal based on the folding factor. The output obtained is a residue which is fed to the fine flash ADC, which generates the fine bits.

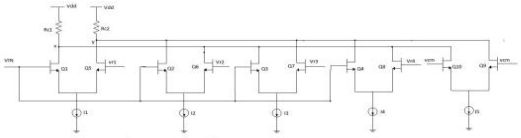


Fig.13 Folding circuit for folding factor 4

FINE ADC-The output of the folding circuit is fed to the fine ADC and the fine ADC resolves the LSB. The references of the fine ADC is generated on the basis of the output swing of the folding circuit. For this we have given a ramp input and the output swing is calculated. The V_{Max} and V_{Min} represent the maximum and minimum values of the reference ladder for the fine ADC labelled as V_{out1} and V_{out2} in the schematic.

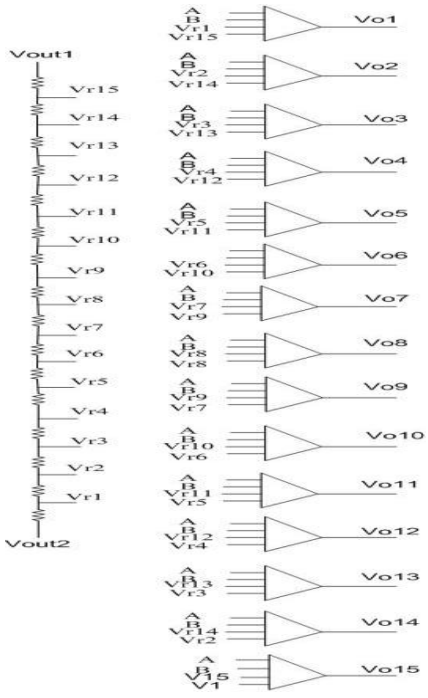


Fig.13: Fine Schematic.

In fine ADC we are resolving 4 bits. That means we need 15 comparators as shown in Fig.13. The inputs to the comparator are the outputs fromthe folding circuit marked as A and B which is compared with the referencevoltages generated by the reference ladder. Here, an R-2R ladder is used togenerate the reference voltages. If the value of A and B is greater than thevalue of reference voltage of a comparator then that comparator produces aone at the output. The reverse will happen if the reference value is greaterthan the value of input. The output of comparator is a thermometer code which is converted to binary using a decoder circuit.3

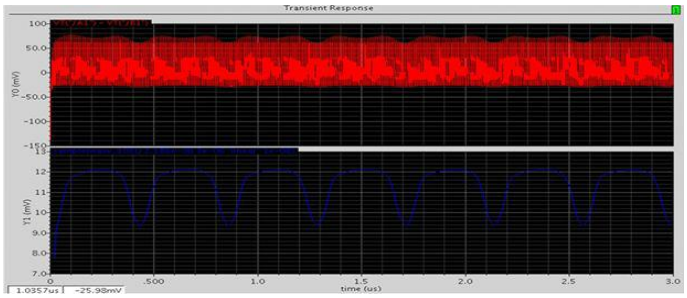


Fig.14 Folding output with sample and hold

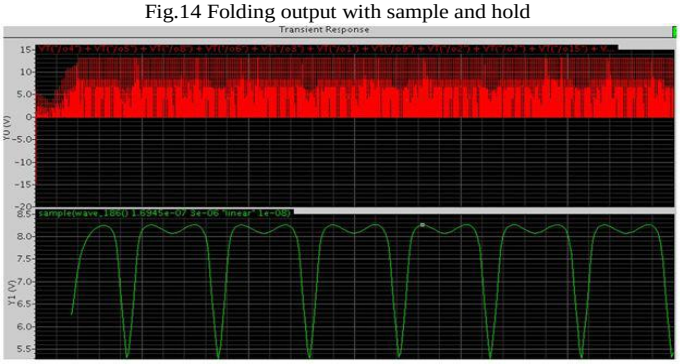


Fig 15. Fine output with sample and hold

The output of the folding circuit is shown in the Fig.14. This output is obtained when the input of the folding circuit is the output of sample and hold. The folding output is fed to fine comparators and where it is compared with the reference voltages generated by the resistor ladder. Each comparator produces a one at the output if the input is greater than the reference level of the comparator. Fig.14. is the output of folding circuit and Fig.15 is the output of the fine ADC. These comparator output follows the input two graphs are identical because comparator output follows the input.

V1.CONCLUSION

The S/H and Coarse ADC are designed for a 6 bit 100 MHz Folding ADC. Sample and Hold is designed using two stage telescopic opamp, first stage provides the gain and second stage provides the required swing. Miller compensation and common mode feedback is done for stabilizing the output of opamp. S/H circuitry is designed in such a manner that the effect of charge injection and clock feed through is minimized. Coarse ADC is designed to resolve the MSB bits . Here we are considering two bits for MSB. Coarse ADC is designed using positive feedback fully differential comparator with neutralization technique for clock feed through. The coarse ADC part is integrated with the fine ADC part which resolve the LSB bits. Fine ADC part consists of analog preprocessing unit called the folding block which is basically cross coupled differential pair. Folding block generates a residue which is the folded version of the input signal. This residue is fed to the _ne flash ADC and it resolves the LSB bits.

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