Design of Single Stage Single Switch Improved Power Quality AC-DC converter

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***Abstract* –AC-DC converter are increasingly used in application such as UPS, battery Charger and in application where size, weight and cost are major concern. Since the power converters draw pulsed current from the utility line current harmonics are injected to the electrical network. Power quality is an issue that is becoming important to electricity consumers at all level of usage. Sensitive equipment and non-linear loads are common place in both industrial and domestic environment. Harmonic distortion can result in malfunction of sensitive equipment and generators. Power factor corrected convertor is increasingly usedin industry to improve input current quality and regulate the output voltage of front end convertor.This paper presents a Single Stage Single Switch Power Factor Corrected Converter. This converter achieves power factor correction and regulates output voltage by using only one switch. In this paper a design solution is presented to avoid the DC bus voltage stress at light load by suitable selection of boost inductor using Equal Area Criterion (EAC).**

Simulation studies done using ORCADsoftware and actual test results are compared and analyzed. The input current waveform is found to be sinusoidal and in phase with input voltage, the voltage stress is quiet insignificant.DC bus voltage stress during light load condition is observed. Under closed loop condition the stress was found almost eliminated.

I. INTRODUCTION

Requirement and stipulations specified by IEEE 519 and IEC 61000-3-2 with respect to low harmonic distortion and high input power factor aroused interest in active current wave shaping technique. Therefore, a power factor correction stage has to be inserted to the existing equipment to achieve a good power factor. There are other reasons for wanting to limit harmonic currents, these include being able to use the full rated current from the available power source. THD is the ratio of harmonic current to the fundamental component. Power factor and THD are related by

$$\text{p.f}=\sqrt{\frac{1}{1+(THD)^2}}$$

The goal then of a PFC convertor is to reduce the harmonic content of the current waveform and keep the phase angle between the current and the voltage as small as possible. In effect the circuit wants to emulate the resistive load.

The new family of power factor corrected switching power supplies normally consists of two stages in the power circuit, viz. – The input power factor correction stage and the output DC to DC converter stage. Continuous efforts to further make these power converters compact and cost effective too lead to the development of new class of power supplies known as Single Stage Single Switch Switch Mode Rectifier, which is the integration of PFC stage and the DC to DC converter stage. It uses only one switch and controller to shape the input current and regulate the output voltage.The energy storage device in between is necessary to absorb and supply the difference between the pulsating instantaneous input power and constant output power [1].

A major problem associated with Single Stage Single Switch power factor converter is strong dependency of DC bus voltage stress across the capacitor with the output load [1], [2]. Power unbalance between PFC stage and DC-DC stage is the inherent reason for causing high DC bus voltage stress. Frequency control is other solution proposed to overcome high DC voltage stress [13]. But this call for complex control circuit.The concept of series charging, parallel discharging capacitor schemeis another solution.[14].But this call for more component count in the power circuit. Another approach to this problem is by modulating the predetermined operating frequency of the converter[15] increased complexity in the control circuit.

In this paper a design solution is proposed based on application of equal area criterion (EAC) to the discontinuous current operation [5]. This paper gives a method to avoid the problem of energy unbalance between energy stored during on period of switch and energy dissipated in the load by optimally sizing the boost inductor. Maximum energy stored in the inductor shall be limited to such a value that this energy matches with maximum output power required. The instant at which maximum power delivered shall be matched with the instant when the input ac voltage is at the peak. Also consider the fact that maximum power is delivered at a duty ratio which is slightly less than the limiting duty ratio (0.5) for DCM operation.Equal Area Criterion is applied between theoretically calculated fundamental component of input ac current and the peak inductor current when $t_{on}$is maximum. Using this approach the design was carried out, and simulated testing as well as experimental observation showed only a very small rise in DC bus voltage at light load condition, even under open loop. After introducing closed loop control with output voltage as controlled variable and duty ratio as manipulated variable the DC bus voltage stress was found almost insignificant.

II.THE BIFRED CONVERTER

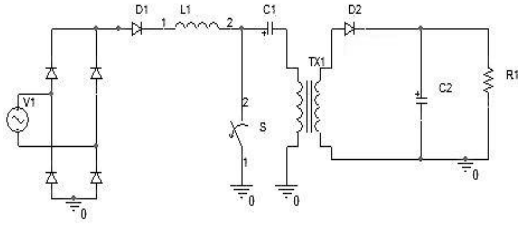

Figure 1. The BIFRED PFC ac/dc converter

One of the basic configurations of single stage single switch SMR is the BIFRED converter which is the acronym for Boost Integrated with Fly Back Rectifier / Energy storage / DC- DC converters which is shown in Fig.1.It integrates a DCM boost converter with dc-dc converter. DCM boost HQR is chosen here as the converter which draws energy at line frequencies due to its inherently law line current harmonics. Continuous current mode Fly back converter can provide wide bandwidth response. Two elements are common in the design of single stage single switch switched mode rectifier. First, the mode of input inductor must be maintained such that input inductor begins and ends each switch cycle at a ground state. Second, the converter must have an energy storage capacitor which is capable of providing energy when the instantaneous line voltage is near zero.

When S is turned on, rectified line input voltage appears across the boost inductor and the output magnetizing inductor stores their energy independently during the on interval of the switch. When the switch is turned off, the stored energies are delivered to the bulk capacitor and to the load.

Under light load condition the PFC stage without realizing this, stores the same energy as that of the heavy load leading to an unbalanced power between the input and the output [1]. This unbalanced power gets stored across the bulk capacitor causing the dc- bus voltage to increase. One way to take care of this problem is through closed loop control which will automatically reduces the on duration of the switch by sensing the output voltage thus by striking a power balance. But thedynamic response of the system being poor this methodis found not so attractive [2].

III.PFC CONVERTER WITH DC BUS VOLTAGE FEEDBACK

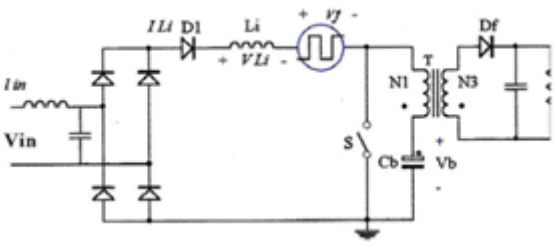

Figure 2.Converter with power stage negative feedback

An alternative method was proposed to use a negative feed back scheme in the power stage instead of in the control loop [2]. Fig 2 shows this scheme.A negative feedback voltage$V_f$is obtained by using a feed back winding coupled with the isolation transformer. This will make the resultant voltage available across boost inductor less when the DC-bus voltage increases, thus putting limit on to the input power drawn and by striking a power balance.

IV. THE PROPOSED SINGLE STAGE SINGLE SWITCH PFC CONVERTER.

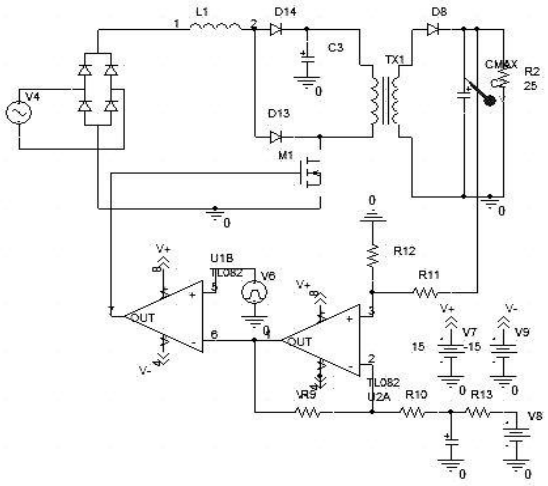

Figure 3. The Proposed Single Stage Single Switch PFC converter

Proposed converter, shown in Fig. 3, is a modified BIFRED converter, which avoids the use of*D*1and thenegative voltage feedback V_f. Equal area criterion(EAC) is applied to achieve optimum design ofboost inductor, coupled with a closed loop control withoutput dc voltage as controlled variable and duty ratio asmanipulated variable so as to eliminate the problem of dc bus voltage stress at light load. To fully explain the circuit, converter operation will be analysed according to the three operational stages.

Stage I.

This stage starts when the switch turns on , causing the current in inductor L1, to ramp up from 0 with a slope, which is proportional to the instantaneous line voltage. Diode D1 is reverse biased. At the end of this interval the amount of energy is stored in L1 which depends only on input line voltage and is independent of the current and voltages of other inductors and capacitors.

Stage II.

This stage starts when S turns OFF, which causes the current in inductor L1, to ramp down with a slope proportional to the instantaneous line voltage minus the energy storage capacitor voltage minus the output voltage reflected to the primary. Diode D1 conducts.

Stage III.

This mode starts when the current in inductor L1 reaches zero. Switch remains off, diode D1 conducts. During this mode, the potential energy level of L1 and C1 remains unchanged. Capacitor C2 and the load receive energy from the coupled inductor L2, and C2 passes energy to the load.

V. DESIGN OF PFC STAGE BY EQUAL AREA CRITERION.

The rectifier input current is discontinuous in nature. A typical input current pulse superimposed on the reference currentI_mSinωt, is shown in Fig. 4.

EAC applied to single stage single switch power factor converter means equalizing the areaunder a sinusoidal reference current and the area underthe input current in the total period of one switchingcycle [4].

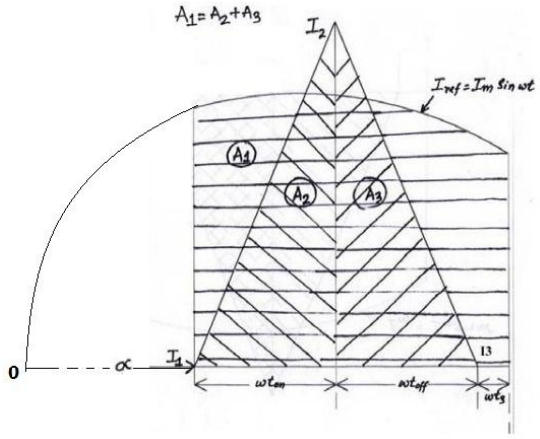

Figure 4. Input current pulse superimposed on reference current.

$T = t_{0n} + t_{off} + t_3$

ω_{ton}- On period of boost switch.

ω_{toff}- Off period of boost switch.

ω_{t3} - Non-conducting period (dead period).

α - Instantaneous switching angle

A.*EAC applied to design of boost inductor for the proposed single stage single switchpower factor converter*

Magnitude of the reference current is selected such a way that-

$$P_{out} = V_{rms} \times I_{rms \cdot ref \cdot}$$

Instantaneous current $i_r$in on mode of boost switch is,

$$i_r = I_1 + \frac{E_m}{\omega L_1} [\cos\alpha - \cos(\alpha + \omega t)] \quad (1)$$

Where $\alpha < \omega t < \omega t_{on}$

i_r in off mode,

$$i_r = I_2 + \frac{E_m}{\omega L_1} (\cos\alpha + \omega t_{on}) - \cos(\alpha + \omega t_{on} + \omega t) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t \quad (2)$$

At the beginning $I_1 = 0$

During on time, $i_r = \frac{E_m}{\omega L_1}[\cos\alpha - \cos(\alpha + \omega t)]$

Where $\alpha < \omega t < \omega t_{on}$ (3)

Off mode current becomes zero at $\omega t = \omega t_{off}$

$$I_3 = I_2 + \frac{E_m}{\omega L_1}[\cos(\alpha + \omega t_{on}) - \cos(\alpha + \omega t_{on} + \omega t)] - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t$$

Where $\alpha < \omega t < \omega t_{off}$ (4)

B. Design of Boost Inductor.

At the end of on duration I_2 is maximum (I_{2peak}).

I_{2peak} occurs at $\alpha = 90^\circ$ and duty cycle is maximum. The off duration followed by this I_{2peak} will be minimum.

Value of L has to be selected in such a way that current at the end of this minimum off duration is zero.

From (3)

$$I_{2peak} = \frac{E_m}{\omega L_1} \sin\omega t_{on} \quad (5)$$

$\sin\omega t_{on} \cong \omega t_{on}$ since switching frequency is high.

$$I_{2peak} = \frac{E_m}{\omega L_1} \omega t_{on} = \frac{E_m}{L_1} t_{on} = \frac{E_m}{L_1} DT \quad (6)$$

$$L_1 = \frac{E_m}{I_{2peak}} DT \text{ Where } D \text{ is duty cycle} \quad (7)$$

C. *DC bus voltage, output voltage and Duty ratio.*

From (4), (5) with I_3 =0 and assuming $\omega t_3 \cong 0$

$$0 = I_{2peak} + \frac{E_m}{\omega L_1}(-\sin\omega t_{on} + \sin\omega t_{on} + \omega t_{off}) - \frac{(V_{dc} + nV_2)}{\omega L_1}\omega t_{off} \quad (8)$$

$$0 = \frac{E_m}{\omega L_1}(\sin\omega t_{on} - \sin\omega t_{on}) + \frac{E_m}{\omega L_1}\sin(\omega t_{on} + \omega t_{off}) - \frac{(V_{dc} + nV_2)}{\omega L_1}\omega t_{off} \quad (9)$$

$$\frac{(V_{dc} + nV_2)}{L_1}t_{off} = \frac{E_m}{L_1}(t_{on} + t_{off}) \quad (10)$$

$$(V_{dc} + nV_2)(t - t_{on}) = E_m T \quad (11)$$

$$(V_{dc} + nV_2)t - (V_{dc} + nV_2)t_{on} = E_m T \quad (12)$$

$$\frac{t_{on}}{T} = \frac{(V_{dc} + nV_2 - E_m)}{(V_{dc} + nV_2)} \quad (13)$$

$$D = 1 - \frac{E_m}{(V_{dc} + nV_2)} \quad (14)$$

$$V_{dc} + nV_2 = \frac{E_m}{1 - D} \quad (15)$$

VI.DESIGN OF OUTPUT CONVERTER STAGE[8].

A.*Voltage transfer function for fly back converter.*

Always volt second balance should be there.

Primary Volt sec/turn= Sec volt sec/turn.

$$(V_1 - V_{swic})\frac{DT}{N_1} = \frac{(V_2 - V_d)(1-D)T}{N_2} \quad (16)$$

$$V_2 = V_1\frac{N_2 D}{N_1(1-D)} \quad (17)$$

B. *Voltage Transfer function of single stage single switch power factor converter*

We can write output voltage V_2 as

$$V_2 = (\frac{E_m}{1-D} - nV_2)\frac{1}{n}\frac{D}{(1-D)} \quad (18)$$

$$V_2 = \frac{E_m D}{n(1-D)} \quad (19)$$

C. *Design of fly back converter.*

For Volt second transformer balance

$$(V_1 - V_{sat})D = n(V_2 + V_f)(1-D) \quad (20)$$

At critical inductance L_c , the peak inductor current is twice the average.

$$I_p = 2I_L = \frac{V_{L_2}T_{on}}{L_C} \quad (21)$$

$$I_p = \frac{V_{L_2}D}{f_s L_C} \quad (22)$$

$$I_p f_s L_C = V_{L_2} D \quad (23)$$

we have

$$i_{2(avg)} = \frac{nI_P(1-D)}{2} = \frac{V_2}{R} \quad (24)$$

$$I_P = \frac{2V_2}{R(1-D)n} \quad (25)$$

from (21), (25)

$$L_C = \frac{(V_2 + V_f)R(1-D)^2 n^2}{2V_2 f_s} \quad (26)$$

VII. DESIGN OF A 100 WATT, 230 V, 50 HZ, 50 VDC SINGLE STAGE SINGLE SWITCH POWER FACTOR CONVERTER

A. *Calculation of 'L_1' using EAC.*

Switching instant is considered as $\propto$ = 90°

$f_s = 20kHz$,

$D = 0.26$

$P_{out} = V_{rms} \times I_{rms}$

$$\therefore I_{rms} = \frac{100}{230} = 0.4348A$$

$$I_m = 0.6148A$$

Value of I_{peak} is calculated using EAC as follows

$$\frac{1}{2} \times 0.456 \times 50 \times 10^6 I_{peak} = I_m \times \theta$$

$$\frac{1}{2} \times 0.456 \times 50 \times 10^6 I_{peak} = 50 \times 10^6 \times 0.6148$$

$$I_{peak} = 2.696A$$

$$\therefore \quad L_1 = \frac{DTE_m}{I_{peak}} = \frac{0.26 \times 50 \times 10^6 \times 230 \times /2}{2.696}$$

$$= 1.57mH$$

B. Calculation of L_C

L_C is calculated for D = 0.26

Using (24), (33) $L_C = 1.2mH$

C. Calculation of energy storage capacitor.

$$I_{peak} = \frac{DTE_m}{L_1}$$

$$= \frac{0.45 \times 50 \times 10^{-6} \times 230 \times \sqrt{2}}{1.57 \times 10^{-3}}$$

$$= 4.66Amp$$

Energy Stored = $\frac{1}{2} L_1 I^2 = \frac{1}{2} \times 1.57 \times 4.66^2 = 17J$

Energy Stored = $\frac{1}{2} C_1 V^2$

$$C_1 V^2 = L_1 I^2$$

$$C_1 \times 540^2 = 1.57 \times 10^{-3} \times 4.66^2$$

$$C_1 = 116\mu F$$

VIII. RELATIONSHIP BETWEEN 'D' and LOAD

We have $I_p = \frac{2V0}{Rn(1-D)}$

$$\frac{DTEm}{L} = \frac{2Vo}{Rn(1-D)}$$

$$Vo = \frac{Rn(1-D)DTEm}{2L}$$

$$\frac{EmD}{n(1-D)} = \frac{Rn(1-D)DEm}{2Lf}$$

$2Lf = Rn^2(1-D)^2$

$$R = \frac{2Lf}{n^2(1-D)^2}$$

$$n^2(1-D)^2 = \frac{2Lf}{R}$$

$$n(1-D) = \sqrt{\frac{2Lf}{R}}$$

$$1-D = \frac{1}{n}\sqrt{\frac{2Lf}{R}}$$

$$D = 1 - \frac{1}{n}\sqrt{\frac{2Lf}{R}}$$

From the above equation we can conclude that for a given circuit duty ratio is function of load.

IX. SIMULATION RESULTS.

Simulation of the proposed single stage single switchpower factor converter withthe designed value of circuit parameters was carried out using Orcad software package. Simulation results were found meeting the design intends.

A. Testing under open loop control.

Open loop simulation was carried out by varying the duty ratio. Output voltage is found linear to on duty ratio. Input current is sinusoidal and in phase with the input line voltage. For duty ratio greater than 0.5, input current transition from DCM to CCM was observed.

B. Testing under closed loop.

Performance under closed loop condition was studied by varying the reference voltage. Output voltage was found varying linear with the reference voltage and input current was found sinusoidal and in phase with the input voltage. Fig 6

shows the harmonics spectrum of input current which indicates fundamental frequency of 50Hz is dominant and higher order components are insignificant .

Fig. 7 shows variation in input line current when the load is reduced after 15 ms.It is observed that in closed loop condition the dc bus voltage stress has been drastically reduced. When load is suddenlyreduced due to the instantaneous power unbalance, the dc bus voltage and output voltage tend to increase. But the increase in output voltage is immediately detected by the controller and duty cycle is automatically reduced within one to two switching cycles, the closed loop is found taking the corrective action leading to a new energy balance and a marginally low hike in dc bus voltage.

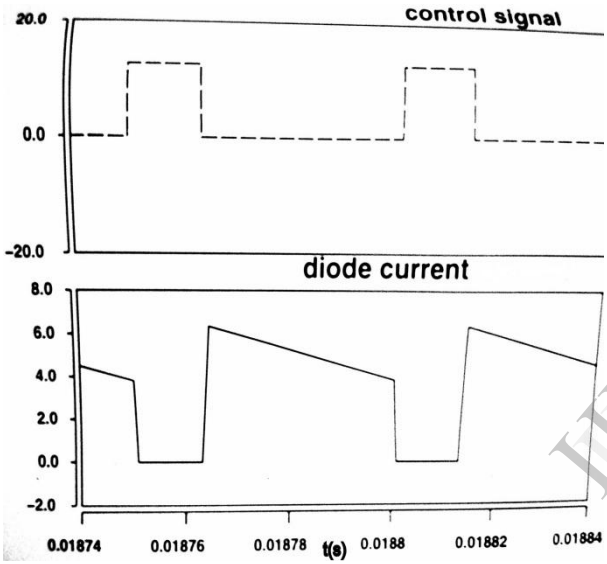

Figure 5. Shows that DC-DC converter operates in CCM

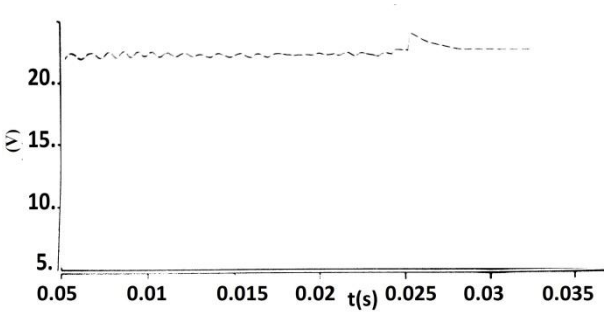

Figure 6. Shows that under open loop there is substantial increase in output voltage when load is reduced after 25 ms

Under closed loop condition when load is suddenly reduced due to the instantaneous power unbalance, the dc bus voltage and output voltage tend to increase.

Fig. 8 shows the increase in output voltage is immediately detected by the controller and duty cycle is automatically reduced, the closed loop is found taking the corrective action leading to a new energy balance.

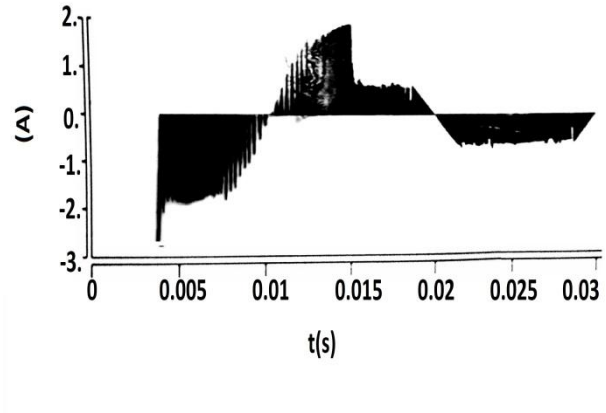

Figure 7. Shows the automatic reduction in the magnitude of input current under closed loop control when the load is reduced after 15ms

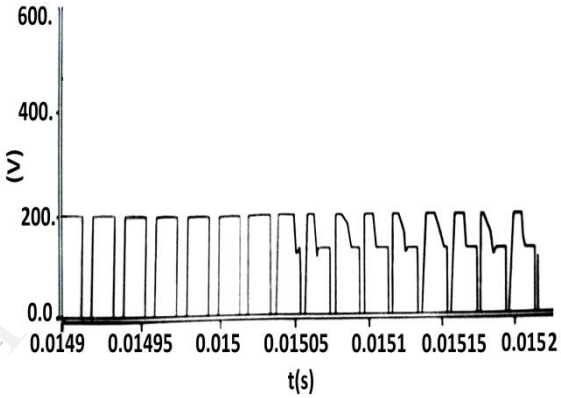

Figure 8.shows the voltage across switch when load thrown out at 15ms.Corrective action started after 2 switching cycle.

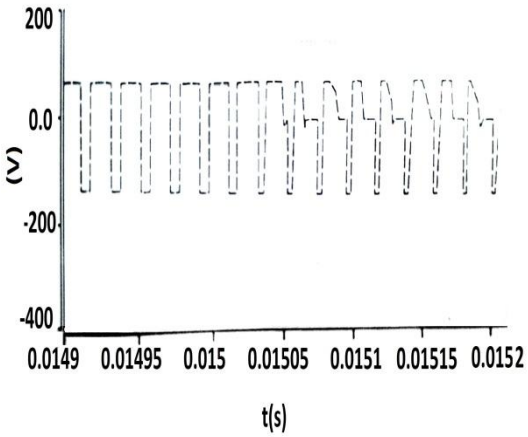

Figure 9.Shows the transformer primary voltage

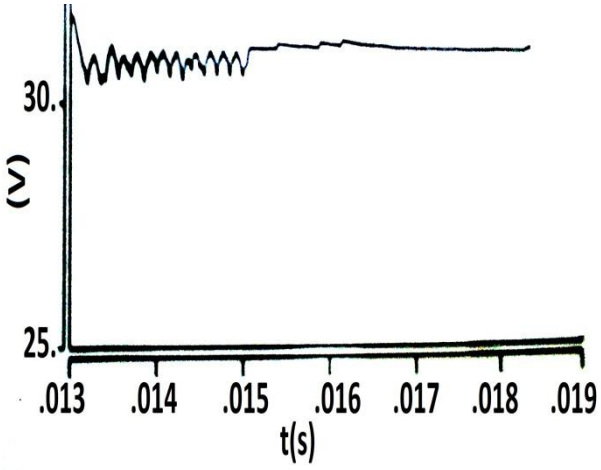

Figure 10.shows the output voltage

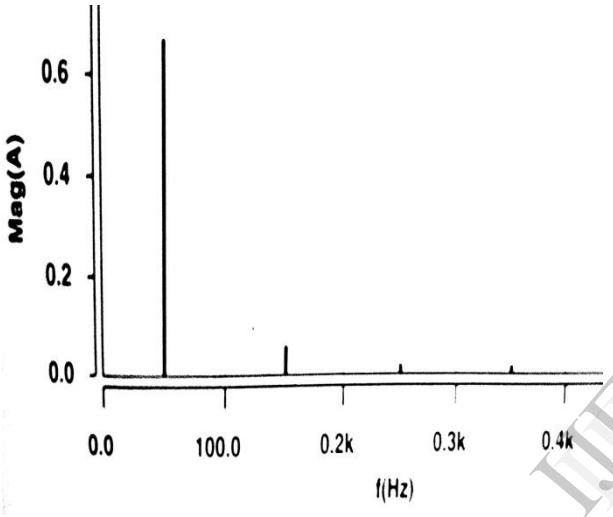

Figure 11.shows harmonic spectrum of input current

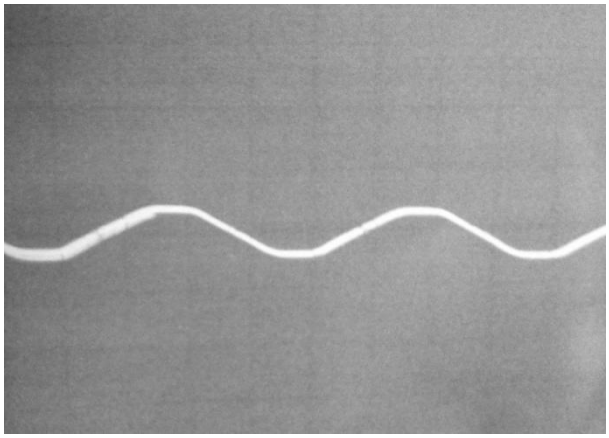

Figure 12shows that line current drawn is sinusoidal

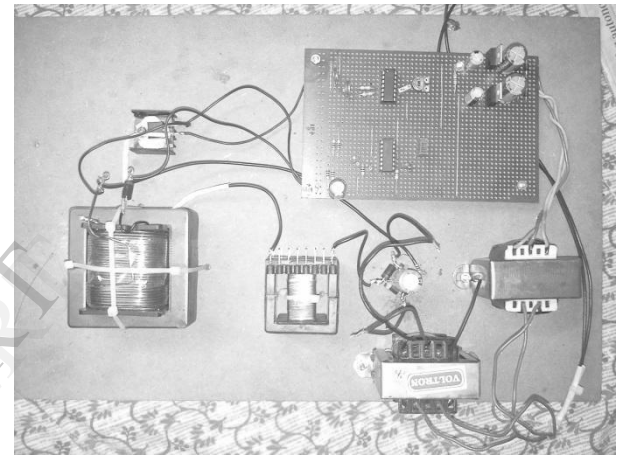

Figure 13. Photograph of the prototype

X. EXPERIMENTAL RESULTS

Experimental 230V, 50Hz input, 10-100V dc, 100w single stage single switch power factor converter has been built and tested using MOSFET IRFPF50 as switch, to verify the results obtained during simulated test. Steady stateoperation of converter is analysed. A design example of converter demonstrates, how to select converter parameters which will cause it to operate in the correct mode for a given line voltage, turns ratio, switching frequency, energy storage capacitor ripple, output voltage switching ripple and output voltage.

Experimental results are found in line with the results obtained during simulation when tested in open loop as well as closed loop condition. Fig. 10 shows sinusoidal nature of input line current and input power factor close to unity.

Main advantage of this converter among the single stage approach are simplicity size and efficiency and it does not contribute to any additional voltage stress.

XI. CONCLUSION

Single stage single switch power factor corrected converter design by applying EAC to determine value of boost inductance and by using closed loop control is presented. The dc bus voltage stress at light load is found completely eliminated under closed loop operations. Output voltage regulation using duty ratio variations and fixed switching period is the most simple method of control. For normal performance of the converter the duty ratio needs to be limited up to 0.5. Experimental results demonstrate that it is possible for the proposed converter to have fast response and low line current harmonic content.

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