Design of SRAM For Low Power and High Speed Applications

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Abstract—This paper presents design methodologies to reduce dynamic power and leakage power individually. In one of the designs a conventional 6T cell with two additional voltage sources, connected to the bit lines. As dynamic power dissipation is more during write operation, this technique reduces the dynamic power by reducing the voltage swing during write '0' or write '1' operation. Simulation is carried out in 90nm and extended to 45nm under 1V supply. Another design which employs asymmetric characteristic of SRAM targets reduction of leakage power by using high threshold(HVT) and low threshold(LVT) devices for robust functionality. This 5 transistor cell also proves to be advantageous in area due to reduced transistor count. Simulation is carried out in 45nm technology at 1V supply.

Keywords—leakage power, dynamic power, SRAM, HVT, LVT

I. INTRODUCTION

Currently, more than 50% of the area of system-on chip designs is occupied by embedded memory. The use of minimum-size transistors in static random access memories (SRAMs), along with technology scaling would adversely affect the leakage characteristics. As technology increases and so the speed of the operation of devices which has a direct impact on dynamic power as it is product of square of supply and capacitance to the frequency of operation $P=cv^2f$.Many topologies have been proposed to reduce dynamic and leakage powers in the past.

In charge sharing technique the bit-lines voltage swing has been reduced [3]. Another technique known as half swing pulse mode technique is also proposed to reduce the dynamic power [4].A 9t cell incorporates a separate read signal which activates the bit lines during read operation reduces leakage by 7% in standby mode [5].Robust asymmetric 6T-SRAM cell for Low-power operation in nano-CMOS technologies another robust asymmetric SRAM cell is proposed for a reliable low power operation and enhanced data stability[6].

An 8T-CDC SRAM cell with a gated word-line which enables the decoupling of the column/half-select condition [5] hence eliminating half select stability fails [7]. Another differential-read symmetric cell is proposed for improved data stability [8].

This paper presents novel design techniques for low power high speed SRAM circuits individually. In this paper the proposed SRAM cell, unlike the conventional 6T SRAM, contains two extra transistors connected to two voltage sources for reducing the voltage swing during write operation. It is found that for high frequency of operation, the dynamic power dissipation is almost constant for the proposed SRAM cell.

This paper also discusses a robust, low-voltage SRAM bit cell with a reduced transistor count, as compared to the standard 6T circuit. The proposed 5T bit cell is based on the circuit introduced in [7] with a number of significant modifications to enable low-voltage operation and low leakage power dissipation.

This paper is organized as follows: in section II, design of conventional SRAM cell is discussed. Section III discusses the design of voltage mode SRAM with reduced voltage swing for reduced dynamic power dissipation. Section IV discusses the design and architectural complexities of 5T asymmetric SRAM cell. The simulation results and discussions are presented in section V and finally section VI concludes the paper.

II. CONVENTIONAL 6T CELL

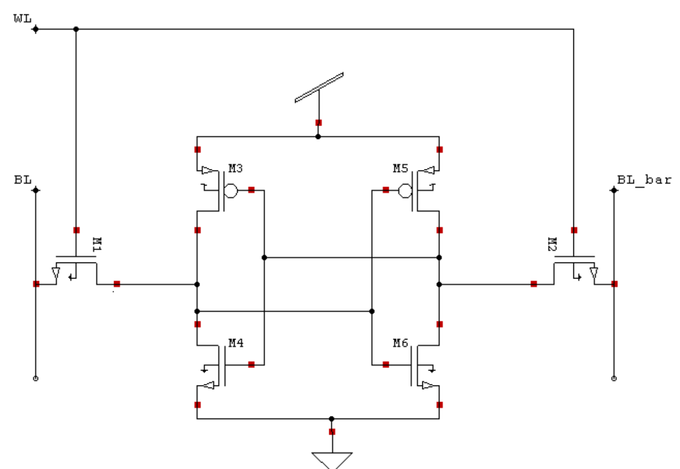

Fig. 1. 6T cell

Figure 1 shows the design of conventional 6T SRAM cell with positive feedback cross coupled inverters. The cell is selected by asserting WL= '1'. Which activates the access transistors M1 and M2. if WL ='0', circuit is in hold mode. For read operation WL is asserted to one and bit-lines are pre-charged.thestored charge on the output nodes, if zero,

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pulls one of the bit-lines to ground. The stored logic in the cell is read by inspecting the status of bit-lines.
For a write operation, the bit-lines are pre-charged to opposite polarity and WL is asserted to logic '1'. The logic is written to the output nodes through access transistors M1 and M2.
Conventional SRAM cell works on the full voltage swing.
This says that if the operating frequency of the SRAM cell isincreased then the dynamic power dissipation will also beincreased. Hence, for high speed CMOS operation theconventional SRAM cell is not a good choice.

III. VOLTAGE MODE SRAM CELL

In order to overcome the drawbacks due to increased frequency of operation in conventional 6t cell, the voltage mode SRAM proposes a technique to reduce the voltage swing on the bit-lines during write operation. It uses two additional voltage sources through two nmos transistors as shown in the figure 2 which are connected to the output node.

Write 0 operation:
During write 0 operation bit line is at logic 0 and bit-line bar at logic 1. Hence transistor vt1 is off and vt2 is on and voltage source vs2 is active which reduces the bit line voltage swing at the output node.

Write 1 operation:
Now bit-line is at logic 1 and bit line bar is at logic 0. Transistor VT1 is on and VT2 is off and hence vs1 source actively interferes at the output node to reduce the voltage swing.Sizing of the transistors is determined by the pull up and cell ratio of the SRAM cell.Cell ratio is the ratio of widths of pull down (NMOS)device to that of access transistor.
W4/W1 =2=W6/W2
Pull up ratio is the width of pull up(PMOS) device to that of access transistor.
W3/W1=1=W5/W2.

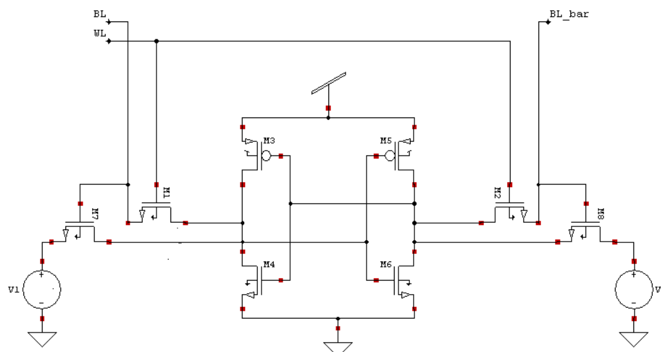

Fig. 2. Voltage mode SRAM cell.

IV. 5T ASYMMETRIC CELL

The performance of 6t cell is severely impeded by its read and write margins due to its destructive positive feedback. As the device dimension decreases, leakage power has a more pronounced effect. Around 40% of the total power in the short channel devices is due to leakage. The 5T cell addresses the leakage problem by a careful design which eliminates the positive feedback by removing one of the pull down transistors. This effect is compensated by use of High threshold voltage and low threshold voltage devices whose functionality in detail will be explained further.

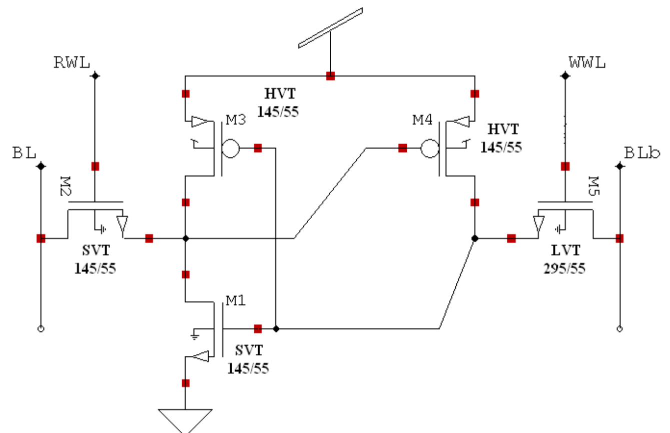

Fig. 3. 5T asymmetric cell.

Hold:For the trivial state of holding a logical "0", the operationof the proposed cell is similar to a standard cross-coupled latch.By discharging node *Q*,M5 is turned on (*V*SG5 = *V*DD), allowingnode*QB* to be fully charged to *V*DD. Accordingly, M1 isturned on (*V*GS1 = *V*DD), ensuring that *Q* remains discharged.The lack of a pull-down device under *QB* results in a veryRobust*hold* "0" state; however, it severely impedes the opposite(*hold*"1") state. In this state, *Q* is charged to *V*DD and *QB* isdischarged to ground. M3 is turned on (*V*SG3 = *V*DD), holding*Q* high, but nothing would seem to be holding *QB* low. Bymaintaining a stronger leakage current from *QB* to ground thanfrom*V*DD to *QB*, a stable state is ensured. This is achievedthrough three mechanisms: implementing M4 with a doublewidthLVT device; implementing M5 with an HVT device.
The read access of the 5T cell is initiated by pre-charging theBL signal, while holding BLbar discharged (its standby state).Subsequently, RWL is asserted, resulting in a single-endedreadout of node *Q*. If *Q* is high (the *hold* "1" state), there is novoltage drop over M2 and all voltage levels remain unchanged.
If *Q* is low (the *hold* "0" state), charge sharing is initiatedbetween BL and *Q*, discharging BL and resulting in a "0"readout. As with a 6T readout, the voltage level at *Q* rises,lowering the overdrive voltage of M5, potentially cutting off thepull-upof*QB*. However, *QB* is left at a high state, as there is noactive pull-down network to discharge it (the leakage pull-downtoBLbar takes much longer than the read access time). Therefore,once the read access is completed and RWL is lowered, M1(with*V*GS = *QB* ≈*V*DD) will quickly discharge *Q* back toits original state.
The single-ended read operation of the proposed 5T cell essentiallyremoves the read-sizing constraint of the right accesstransistor (M4). In fact, the 5T cell enhances the efficiency ofthe pull-up operation through M4, as node *QB* has no pull-downnetwork to contend with. Therefore, by charging BLbarand asserting WWL, *QB* is easily pulled up past the thresholdvoltage of M1, enabling the pull-down network of node *Q*. This*write*"0" operation can be achieved

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single-ended; however,by discharging BL and asserting RWL, a faster and more robustwrite operation is achieved. Writing a "1" is very similar to a 6T write operation. BL is charged, BLbar is discharged, and both WLs are asserted. Tosuccessfully flip the cell state, *QB* must be discharged past theswitching threshold of the left inverter (made up of M1 andM3), while *Q* must be charged high enough to cut offM5.

V. RESULTS AND DISCUSSION

Simulation is carried out in cadence spectre. Circuit layout is carried out according to standard design rules.

In voltage mode SRAM cell Switching instantaneous power atthe output nodes and bit-lines are analyzed and compared with that of standard 6T cell. Comparison is carried out both in 90nm and 45nm technology. Sizing of the transistors according to the technology is fixed using the cell ratio and pull up ratio mentioned in section III.

COMPARISON OF POWER DISSIPATION BETWEEN THEPROPOSED VS CONVENTIONAL SRAM CELL

At 90nm:

Table I: Power in 6T cell(units in watt):

frequency	Bitline	Bitline bar	Q	Q bar
100 MHz	11.15µ	13.5µ	0.66µ	0.65µ
500 MHz	65µ	67µ	0.71µ	0.7µ
1 GHz	132.6µ	135µ	0.77µ	0.77µ
2 GHz	267.6µ	270µ	0.9µ	0.89µ

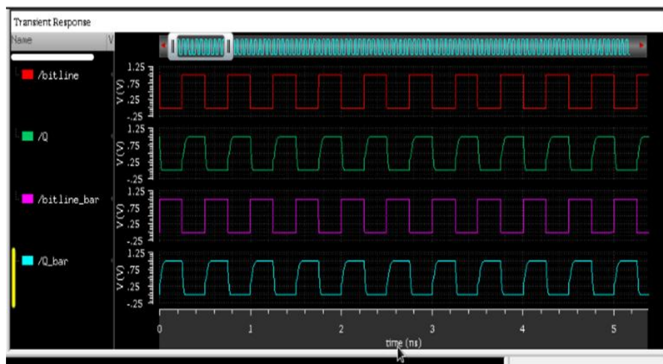

Fig. 4. Voltage mode SRAM cell operation at 2GHZ.

Table II: Power in voltage mode cell(units in watt)

Frequency	Bitline	Bitline bar	Q	Qbar
100 MHz	13.3µ	13.3µ	0.026µ	0.026µ
500 MHz	66.6µ	66.7µ	0.13µ	0.13µ
1 GHz	133µ	133µ	0.26µ	0.26µ
2 GHz	266µ	266µ	0.5µ	0.5µ

It is evidently seen that there is a reduction in the average switching powers of the bit-lines at different frequency of operations.

At 45nm:

Table III: Power in 6T cell(units in watt)

frequency	Q	Q bar	Bit-line	Bit-line bar
100 MHz	16.1n	21.3	1.837µ	2µ
500 MHz	98.8n	104n	10.1µ	10.32µ
1 GHz	202.2n	207.4n	20.6µ	20.6µ
2 GHz	408.8n	414n	41.9µ	41.39µ

Table IV: Power in voltage mode cell(units in watt)

Frequency	Q	Q bar	Bitline	Bitline bar
100 MHz	20.5n	27.14n	1.75µ	1.96µ
500 MHz	125.9n	132.5n	9.72µ	9.9µ
1 GHz	257.5n	264n	19.6µ	19.8µ
2 GHz	520.8n	527.4n	39.5µ	39.7µ

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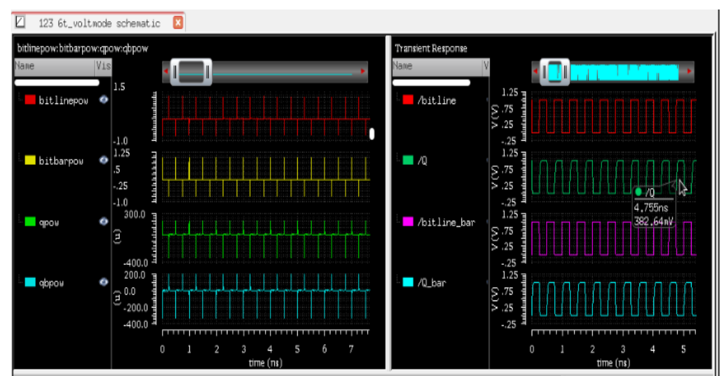

Fig. 5. Instantantaneous power of the output nodes and bitlines along with functionalitycheck of the cell at 2GHz.

Leakage power is calculated in 5T asymmetric cell and a drastic reduction in leakage power is observed. In conventional 6T cell the leakage power is measured to be 2.8µW and in 5T cell, it is measured to be 92.9pW. Such a drastic reduction is attributed to the use of HVT transistors.

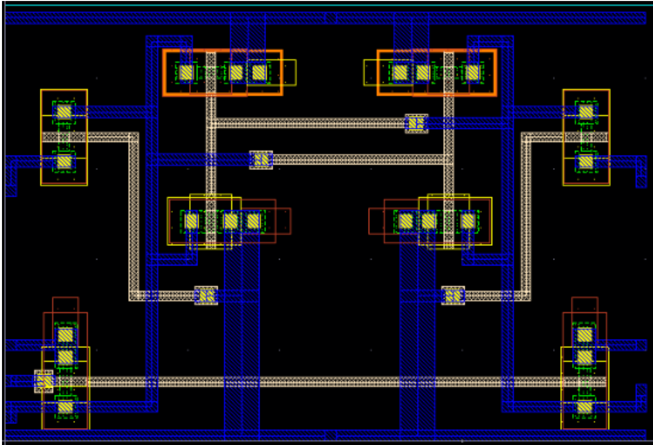

Fig. 6. Layout of voltagemode cell.

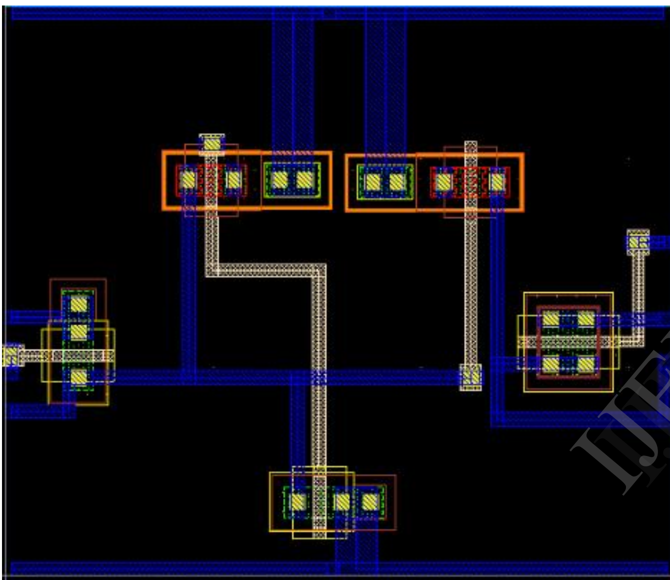

Fig. 7. Layout of 5T asymmetric cell.

VI. CONCLUSION

Though voltage mode SRAM proved to be advantageous in reduction of dynamic power, the overhead is in terms of area due to addition of two more transistors and voltage sources. But this technique can be very well used where low power is the target. The 5T cell proved to be good in terms of area, functionality but overhead is in the terms of design complexity. Further research can be carried out in integrating these techniques to achieve both low dynamic and leakage power.

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