Design of Universal Logic Gates based on CNTFET for Binary and Ternary Logic

[1]Radha Tapiawala, [2]Rahul Kashyap
[1,2]Department of Electronics and Communication Engineering (VLSI and Embedded system design)
Gujarat Technological University, Ahmedabad,
India and CDAC, Pune, India

***Abstract*—This paper addresses to comparison of logic gates using Carbon Nanotube Field Effect Transistors (CNTFET), for Ternary and Binary logic. First Carbon Nanotubes (CNTs) and importance of CNT over silicon based devices has been discussed, and then Basics of Ternary logic have been explained. Simulation of logic gates is performed using CNTFETs and comparison is done by changing various parameters.**

***Keywords*— MOSFETs, CNTs, CNTFETs, Ternary Logic**

I. INTRODUCTION

As Gordon Moore law predicted in 1965, the numbers of transistors duplicates in every 18 months in chips [1]. Therefore, the feature size of transistor should be as small as possible to impose more transistors on chip. While reducing feature size of traditional silicon based transistor in sub-10nm regime, it suffers from short channel effects which increases the gate leakage current, punch through effect and direct tunnelling from source to drain. Due to the limitation for miniaturization of transistors possess issues for researcher and directs the research towards the alternative semiconductor than silicon. The alternative of silicon in near future is Carbon Nanotubes with the properties like large mean free path, high carrier mobility. CNTs exhibit remarkable electronic and mechanical characteristics due to its extraordinary strength of the carbon-carbon (C-C) bond, the small atomic diameter of the carbon atom, the availability of free π-electrons in the graphitic configuration. The Study of Papers shows that CNT's can replace the channel, controlled by isolated electrostatic gates, for better switching behaviour.

In a ternary logic system, three logic levels are used (1, 0.5, 0) corresponding to high, middle and low voltage. Ternary Logic is a class of MVL (Multi-valued Logic) in which there are more than two truth values. Some of the other classes are Quaternary and Pentanary Logic. The Carbon Nanotube Field Effect Transistor (CNTFET) has emerged as a viable alternative to the bulk silicon transistors. It is a Low-power and High Performance Device due to its Ballistic Transport properties [9]. In CMOS based logic circuits the performance depends on the body effects using different bias voltages on the base or bulk terminal of the transistor. The Threshold voltage of a CNTFET is determined by the diameter of the CNT. Therefore, in order to achieve a multi-threshold design, CNTs with different diameters are used in a single circuit. This in turn implies the employment of different chirality in the CNTFETs. In [10], a resistive load design based on CNTFET has been initially proposed. The comparisons made in this paper depend on the design of universal gates. The design of digital hardware system depends on some of the important designs which are the inverter, NAND gate and NOR gate. In this paper, we have proposed some new ternary implementations of digital system like Standard ternary inverter, Negative ternary inverter, Positive ternary inverter, T-NAND and T-NOR gate.

In this paper, extensive simulation results and analysis of the same is shown so as to understand the comparison of binary and ternary logic's high speed performance and low power consumption. For the simulation purposes, SPICE language is used in which HSPICE simulation tool is accepted for its accuracy and speed-up simulations at an industry level.

II. CARBON NANOTUBES (CNTS)

Firstly introduced by Iijima during the IEEE Transactions on Nanotechnology in 1991. He proposed about the new type of carbon structure which was needle like tubes of diameter varying from 4-30 nm [2]. By surveying application regarding to the transistors the channel of traditional MOSFET will replace by CNT. In MOSFET when we shrunk the size 20nm then face the serious limit like short channel, power dissipations and electron tunnelling, from MOSFET channel. Carbon Nanotubes (CNTs) have attraction of researchers worldwide in recent years because of its small dimensions and unique architecture properties. For passive or active elements in post-CMOS Nano-electronics carbon Nanotubes are the best replacement device.

CNTs are basically hollow cylinders of rolled-up Graphene sheet composed of one or more concentric layers of carbon atoms in a honeycomb lattice arrangement. All carbon atoms are involved in hexagonal aromatic rings only and are therefore in equivalent position, except at the Nanotubes tips each tip are involved in pentagonal rings. CNTs can carry current density of the order 10 μA/nm2, while standard metal

wires have a current carrying capability of the order 10 nA/nm2. Nanotubes are mainly classified into two types depending upon the structure:

Single-walled Carbon Nanotubes (SWNTs):
Consist of a single graphite sheet seamlessly wrapped into a cylindrical tube.

Multi-walled Carbon Nanotubes (MWNTs):
Comprise an array of such Nanotubes (more than one wall) that are concentrically nested within.

The diameter of SWCNT's can be as small as 0.4 nm. The range of diameter is between 0.7 to 3 nm with the mean diameter of 1.7 nm [3]. The diameter of CNT can be calculated by the following expression,

$$D_{CNT} = \frac{\sqrt{3}a0}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad \text{.....(1)}$$

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \qquad \text{.....(2)}$$

The SWNTs are structurally different from MWNTs by having different basic arrangements of the carbon atoms to give three different structural configurations depend on the chiral number (n_1, n_2):

Armchair arrangement ($n_1 = n_2$) where the presence of chairs are perpendicular to the tube axis which characterized the chiral vector;
Zigzag arrangement ($n_1 = 0$ or $n_2 = 0$) where the tube is characterized by having a V-shape perpendicular to the tube axis; and
Chiral or helical arrangement, which is different from the above two types of arrangement in this electrons in CNT are restricted within the atomic plane of graphene.

III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

In the Nano scale era, Carbon Nanotube Field Effect Transistor (CNTFET) is a promising device for future integrated circuits because of its tremendous properties like ballistic electron transport, high carrier mobility (103–104 cm2/V·s) within semiconducting carbon nanotube (CNTs) moreover because of the absence of dangling bond which enable integration of high-k dielectric material that result in better gate electrostatics. The first carbon nanotube field-effect transistors were reported in 1998.

A. *Structure of CNTFET*

The CNTFET has basically four terminals: (drain, source, gate, and back-gate). It has structure of double gate to improve carrier mobility and to control off state of CNTFET.CNT acts as conducting channel between two electrodes served as source and drain. The doped Si-substrate served as the back-gate. A metal gate surrounds a dielectric which is wrapped around a portion of the undoped nanotube in the intrinsic region, whereas the other nanotube regions are heavily doped for a low series resistance during the ON-state. The field effect transistors of Carbon Nanotubes can be structured in into three types:

a) Back gate CNTFET: The back gate CNTFET was firstly proposed by Rahman et al. [4]. Majority of early CNTFET devices were back-gated with very thick gate insulators made of silicon oxide approximately around 100-150 nm [5]. The highly doped SWCNT was used as bridge and acts as conducting channel to connect the two metal contacts source and drain.

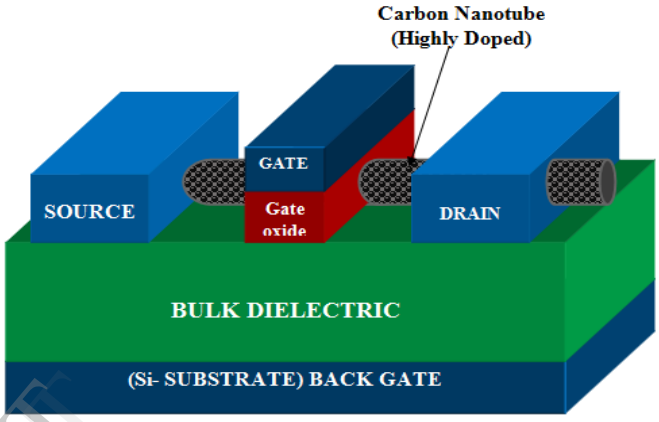


Figure 1 Back gated CNTFET

b) Top gate CNTFET: The first top gate CNTFET was proposed by Wind et al. in 2003. This top-gated structure is the next generation of CNTFET to improve the device performance. Since the device operation of back gated structure has rated lower in performance, thus this new structure is expected to bring better result. This structure was fabricated by dispersing the Carbon Nanotube on an oxidised wafer [5]. In this structure the gate is placed over the CNT, shown in Figure 2.

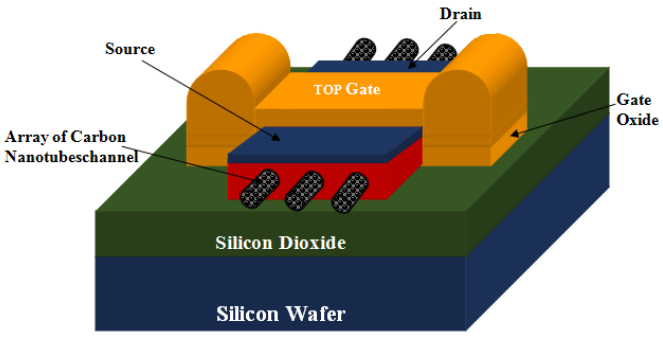


Figure 2 Top gated CNTFET

c) *Vertical CNTFET:* The latest development in structure of CNTFET could be the vertical CNTFET. This structure was suggested by Choi et al. in 2004. The diameter of carbon nanotube which corresponds to tera-level CNTFET and density of 1012 elements per cm^{-2} as the transistor size could be as small as possible. The cross section and schematic of vertical CNTFET is shown in Figure 3.

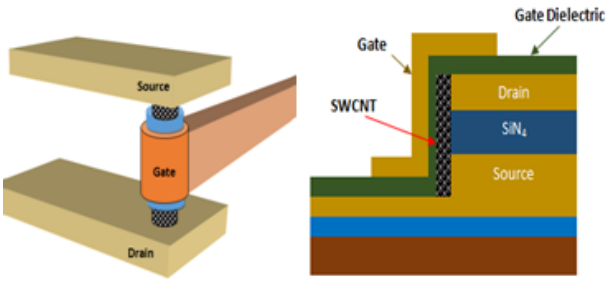


Figure 3 Vertical Gated CNTFET

B. *Types of CNTFET*

As CNTFET can be available in different structure, it can be classified into two types (1) Schottky barrier CNTFET, (2) MOSFET like CNTFET, based on their current injection methods [6]. Current transport mechanism and device output characteristic is used to differentiate the type of contact of CNTFET as its Ohmic or Schottky contact.

a) SB-CNTFET: The Schottky barrier type CNTFET is shown in Figure 4 given below. In this type of CNTFET Intrinsic CNT is used as channel with direct metal contacts. These metal contacts are made of source and drain region [7]. Current is constituted by potential barrier of source and drain region which is produced by tunnelling of electron and holes.

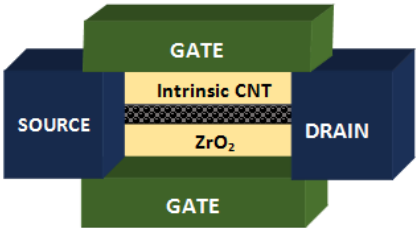


Figure 4 SB – CNTFET

b) MOSFET like CNTFET: In this structure source and drain terminals are heavily doped by n^+ impurities like MOSFET and therefore it is termed as MOSFET-like CNTFET. The device structure is shown in Figure 5. In this device the variations in barrier height is due the change in applied gate voltage and the number of charge is induced by the gate terminal in the channel which made of CNT to control the drain current.

IV. CONCEPT OF TERNARY LOGIC

Ternary logic system is defined by using three significant values as compared to binary logic, which uses two values. These values are represented as false, undefined and true respectively and are denoted as 0, 1 and 2 in this paper.

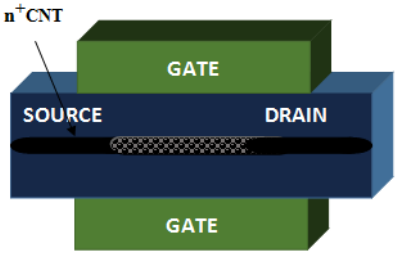


Figure 5 MOSFET like CNTFET

According to the definition, any ternary function *f(X)* with variable *n* {*X1... Xn*} is defined as a logic function mapping $\{0,1,2\}^n$ to {0,1,2}. The Basic operations of a ternary Logic is defined as follows:

$$X_i, X_j = \{0,1,2\}$$
$$X_i + X_j = \max\{X_i, X_j\}$$
$$X_i \bullet X_j = \min\{X_i, X_j\}$$
$$\bar{X}_i = 2 - X_i \qquad \text{.....(3)}$$

Where – denotes arithmetic subtraction, operations +, • denotes the OR, AND in ternary logic arithmetic, respectively. In a binary logic system the universal gates are NAND and NOR, which are used to design circuits. The fundamental gates in a ternary logic system are the inverter, NOR and NAND gates respectively. The ternary logic levels and values are shown in TABLE I.

TABLE I
Logic Values

Voltage Level	Logic Value
0	0
$1/2V_{dd}$	1
V_{dd}	2

A. *Ternary Inverter*

A Ternary Inverter is a fundamental gate in ternary logic system. A general ternary inverter is defined as an operator with one single input *x* and three outputs *y0, y1* and *y2*.

$$y_0 = C0(x) = \begin{cases} 2, & x = 0 \\ 0, & x \neq 0 \end{cases}$$
$$y1 = C1(x) = \bar{x} = 2 - x$$
$$y_2 = C2(x) = \begin{cases} 2, & x \neq 2 \\ 0, & x = 2 \end{cases}$$

.....(4)

Thus, for the implementation of ternary inverter, three inverters are required. These three inverters are Standard ternary inverter (STI), Negative ternary inverter (NTI) and Positive ternary inverter (PTI). According to (4) if the three *y0, y1* and *y2* are the outputs, and *x* is the input then the truth table for STI, NTI and PTI is shown in TABLE II. The

phenomenon behind working of these three inverters is entirely different from that in binary inverters.

B. Ternary NOR and NAND gates

The Ternary NOR and NAND gates are multiple input operable gates used in Ternary Logic system. For the two inputs X_1 and X_2, the functions for the Ternary NOR and NAND gates are defined by following two equations.

$$Y_{nand} = \overline{\min\{X_1, X_2\}}$$
$$Y_{nor} = \overline{\max\{X_1, X_2\}} \quad \ldots\ldots\ldots\ldots(5)$$

TABLE II
TRUTH TABLE FOR STI, NTI AND PTI

Input X	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

TABLE III
TRUTH TABLE of NAND and NOR GATES

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

The Truth table for Ternary NAND and NOR gates is shown in the TABLE III.

V. ANALYSIS OF LOGIC GATES

We have designed the different digital logic gates and demonstrate the simulation of these logic gates by binary and ternary logic. After simulation, we have analysed their average power, delay and PDP (Power delay product). As analysis is shown below in TABLE IV which shows that among all basic logic gates, NAND gate is the most beneficial in terms of power and total delay. The schematic design and simulation waveform is shown in this section.

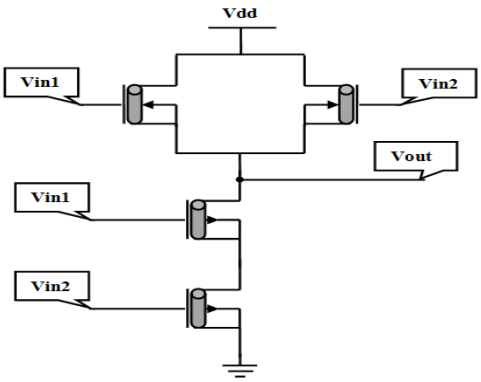


Figure 6 Schematic of NAND gate

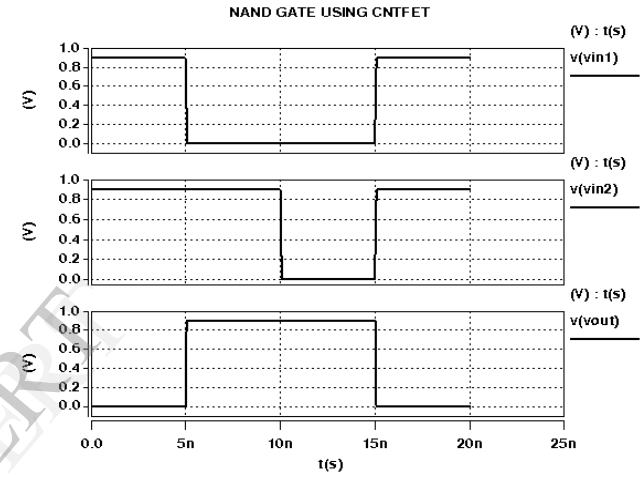


Figure 7 Transient Response of NAND gate

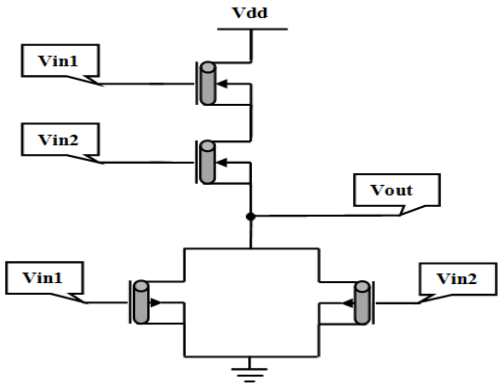


Figure 8 Schematic of NOR gate

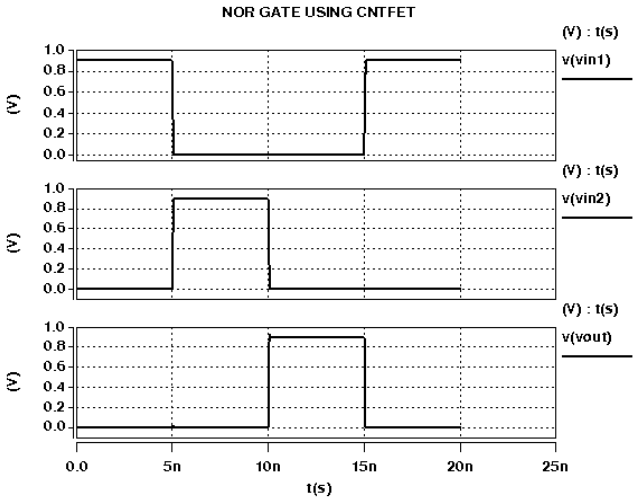
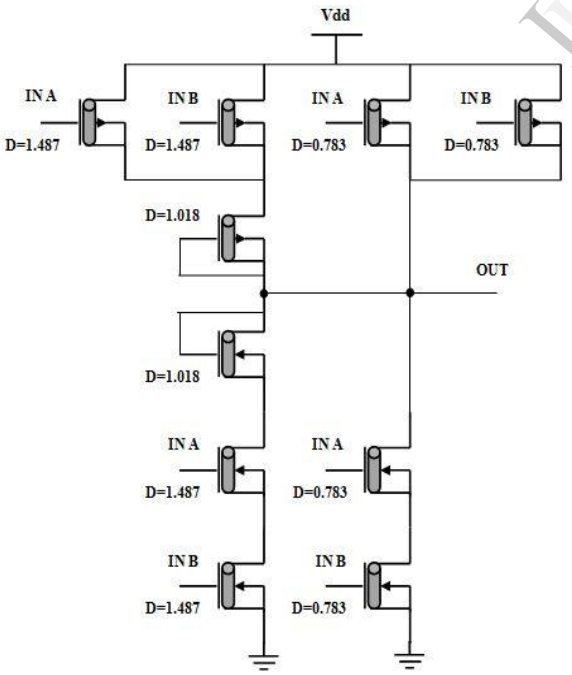


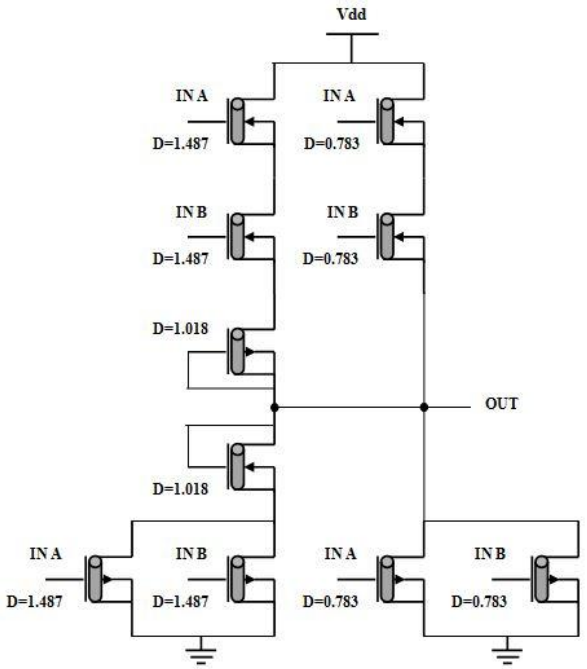
Figure 9 Transient Response of NOR gate

In the schematic of Binary NAND gate shown in Figure 6, there are four CNTFETs used. The schematic is similar to that used in CMOS NAND structure. The design of binary NOR gate is also similar to that in traditional circuits. The transient response for NAND gate is shown in Figure 7 and for NOR gate is shown in Figure 9. In Ternary Logic based NAND gate design, there are ten CNTFET transistors.

The Circuit schematic for two input Ternary NAND and NOR gates are shown in the Figure 10(a) and Figure 10(b) and their logic expressions are given by (5).



(a)



(b)

Figure 10 Schematic Diagram of CNTFET based
(a) Ternary NAND and (b) Ternary NOR gates.

Each of these gates consists of ten CNTFETs with three different Chiralities. In these two gates, the transistors with diameters of 1.487, 0.783, and 1.018 nm have threshold voltages of 0.289, 0.559, and 0.428 V, respectively, as established using (2). HSPICE simulation has confirmed the correctness of these designs with Tables II and III.

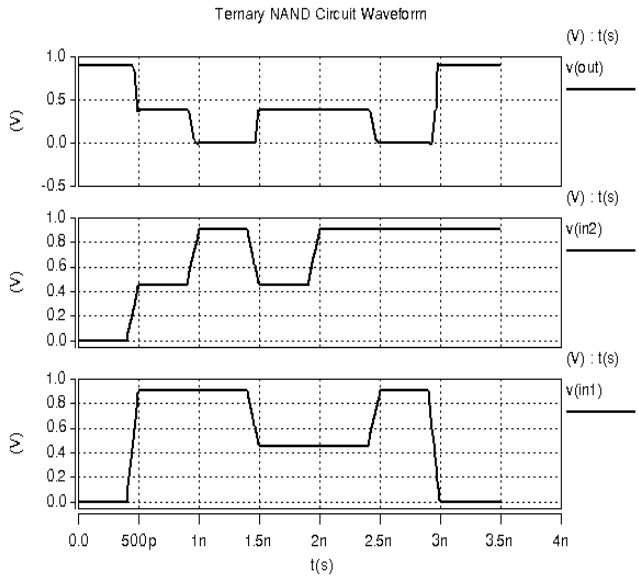


Figure 11 Transient Response of Ternary NAND Gate

The simulation for the characteristics of STI is done using the CNTFET model in [12]. The model is MOSFET like CNTFET model for circuit simulation purpose developed by Stanford University. The language used to develop the Stanford CNTFET model is HSPICE. This HSPICE model is described more detail in [13] and [14].

TABLE IV
Performance Analysis of CNTFET Based Logic Gates

Logic Gates	Propagation Delay (τ_P)(sec)	Average Power(P_{AVG}) (Joule/sec)	PDP(Joule) = $P_{AVG}*\tau_P$
NAND	2.6877e-11	1.5360e-08	4.1282e-19
NOR	9.9816e-09	2.1703e-08	2.1663e-16
TNAND	2.9353e-11	9.3797e-08	2.7532e-18
TNOR	1.9131e-09	1.5126e-09	2.8936e-18

The results in Table IV show the exact performance of universal logic gates in terms of propagation delay, average power and PDP. It can be seen clearly that speed of operation and average power are nearly similar for both types of NAND gate. Moreover, the PDP analysis gives the exact idea about overall performance of these gates and helps in finding the static Noise Margin for these gates. As far as the application is concerned they can be used together in a combination for a single circuit design.

VI. CONCLUSIONS

Simulations are performed on HSPICE, which shows that the proposed CNTFET device is more preferable then silicon based device in terms of performance. After analyzing the simulation results for Universal Gates for both Binary and Ternary Logics, Conclusions are derived that the CNTFET based Logic gates consume less power with better speed of operation. Though there is a trade-off between Number of Computations and Size of the Chip in Ternary Logic, both of them have their own importance and uses. Therefore the assessment of this work demonstrates that CNTFET is a viable candidate for design of logic circuits in Nano scale era. Also, combining both Ternary and Binary Logic on a same circuit board can reduce number of operations to realize a function and also the size of the chip.

ACKNOWLEDGMENT

This is acknowledging with thanks to department of Electronics and Communication Engineering (VLSI and Embedded System Design) of Gujarat technological University, Ahmedabad, India and CDAC, PUNE for giving us facility of IEEE E-Library access, Computer lab and Library which facilitated and encouraged us to complete this work.

REFERENCES

[1] Samira Shirinabadi Farahani, Ronak Zarhoun and Keivan Navi, "An Efficient CNTFET Based 7-Input Minority Gate", *International Journal of VLSI design & Communication Systems (VLSICS)*, Vol. 4, No.1, February 2013.
[2] Iijima S., "Helical microtubules of graphitic carbon". *Nature 1991*; 354: 56–58.
[3] Rasmita Sahoo and R. R. Mishra, "Simulations of Carbon Nanotube Field Effect Transistors", *International Journal of Electronic Engineering Research ISSN 0975- 6450*, Volume 1 Number 2 (2009) pp. 117–125.
[4] Rahman. A. et al., "Theory of Ballistic Nano transistors", *IEEE transactions on Electron Devices ISSN 1853-1861*, 2003.
[5] Zoheir Kordrostami and Mohammad Hossein Sheikhi, "Carbon Nanotubes", Chapter 9.
[6] Subhajit Das, Sandip Bhattacharya, Debaprasad Das, "Design of Digital Logic Circuits using Carbon Nanotube Field Effect Transistors", *International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307*, Volume-1, Issue-6, December 2011.
[7] Jingqi Li, Chao Zhao, Qingxiao Wang, Qiang Zhang, Zhihong Wang, X.X. Zhang, A.I. Abutaha, H.N. Alshareef, "Vertically aligned carbon nanotube field-effect transistors", *2012 Print, Elsevier Ltd.*
[8] Aaron D. Franklin, Robert A. Sayer, Timothy D. Sands, David B. Janes, Timothy S. Fisher, "Vertical Carbon Nanotube Devices With Nanoscale Lengths Controlled Without Lithography", *IEEE Transactions On Nanotechnology*, Vol. 8, No. 4, July 2009.
[9] J. Appenzeller, "Carbon Nanotubes for high-performance electronics: Progress and prospect," *Proc. IEEE*, vol. 96, no. 2, pp. 201–211, Feb. 2008.
[10] A. Raychowdhury and K. Roy, "Carbon-Nanotube-based voltage-mode Multiple valued logic design," *IEEE Transactions on Nanotechnology*, vol. 4, no. 2, pp. 168–179, Mar. 2005.
[11] Sheng Lin, Student Member, *IEEE, "*CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits" *IEEE Transactions on Nanotechnology*, Vol. 10, No. 2, March 2011.
[12] (2008). Stanford University CNFET model Website. Stanford University, Stanford, CA [Online]. Available: http://nano.stanford.edu/model.php?id=23.
[13] J. Deng and H.-S. P. Wong, "A compact SPICE model for Carbon-Nanotube field-effect transistors including no idealities and its application—Part I: Model of the intrinsic channel region," *IEEE Trans. Electron Device*, vol. 54, no. 12, pp. 3186–3194, Dec. 2007.
[14] B. Wang, P. Poa, L. Wei, L. Li, Y. Yang, and Y. Chen, "(n, m) Selectivity of single-walled Carbon Nanotubes by different carbon precursors on Co–Mo catalysts," *J. Amer. Chem. Soc.*, vol. 129, no. 9, pp. 9014–9019, 2007.