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Designing A Differential Flip-Flop with Static Contention Free Characteristics Utilizing GDI-AND Implementation in Clock Gating Technique

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***Abstract*—In this study, a static contention-free differential flip-flop architecture is shown. This is accomplished by utilizing a clock gating mechanism in conjunction with a GDI-AND configuration. The goal of the suggested method is to improve flip-flop performance and reliability in digital circuits, especially for applications that call for low-power and low-voltage operation. Contention problems are reduced by using a GDI-AND structure in the clock gating approach, guaranteeing reliable and effective operation. The design process is described in the abstract, with special attention to the creative application of clock gating using a GDI-AND and the incorporation of static contention-free features. By improving the reliability and efficiency of differential flip-flops, this research helps to advance their design and benefit contemporary digital system.**

■ ***Keywords*—GDI-AND structure,Differential Flip-Flop**

1. INTRODUCTION

In the recent past, low power consumption and small surface area have drawn the attention of VLSI system designers, and this tendency is still present today. The transmission gate, which produced better results in the fields of power and surface area, effectively provided a remedy to this problem as the conventional complementary metal oxide semiconductor (CMOS) gates were unable to meet the aforementioned basic criteria. The intense research being done in low power microelectronics is a result of the rapid advancements in cellular networks and portable systems.

Static Flip flop are the basic part of industrial digital circuit,Which effect speed & total power consumption .Introduces the design of a differential flip-flop featuring static contention-free characteristics.In CMOS, a static contention-free differential flip-flop (SCDFF) is introduced for low-voltage and low-power applications. Using two differential latches and the same area as a traditional transmission-gate flip-flop (TGFF), the SCDFF provides completely static and contention-free operation without superfluous internal clock transitions. Wide-range voltage scalability is made possible by the entirely static and contention-free operation, which permits significant variation tolerance at a low supply voltage regime.

One interesting approach to obtaining higher energy efficiency is NEAR-THRESHOLD voltage (NTV) computing, in which the supply voltage is placed in close proximity to the transistor threshold voltage. While near-threshold approaches offer tremendous benefits in terms of energy and power, they also present significant hurdles in terms of performance and variability.

In this context, flip-flops (FFs), which are essential parts of sequential logic circuits, are especially important. These FFs have a significant impact on the ruggedness, size, overall power consumption, and overall performance of systems. Acknowledging the critical significance of FFs, current research efforts have been focused on the creation of reliable, low-power circuits, primarily in the NTV region. This focus results from the realization that FFs are essential for maximizing system dependability and energy efficiency in semiconductor technologies that operate within the NTV paradigm.

One differential-type FF eliminates superfluous data entirely.Internal clock oscillates yet experiences conflict.Due to the absence of attribute 1 or 2, the documented FF designs to date experience redundant internal clock transitions and/or functional failure. One differential-type FF, for instance, eliminates all unnecessary internal clock transitions, but it has contention issue.

This piece suggests a static contention-free differential FF (SCDFF) that maintains no redundant clock transitions with a silicon area equivalent to that of a conventional transmission-gate FF (TGFF), eliminates contention from the differential type FF with a footer/header structure, and removes dynamic nodes using a ground/supply bridge to achieve fully static operation and contention-free transitions. The suggested design, which maintains reliability very close to threshold voltage, exhibits a considerable reduction in power consumption when compared to previous arts FFs thanks to the use of a differential structure with static contention-free properties. To confirm its low power, dependable characteristic, the SCDFF is implemented in a 32-nm LP process with various prior-art FFs (TGFF, S2CFF, and ACFF). Power, reliability, setup time, hold time, and clock-to-q (c–q) latency are measured.

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II. LITERATURE REVIEW

The topologically-compressed flip-flop (TCFF), a very low-power flip-flop (FF), is suggested. At 0% data activity, the FF reduces power dissipation by 75% in comparison to conventional FFs. Among the FFs that have been recorded thus far, this one has the largest power reduction ratio. The reduction is accomplished by merging conceptually equivalent transistors into an unusual latch structure and using the topological compression method. The power is significantly reduced by the relatively small number of transistors—just three—connected to the clock signal, and the smaller overall transistor count ensures the same cell area as traditional FFs. Furthermore, the cell is resistant to variations in input slew and supply voltage due to its entirely static full-swing operation. A 40 nm CMOS experimental chip design demonstrates that nearly all typical FFs are interchangeable.

For real-time, portable electronics, low power consumption and high throughput are essential criteria. Digital signal processing (DSP) systems have effectively achieved high throughput through the use of pipelining. The most power-efficient circuit family is thought to be static CMOS when the throughput demand is not particularly great. Nevertheless, static CMOS tends to lose its power-delay efficiency for very high throughput applications. This is because static CMOS limits throughput rate and increases power consumption by requiring additional pipelined latches, which add extra latency. In the deepest level of pipelining, instead of using lengthy chains of transistors in series, each pipeline block is made up of just two or three basic input gates (AND/NAND, OR/NOR, or XOR/XNOR, for example).

For ultra-low power applications, we present a unique 24-transistor change-sensing flip-flop (CSFF) in this study. When there is no change in the flip-flop content, the suggested CSFF removes unnecessary transitions of internal clocked nodes with the use of an internal change-sensing unit. Unlike the traditional transmission-gate flip-flop (TGFF), no extra transistors are needed. Compared to TGFF and SSCFF, CSFF achieves the power reduction of 82% and 68% at 10% activity rate and 1.0V, and the C-Q delay improvement of 37% and 11% .supply voltage range of 0.4V to 1.0V, according to measurement data from a test chip made in 40nm CMOS technology. Improved power and energy efficiency are attained by CSFF without sacrificing reliable performance at ultra-low voltage operations. A transistor may enable the slave latch to interfere with the master latch's stored value. An SFL can be used as the master latch and a static headed latch as the slave latch to create a SCDFF. The SFLs in the SCDFF, in contrast to the ACFF, are connected by gate connections rather than diffusion connections, enabling completely static and contention-free operation. When the present data (Qprev) and the next data (D) diverge, the SCDFF operates in detail.

For chip designers nowadays, power has emerged as the main design limitation. This area has more favorable performance and variability characteristics while retaining a large portion of the energy savings of subthreshold operation. This means that it can be used with a wide variety of power-constrained computer segments ranging from high-end servers to sensors

In 28-nm CMOS, a static contention-free differential flip-flop (SCDFF) is introduced for low-voltage and low-power applications. Using two differential latches and the same area as a traditional transmission-gate flip-flop (TGFF), the SCDFF provides completely static and contention-free operation without superfluous internal clock transitions. Wide-range voltage scalability is made possible by the entirely static and contention-free operation, which permits significant variation tolerance at a low supply voltage regime.

III. DESIGN METHODOLOGY

In a brand-new CMOS Static Contention-Free Differential Flip-Flop (SCDFF) intended for low-voltage and low-power applications. With the use of footed differential latches, the SCDFF provides a novel method for static and contention-free operation without requiring unnecessary internal clock changes. Interestingly, it takes up the same silicon area as a traditional TGFF (Transmission-Gate Flip-Flop).An SFL can be used as the master latch and a static headed latch as the slave latch to create a SCDFF. The SFLs in the SCDFF, in contrast to the ACFF, are connected by gate connections rather than diffusion connections, enabling completely static and contention-free operation.

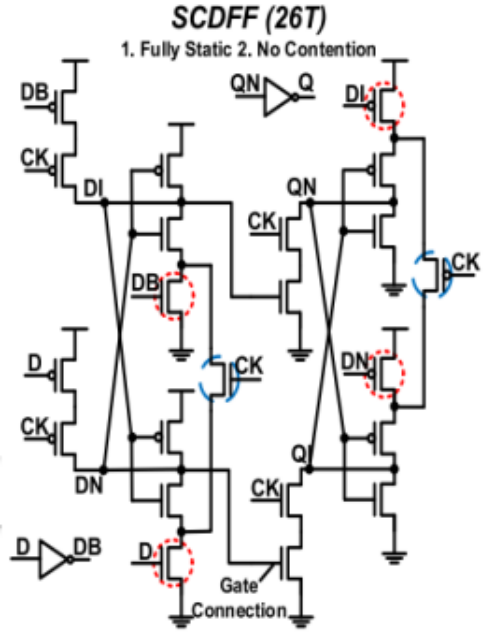

Fig.1 Static Contention free Differential Flip-flop (S CDFF)

In contrast, the proposed SCDFF provides static contention-free operation with a footer/header + ground/supply bridge construction and completely avoids redundant clock transitions through a differential structure. Low-voltage operation down to the NTV regime is made possible by this.*The SCDFF* can operate down to NTV because, as its comprehensive operation demonstrates, it is static and free from contention.The suggested SCDFF has the fewest effective clock load transistors

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when extra sizing for FFs with unreliable characteristics is taken into account. The differential structure removes redundant internal clock transitions, and the footer/header + supply/ground bridge structure ensures variation-tolerant operation.
Describes how a GDI-AND configuration within a clock gating approach is used to create a differential flip-flop with static contention-free properties. The goal of the suggested method is to improve flip-flop performance and reliability in digital circuits, especially for applications that call for low-power and low-voltage operation. Contention problems are reduced by using a GDI-AND structure in the clock gating approach, guaranteeing reliable and effective operation.Additionally, a thorough discussion is held regarding the benefits and significance of clock gating strategies. Power consumption is a disadvantage even though the traditional qualities have the greatest advantages in terms of contention and retention free.

CLOCK GATING TECHNIQUE:
Clock gating reduces power or delay depending on the circuit by requiring an additional logic to provide a clock enabling signal, which is only activated when the circuit design dictates a logic 0 or 1 value. Knowing the approximate power dissipation of a circuit, given its intended use, is a crucial prerequisite for designers. Any circuit's overall power consumption is made up of both static and dynamic power. The clock network's decreased switching capacitance and the switching activity caused by storage components when the clock is idle are the sources of the power savings.

GATE BASED CLOCK GATING:
One of the most straightforward methods is gate-based clock gating, which has an easy-to-implement design. Any gate can be utilized with this method. The AND, XOR, and NOR gates are the ones that are being discussed.

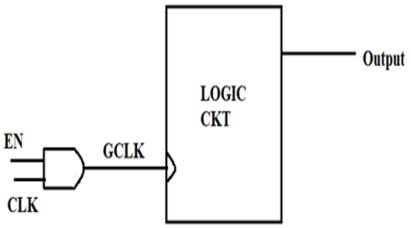

Fig.2 Model diagram of clock gating technique

GDI (GATE DIFFUSION INPUT):
Due to the rising need for modern technology, reduced power consumption has been a crucial design constraint in recent years.intricate mobility system in the VLSI circuit architecture. Circuit designers are more aware than ever of how power consumption affects integrated circuit performance because it is a direct correlation to IC dependability.
The GDI cell contains three inputs: G (common gate input of pMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS.

GDI BASED SCDFF:
Explains how to make a differential flip-flop with static contention-free qualities using a GDI-AND arrangement within a clock gating technique. Enhancing flip-flop performance and reliability in digital circuits is the aim of the proposed approach, particularly for low-power and low-voltage applications. By employing a GDI-AND structure in the clock gating technique, contention issues are minimized and dependable and efficient operation is ensure

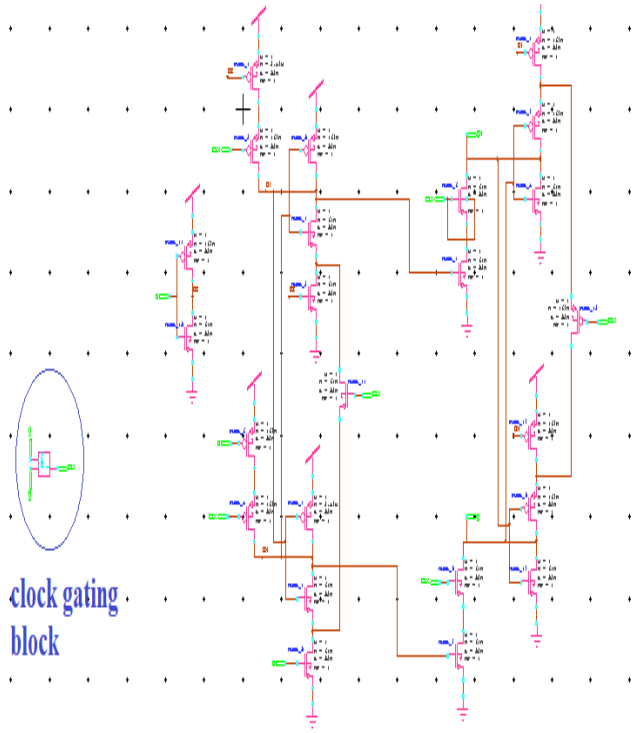

Fig.2 SCDFF Structure with GDI Implementation

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IV.RESULTS AND DISCUSSION

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication.
The Figures shown below is the Output for SCDFF with Clock gating technique implementation.
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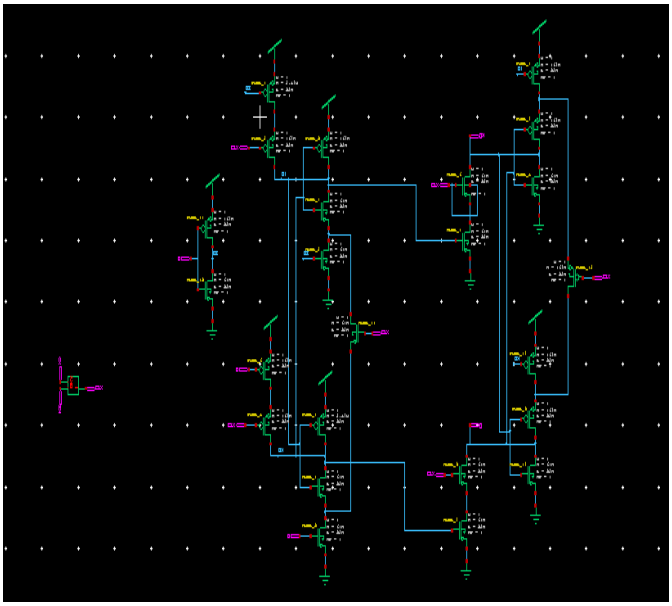

Fig.3 Schematic design of Clock gating implementation based SCDFF

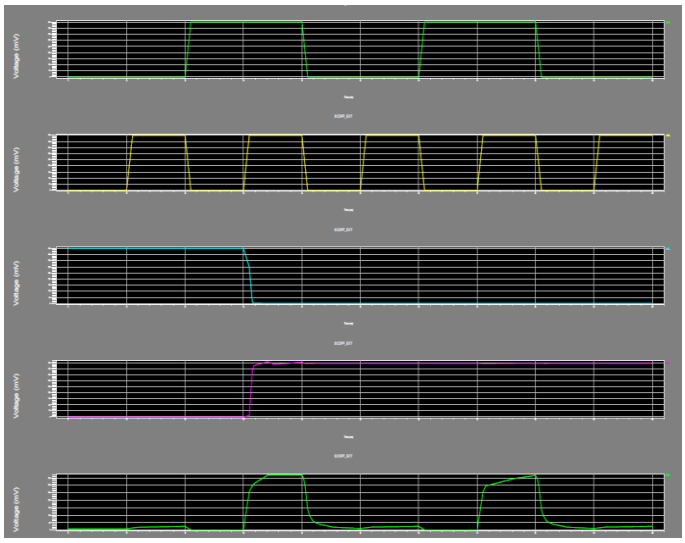

Fig.4 Waveform of Clock gating technique implemented SCDFF

COMPARISION TABLE :

Parameters	Power	Delay	Area
Existing	5.5 µ	10ns	24
Proposed	4.63 µ	0.2s	28

The comparison between the SCDFF and the Static Contention free Differential flip-flop employing the Clock Gating Technique concept is displayed in the above table. Three metrics are compared: area, delay, and power usage. Evidence indicates that SCDFF, which employs GDI-based clock gating, uses less power than Static Differential Flip-Flop. The proposed SCDFF uses more space in terms of area utilization, whereas the GDI-based SCDFF performs better in terms of delay.

V. CONCLUSION

For low-voltage and low-power applications where reliability and power consumption are crucial, a SCDFF is offered. In terms of power consumption, the differential structure is superior to the single-ended construction; however, it lacks reliability while operating at low voltages.The presented design approach emphasizes the new application of clock gating with a GDI-AND and emphasizes the importance of incorporating static contention-free characteristics. The knowledge and understanding acquired from this study advances the design of differential flip-flops and provides useful solutions for increased efficiency and reliability in modern digital systems. Further advancements in flip-flop design approaches are made possible by the contributions of this study, as digital circuits continue to evolve towards greater performance and energy efficiency.

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