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Designing a fully integrated low noise Tunable-Q Active Inductor for RF applications

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***Abstract*— Many architectures of Active Inductors have been proposed until now in literature which exhibiting tuning possibilities, low chip area and offering integration facility, they constitute promising architectures to replace passive inductors in RF circuits. An improved CMOS active inductor topology is proposed in this paper. This paper presents a novel design of CMOS low noise tunable-Q Active Inductor, which is made-up of Gyrator-C network and it uses different topology i.e. modified and regulated modified cascode stage for improving Inductance, frequency range and higher and tunable-Q. And it also includes the feed forward noise reduction path topology to decrease the noise performance of Active Inductor. This active Inductor is made for the applications of RF and microwave circuits. So the typical range of the Inductor is > 1GHz. This active Inductor has been designed in the standard 0.18 µm technology and it is working on 2 – 25GHz as an Inductor with tunable Q value of 45 to 80 at different input bias current is given. The use of feed forward path to reduce the noise is up to 3nV/sqrt (Hz) and the power dissipation of this proposed active inductor is 0.9mW.**

Keywords- RFIC, Active Inductor, Gyrator C network, Quality factor

I. INTRODUCTION

The increasing popularity and growth of wireless communications has inevitably boosted research in the field of radio-frequency integrated circuit (RFIC) design, especially in CMOS technology due to the shrinking of sizes and low cost availability of the process.

The Inductor, an essential component in RF design, finds use in many blocks such as oscillators, filters, phase shifters, low noise amplifiers, impedance matching circuitry, biasing, etc however their implementation still remains to be a challenging task in CMOS. The specifications of Low Noise amplifier must be satisfied simultaneously including, wide bandwidth, large power gain, good impedance matching, good linearity, low power consumption and low cost. In past most of the publications in this field was implemented by using on chip passive spiral inductors to achieve good matching and power gain. An on-chip passive inductor presents major disadvantages such as large silicon area, limited inductance value and low quality factor. And in ICs most of the time, the inductor will be a major factor in determining the total chip area where higher inductance values imply larger area consumption. Furthermore, their values are not precise even if the technology is well-characterized. On the other hand, the Active Inductors offer much less area consumption independent of the desired inductance value, high quality factors and tunability- both with the inductance and the quality factor although the noise performance**,** power consumption and dynamic range will be degraded, it can be maintained at low enough levels for many applications for use in RF and microwave application. Historically, many efforts have been done to replace passive inductors with active circuits [8], [9]. However, because of the poor noise and linearity performance of active inductors, their application in RF has been limited. In this paper, a new Active Inductor designed for specially the low-noise applications like in LNA this active inductor can be implemented in different ways i.e. using the Op-Amp circuit and Gyrator C approach.

This article is organized as follows. First, detail information about the radio frequency IC design need of Active Inductor over passive Inductor and its advantages than a brief overview of gyrator C approach is discussed in Section II. Than in section III and IV is discussing about Quality factor and frequency range at which the circuit will run as Inductor, its dependence on parasitic series as well as parallel resistance and trans-conductance values. After that the section V describes the proposed design of CMOS active Inductor with regulated cascode and feed forward noise reduction path. Section VI explains briefly all simulation results and comparison tables. And finally section VII provides the conclusions.

II. GYRATOR- C ACTIVE INDUCTORS

The basis for the Active Inductor design is a gyrator circuit. The advantage of the gyrator is that it can be implemented on an integrated circuit using transistors. The transistors act as trans-conductors and adjustments to their bias points allow their trans-conductance to be tuned.

A conceptual representation of a gyrator based on two trans-conductors is shown in Figure- 1(Loss Less single ended) which consists of two back-to-back connected trans-conductors and one port of the gyrator is connected to a capacitor, the network is called the gyrator-C network. The Trans-conductor-1 provides a negative trans-conductance g_{m1}, meaning its current flows into the trans-conductor when a positive voltage is applied at its input. The Trans-conductor-2 provides a positive trans-conductance, g_{m2} meaning its current flows out

of the trans-conductor when a positive voltage is applied at its input. There are mainly four types of gyrator C approaches

- Loss-less single ended gyrator-C active Inductor

  Which is loss less and one of the two nodes is either ground or supply voltage V_{DD}.

- Lossless Floating Gyrator-C Active Inductors

  This is lossless and used b/w two different nodes.

- Lossy Single-Ended Gyrator-C Active Inductors :

  Which is when the gyrator-C networks are finite, it will no longer be lossless and it has one end as ground or supply voltage.

- Lossy floating Gyrator-C Active Inductors :

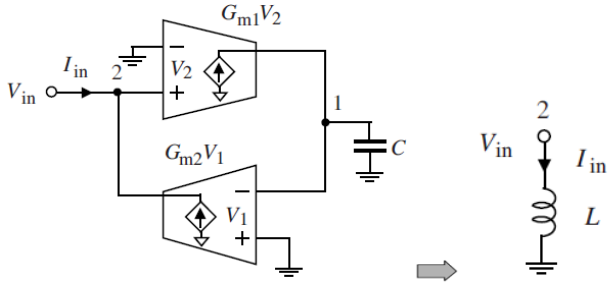

Fig.1. Gyrator – C topology

Here in fig.1 Loss-less single ended gyrator-C active Inductor is given in which looking into port 2 of the gyrator-C network admittance is given by,

$$Y = \frac{Iin}{V2} = \frac{1}{s(\frac{C}{Gm1\ Gm2})} \quad (1)$$

This indicates that port 2 of the gyrator-C network behaves as a single-ended lossless inductor with its inductance given by,

$$L = \frac{C}{Gm1\ Gm2} \quad \text{and} \quad \omega_0 = \frac{1}{LC} \quad (2)$$

Gyrator-C networks can therefore be used to synthesize inductors. These synthesized inductors are called gyrator-C active inductors. The inductance of gyrator-C active inductor is directly proportional to the load capacitance *C* and inversely proportional to the product of the trans-conductance of the trans-conductors of the gyrator. Also, the gyrator-C network is inductive over the entire frequency spectrum. Here in above figure there is an example of loss less or ideal single ended gyrator C network. But in application point of view the Lossy Single-Ended Gyrator-C Active Inductors are mainly used which is as given in figure 2. Which gyrator circuit is equivalent to the RLC circuit which is as given in figure-2.

In Lossy Active Inductor when either the input or the output impedances of the trans-conductors of gyrator-C networks are finite, the synthesized inductors are no longer lossless. Also, the gyrator-C networks are inductive only in a specific frequency range. The admittance looking in to Port-2,

$$Y = sC_2 + G_{o2} + \frac{1}{s\left(\frac{C1}{Gm1\ Gm2}\right) + \frac{Go1}{Gm1\ Gm2}} \quad (3)$$

This equation can be represented by the RLC network shown in fig with its parameter given by,

$$Cp = C_2, \quad Rp = \frac{1}{Go2}, \quad L = \frac{C1}{Gm1\ Gm2}, \quad Rs = \frac{Go1}{Gm1\ Gm2} \quad (4)$$

$$\omega_0 = \frac{1}{LCp} = \sqrt{\frac{Gm1}{C1}\frac{Gm2}{C2}} = \sqrt{\omega_{t1}\omega_{t2}}$$

Where,

$$\omega_{t1,2} = G_{m1,2}/C_{1,2} \quad (5)$$

In which the C_P and R_P is parasitic parallel capacitance and resistance and R_S is parasitic series resistance of an Inductor. The trans-conductors of gyrator-C networks can be configured in various ways, the constraint that the synthesized inductors should have a large frequency range, a low level of power consumption, high-low Q value compatibility and a small silicon area requires that these trans-conductors be configured as simple as possible.

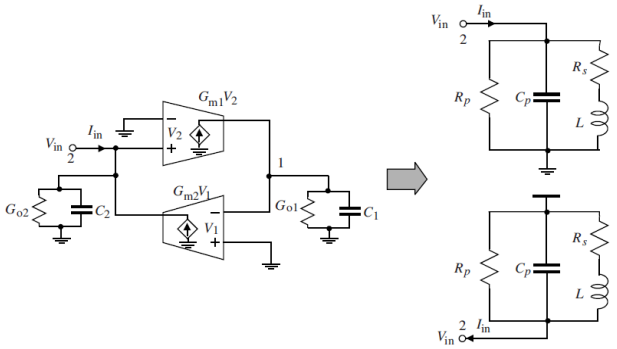

Fig.-2 Lossy single ended gyrator C active Inductor

III. FREQUENCY RANGE

A lossless gyrator-C active inductor exhibits an inductive characteristic across the entire frequency spectrum. A lossy gyrator-C active inductor, however, exhibits an inductive characteristic over a specific frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor,

$$Z = \frac{Rs}{Cp\ L} \frac{S\frac{L}{Rs} + 1}{S^2 + S\left(\frac{1}{Rp\ Cp} + \frac{Rs}{L}\right) + \frac{Rp + Rs}{Rp\ Cp\ L}} \quad (6)$$

When complex conjugate poles are encountered, the pole resonant frequency of *Z* is given by,

$$\omega_P = \sqrt{\frac{Rp + Rs}{Rp\ Cp\ L}} \text{ as always } R_p >> R_s, \quad \omega_P = \sqrt{\frac{1}{L\ Cp}} = \omega_0 \quad (7)$$

Where, ω_o is the self-resonant frequency of the active inductor. Also observe that Z has a zero at frequency,

$$\omega_Z = \frac{Rs}{L} = \frac{Go1}{C1} \quad (8)$$

The gyrator-C network is resistive when $\omega < \omega_Z$, Inductive when $\omega_Z < \omega < \omega_o$, and capacitive when $\omega > \omega_o$. The frequency range in which the gyrator-C network is inductive is

lower-bounded by ω_z and upper-bounded by ω_o. Rp has no effect on the frequency range of the active inductor. Rs, however, affects the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self resonant frequency of the active inductor, which is set by the cut-off frequency of the trans-conductors constituting the active inductor. For a given inductance L, to maximize the frequency range, both Rs and Cp should be minimized.

IV. QUALITY FACTOR

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. For spiral inductors, the quality factor of these inductors is independent of the voltage/current of the inductors. This property does not hold for active Inductors as the inductance of these Active Inductors depends upon the trans-conductance of the trans-conductors constituting the active inductors and the load capacitance. A linear inductor, the complex power of the active inductor is obtained from,

$$P(j\omega) = I(j\omega)\, V^*(j\omega) = RE[Z]\,|I(j\omega)|^2 + j\,IM[Z]\,|I(j\omega)|^2$$

RE[Z] and IM[Z] are the resistance and inductive reactance of the inductor, respectively, V (jω) and I (jω) are the voltage across the inductor and the current through the inductor. The first term in above equation quantifies the net energy loss arising from the parasitic resistances of the inductor, whereas the second term measures the magnetic energy stored in the inductor so,

$$Q = \frac{IM[Z]}{RE[Z]}$$

Considering Z from eq.(6) Q of the inductor will be,

$$Q = \left(\frac{\omega L}{Rs}\right) \frac{Rp}{Rp + Rs + \left[1 + \left(\frac{\omega L}{Rs}\right)^2\right]} \left[1 - \frac{Rs^2\, Cp}{L} - \omega^2 LCp\right] \qquad (9)$$

Here, the first term quantifies the quality factor of the active inductor at low frequencies. The second term accounts for the effect of the finite output impedance of deep sub-micron MOSFETs, whereas the third term shows that the quality factor vanishes when frequency approaches the cut-off frequency of the trans-conductors of the active inductor. The sensitivity of the quality factor of the active inductor is merely depends on Rs and Rp respectively. So to boost the quality factor of active inductors, Rs must be minimized.

$$Q = \omega L / R_S \quad \text{or} \quad Q = R_P / \omega L \qquad (10)$$

V. ACTIVE INDUCTOR IMPLEMENTATION

The basic schematic for a CMOS-based active inductor is shown in figure 2 in which there are two schematic of basic gyrator-C active inductors In Figure 3(a), the trans-conductor with a positive trans-conductance is common gate configured while the trans-conductor with a negative trans-conductance is common-source configured. In Figure 3(b), the trans-conductor with a positive trans-conductance is common-drain configured while the trans-conductor with a negative trans-conductance is common-source configured. All transistors are biased in the saturation and a notable advantage of the active inductor in Fig. is that all transistors are nMOS, making it attractive for high frequency applications. So here for this paper work we have considered the fig.3(b) nMOS topology.

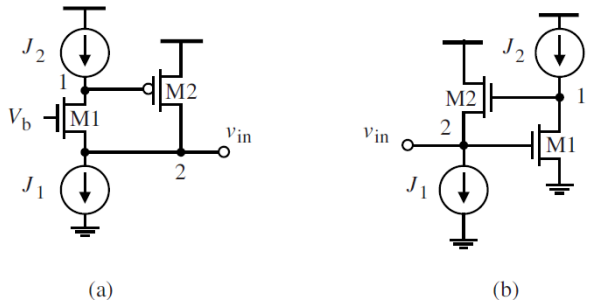

Fig. 3 simplified CMOS-based active inductor.

Where,

$$\text{We have} \quad C_1 = C_{gs2}, \quad G_{O1} \approx g_{O1} = G_{ds}, \quad G_{m1} = g_{m1},$$

$$C_2 = C_{gs1}, \quad G_{o2} \approx gm_1, \text{ and } \quad G_{m2} = g_{m2} \qquad (11)$$

And we obtained the parameters of the equivalent RLC network of the active inductor as,

$$Cp = Cgs1, \qquad Rp = \frac{1}{Gm1}$$

$$L = \frac{Cgs2}{Gm1\ Gm2} \qquad Rs = \frac{Go1}{Gm1\ Gm2} \qquad (12)$$

It is observed from above equation that the parasitic parallel resistance R_P is rather small, limiting the quality factor of the active inductor. Also, the parasitic series resistance is large, further lowering the quality factor. In evaluating the quality factor of this active inductor, the effect of the parasitic series resistance R_s is often neglected as R_P is small. In this case, the quality factor of the active inductor is obtained from eq.(10) to avoid low Q condition R_s should be low and R_P should be high. Similarly to increase the frequency range value of R_s should be low.

So a new proposed schematic of CMOS active inductor is shown in figure.4 which consists of base gyrator circuit with feedback resistor R_{f1} and regulated cascode stage with the use of feed forward noise reduction path.

In this proposed circuit we have added a feedback resistor between the two trans-conductors of the active inductor or say two nMOS of Fig.3 circuit to improve the quality factor of the inductor, The added feedback resistor increases the inductance of the active inductor and at the same time lowers the parasitic series resistance R_S of the active inductor, thereby boosting the quality factor of the active inductor. Transistor M_3 reduces output conductance of M_1 thus increase in the frequency range of inductive operation (because of (10)). And also reduction in parasitic series resistance so inductive Q value will be increase. So the inductive Q value is related to cascode gain of M_3. So, Inductor loss can be reduced (i.e. increase Q) by increasing the cascode gain, that can be done by adding more transistor. But stacking more transistors is undesirable as it will introduce additional poles and zeros in to signal path. An

alternative method to increase the cascode gain is to use feedback amplifier to regulate the gain of M_3. A regulated and multi-regulated cascode technology is based on increasing the cascode effect by adding the additional regulated gain stages.

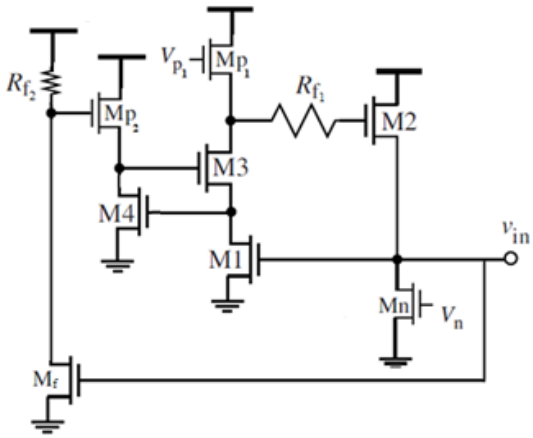

Fig.4 Proposed Regulated cascode Active Inductor

A regulated cascode stage can be implemented by a simple inverter gain stage M_4. If regulated amplifier itself cascode gain stage (M_4 and M_5) repetitively applied to implement multi-regulated cascode stage as in fig.5. Addition of these regulated stages doesn't degrade the high frequency response of the inductor because the signal path is still M_1 M_2 and M_3. However the cascode gain can now be controlled. Hence, the Q value of inductor can independently tuned. This regulated and modified regulated cascode stage shifts zeros value to even lower frequency independently by varying the current source at M_{P2}. Thus improving the response of inductor this cascode stages achieves bandwidth of over three decades. In order to improve the noise performance of the Active Inductor we added a feed-forward path (FFP) to the bias input, the FFP comprising the common source transistor M_F and its resistive load R_F s given in figure

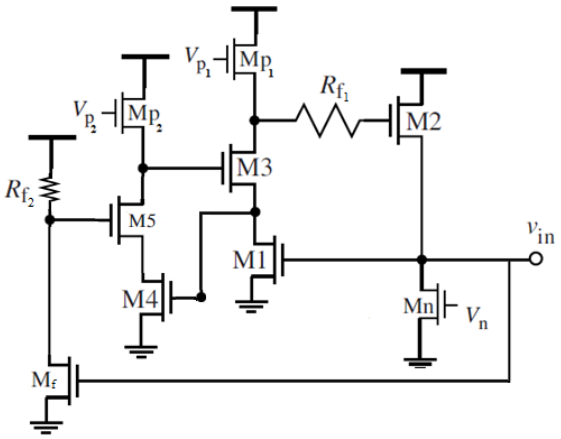

Fig.5 CMOS multi-regulated cascode Active Inductor

The input noise current of an Active Inductor of fig.4 RLC circuit can be calculated as,

$$\overline{i_{n,in}^2} = 4kT\gamma \left(\frac{1}{g_{m1}(L\omega)^2} + g_{m3}\right) \quad (13)$$

Comparing the noise currents generated by the regulated cascode CMOS Active Inductor without and with FFP.

$$\overline{i_{n,out}^2} = 4kT\gamma\, g_{m1} \quad \text{(Without FFP)}$$

$$\overline{i_{n,out}^2} = 4kT\gamma\, g_{m1} + 4kT\gamma \left(\frac{a_f\left(a_f + \frac{1}{\gamma}\right)g_{m1}^{\,2}}{g_{mf}}\right) \quad \text{(With FFP)}$$

Where, (14)

$$a_f = g_{mf} * R_f$$

VI. SIMMULATIONS AND RESULTS

The proposed design of an Active Inductor circuit which given in fig.4 is designed using 0.18μm CMOS technology in mentor graphics design architect tool with a power supply voltage of 1.8V and it is simulated to verify its results of Active Inductor with feed forward loop. The power dissipation without feed forward loop we got is 0.9mW and with FFL it is 1.05mW. The output which we got as waveform had been plotted in EZWave which is used with mentor graphic tool. It is evident from fig.6 that the current phase shift we got which is almost negative 90° to 94° within the frequency range of 2GHz to 25GHz which is when the voltage phase shift we have considered 0°, it describes active inductor circuit, is inductive within that particular range. Now the value of quality factor Q of the Inductor is totally depends on the trans-conductance and output resistance of the transistor M_3 and M_4 as if we use regulated cascode, and the value of Q is in the range of 50-100 within the frequency range of 1–3 GHz and if we use multi regulated cascode given in fig.5 one more transistor M_5 which more increases the value of Q which we can get in range of thousands. Now here as the value of R_f changes the Q will be change. So by tuning the value of resistance or can say input bias current the Q can be changed. Fig.7 describes the value of Q with respect to frequency the Quality factor Q is varying between values 50 to 80.

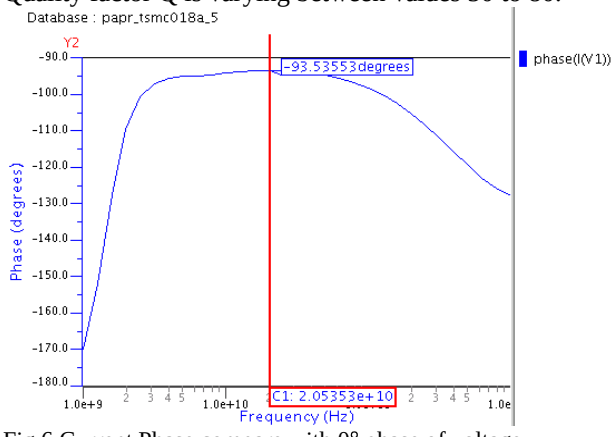

Fig.6 Current Phase compare with 0° phase of voltage.

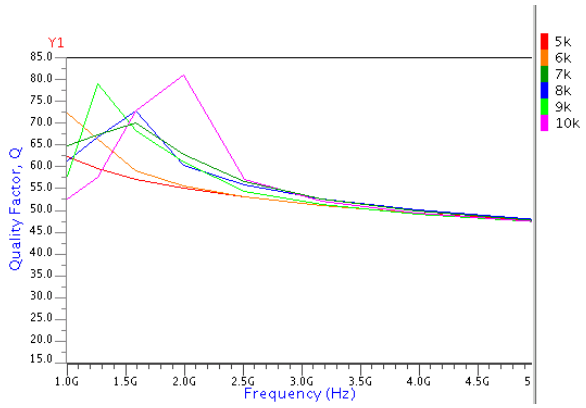

Fig.7 Q factor vs. frequency as different values of R_F

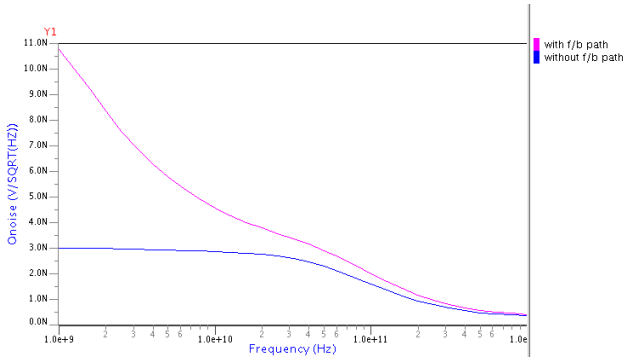

Fig.8 noise of an AI with and without feed forward path.

Now, using the feed forward loop the noise of an active inductor can be reduce theoretical with using equation (13) (14). Here in this section fig.8 gives the difference of noise with and without feed forward path which gives reduced noise at less than or equal to 3nV/sqrt (Hz).

CONCLUSION

The design and implementation of low noise high Q tunable active inductor in 0.18 μm CMOS technology have been introduced. Measured result shows that within the range of 1–3 GHz frequency range, Q can be tuned within the value 50-85. And using the feed forward topology the noise of the active Inductor can be optimized which have been proved in result section. So using feed forward topology the noise decreased to 3nV/sqrt (Hz). The total power dissipation of the active inductor circuit with multi-regulated cascode topology is 1.05mW and with regulated cascode technology it is 0.9mW. This means if we want to increase the Quality factor value the bandwidth will decrease and comparatively more power consumption will be there.

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