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Designing a XOR Gate Circuit based on Floating Gate and Quasi-Floating Gate

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***Abstract*- Nowadays important parameter in designing analog and digital circuits is reducing power consumption of the circuit. In analog and digital circuit power dissipation is given by $P=CfV^2$ which shows power is directly proportional to square of voltage. So power consumption can be decreased by reducing the voltage supply. Another importance of low voltage is that circuits are easy to transport because the small battery is used as the voltage supply on them.**

Keywords: CMOS, low voltage, floating gate, quasi floating gate, power consumption, PSPICE.

I. INTRODUCTION

The CMOS digital circuits with very low power consumption and high operating speed have always been the focus of the design criteria. Since there is always a trade-off between power dissipation and time delay in digital circuits, so reducing the power dissipation and still maintaining the high performance of circuits in terms of speed is important in digital designs. There is a need for new design techniques for optimum performance of devices to be operated at sub-volt supplies and consuming very low power with the continuous reduction of their dimensions. The power supply reduction is must with scaling down of devices but it happens at the expense of speed. Since the performance of circuits can be altered with tuning of threshold voltage of transistors, therefore FGMOS has been abundantly employed to enhance the performance of mixed mode low voltage circuits despite their inherent limitations like reduced gain-bandwidth product and large chip area due to the need of large biasing capacitance. The use of Quasi-floating gate MOSFET (QFGMOS) can further enhance the performance of circuits in terms of high speed and low power dissipation as compared to FGMOS. It is because of the fact that QFGMOS doesn't need a large biasing capacitance as its gate is feebly connected to supply voltage through a large value resistor.

II. FLOATING-GATE MOS TRANSISTOR

The first appearance of floating–gate technique was in 1967. In the late 1980s, the Intel ETANN chip employed it as an analog nonvolatile memory element. From that date, floating–gate devices are finding wider applications by analog researchers. A number of papers have been reported in the literature for applications of floating–gate technique in analog circuits, such as floating gate CMOS analog trimming circuits , neural network components, multipliers , D/A converters , amplifiers, operational transconductance amplifiers , and differential voltage current conveyors .

These devices can be fabricated in all CMOS technologies, but a double poly CMOS technology is preferred. In FGMOS, the gate is fabricated using the gate electrode (poly1) layer and is surrounded by two SiO2 insulator layers thus electrically isolated from the rest of the device.

The device inputs are placed on top of the upper SiO2 insulating layer and are fabricated using another conducting layer, preferably a second layer of polysilicon (poly2). Thus, from the dc operating point of view, the gate is floating node, and that is why the MOS is called floating–gate MOS. Inputs are capacitively coupled to the FG, and the sizes of the input electrodes determine the values of the capacitors, which can be varied according to the designer's needs. The circuit symbol, equivalent circuit, layout, and cross–section of a two– input floating gate NMOS are shown in Fig.1.

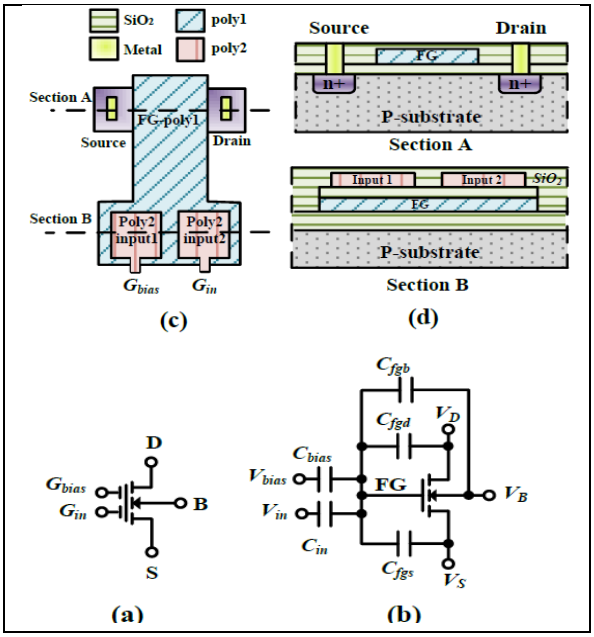

Fig 1: Two-input floating-gate NMOS: (a) symbol, (b) equivalent circuit, (c)layout and (d) cross section

Cfgd, *Cfgs*, and *Cfgb* denote the parasitic capacitances from gate to drain, source, and bulk,

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$$C_{Total} = C_{fgd} + C_{fgs} + C_{fgb} + \sum_{i=1}^{n} C_{Gi}$$

respectively, *CGi* is the coupling capacitance of the ith input branch, the term C_{TOTAL} refers to the total capacitance seen by the FG and is given by:

Assuming zero initial charge and neglecting parasitic capacitances as compared to *Cbias* and *Cin*, the gate voltage of MOS

$$V_{FG} \approx k_1 V_{in} + k_2 V_{bias},$$

$$\text{where } k_1 = \frac{C_{bias}}{C_{Total}} \text{ and } k_2 = \frac{C_{in}}{C_{Total}}.$$

The equivalent threshold voltage for the MOS adjusts itself

$$V_{T,eq} = \frac{V_T - V_{bias} k_1}{k_2}.$$

to a new value *VT,eq*

The transition frequency equation of FG MOS

$$f_{T,FG} = \frac{g_m}{2\pi(C_{bias} + C_{fgs})}$$

It is clear that the transition frequency of FG MOS is smaller than the transition frequency of GD MOS; hence FG MOS has smaller bandwidth than conventional MOSFET.

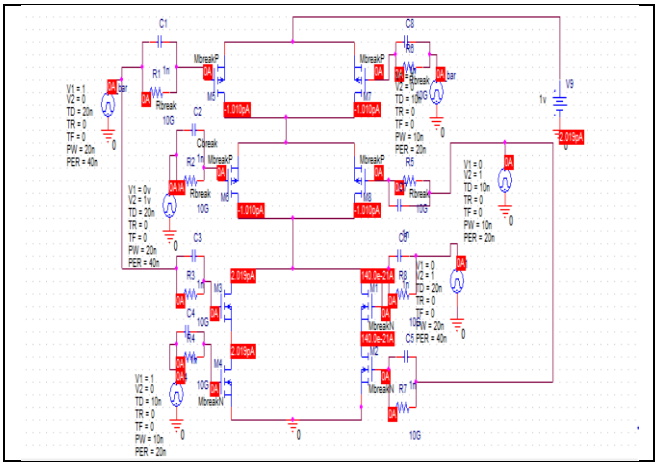

Fig 2: XOR gate using FGMOS technique

III. QUASI–FLOATING–GATE

To overcome the main problems of the floating–gate MOS, namely the initial charge trapped in the floating gate problem and the large silicon area problem, a quasi–floating–gate MOS (or pseudo–floating–gate MOS) is an appropriate solution. Applications based on QFGMOS include: differential operational amplifiers, transconductors, current mirrors, filters, current conveyors, and linear MOS resistors.

Floating–gate MOSs use voltage dividers with relatively large attenuation factors at the transistor gates to reduce supply requirements. The dividers use large capacitance to set the floating gate DC voltage close to one of the supply rails. Unfortunately, this large capacitance leads to an increase in silicon area and a reduction of the effective transconductance and gain–bandwidth product (GBW). Besides, as mentioned before, some technique is required to avoid the initial charge trapped in the floating gate.

All these issues are solved by weakly connecting the floating gate to a proper DC voltage using a large–valued resistor which can be implemented by the leakage resistance of a reverse–biased junction of a diode–connected MOS transistor operating in cutoff region. Therefore, this pull–up or pull–down resistor *Rleak* sets the DC gate voltage to a power rail, thus preventing initial charge issues and simultaneously minimizing the supply voltage requirements.

The large resistance value employed makes the gate effectively floating from signal frequencies of above 0.05 Hz so that AC operation is unaffected even for very low frequencies. At the same time, GBW degradation effects are avoided since a large biasing capacitor is no longer required.

The symbol of single input terminal QFG MOS (a), its equivalent circuit (b) and layout (c) are shown in Fig. 3. The input terminals are capacitively coupled to the quasi–floating gate, but the DC gate voltage is set to *Vbias* without requiring a large capacitor.

The pull–up or pull–down resistor can be implemented in practice by the large (and nonlinear) leakage resistance of reverse–biased p–n junction of MOS transistor operating in cutoff region, as shown in Fig. 3. This fact leads to significant savings in terms of area compared to the MIFG device.

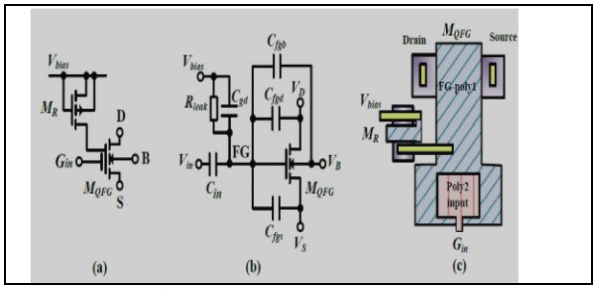

Fig 3: One-input-floating gate NMOS: (a) symbol, (b) its equivalent circuit and(c) layout

Cfgd, *Cfgs* and *Cfgb* denote the parasitic capacitances from gate to drain, source, and bulk respectively, *Ck* is the coupling capacitance of the kth input branch, and C_{TOTAL} is the total capacitance and is given by:

$$C_{Total} = C_{gd} + C_{fgd} + C_{fgs} + C_{fgb} + \sum_{k=1}^{n} C_k$$

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Due to a large value of *Rleak*, even at low frequencies. A simple analysis reveals that the AC voltage at the floating gate is given by

$$V_{QFG} = \frac{1}{C_{Total}} \times (C_{fgd} V_D + C_{fgs} V_S + C_{fgb} V_B + \sum_{k=1}^{n} C_k V_k)$$

The transition frequency can be expressed by

$$f_{T,QFG} = \frac{g_m}{2\pi(C_{fgs} + C_{gd})}$$

The input referred noise of QFG MOST is smaller than it of FG MOST, since C_{TOTAL}, *QFG* <C_{TOTAL}, *FG*.

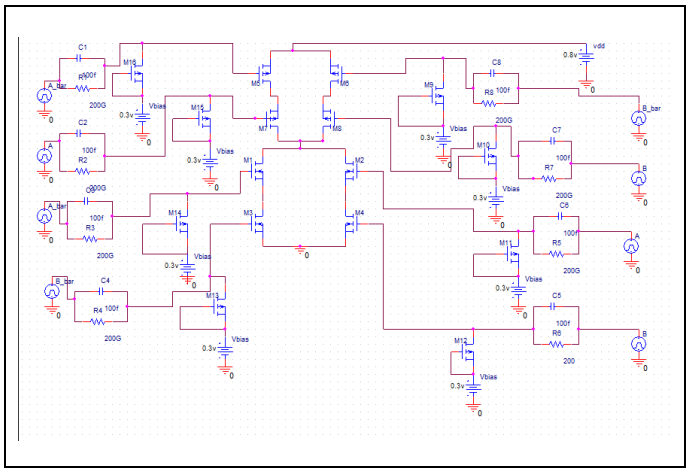

Fig 4: XOR Gate Using Quasi Floating Gate Technique

IV. SIMULATION RESULTS

The performance of the FGMOSFET and QGMOSFET was verified by PSpice simulations with supply voltage 0.8V using 0.35um CMOS technology parameters.

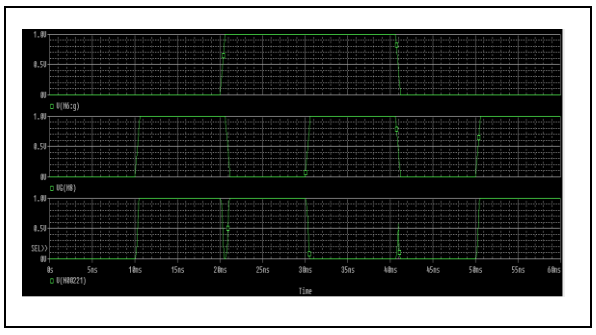

Fig 5: Transient analysis of FGMOS XOR gate

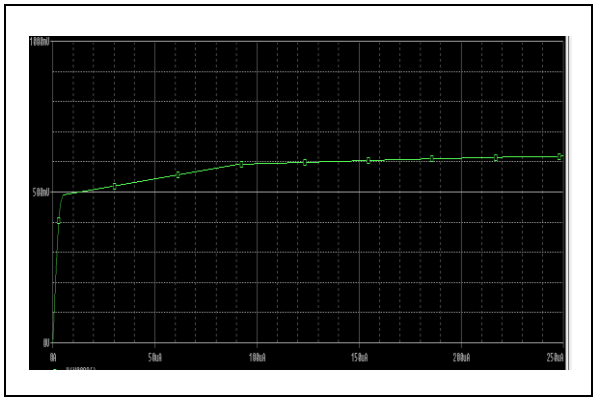

Fig 6: Output current Vs applied voltage

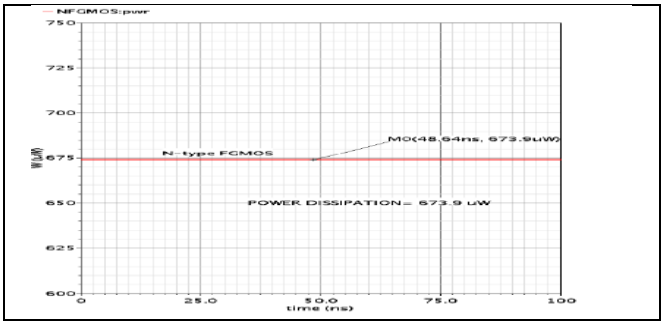

Fig 7: Power Dissipation FGMOS XOR gate

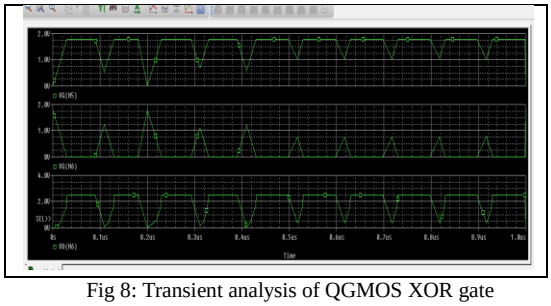

Fig 8: Transient analysis of QGMOS XOR gate

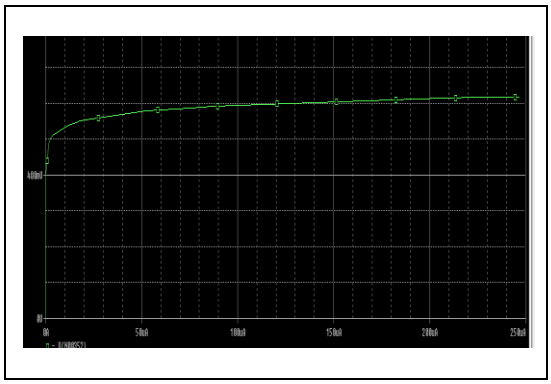

Fig 9: Output current Vs applied voltage in QGMOS

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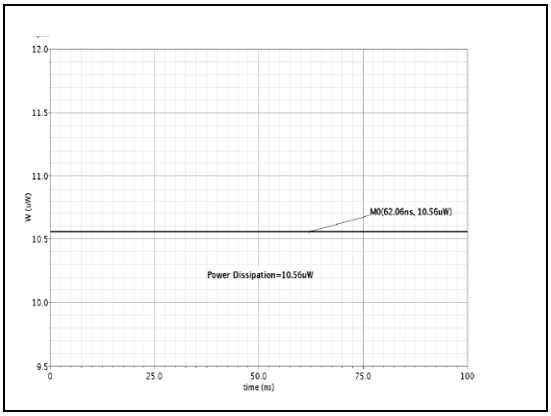

Fig 10: Power Dissipation in QGMOS XOR gate

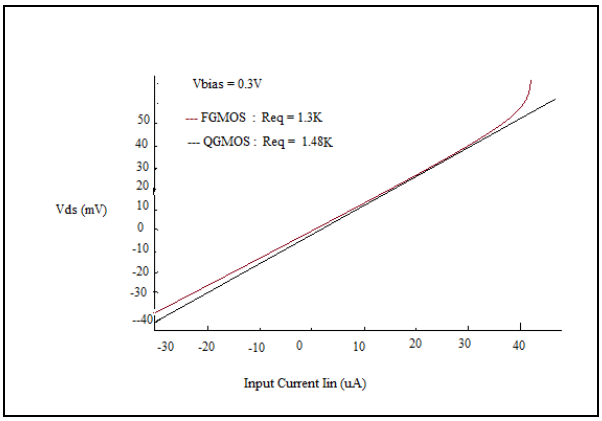

Fig 11: Comparative resistance simulation characteristics

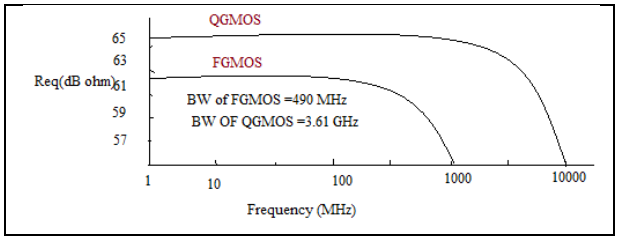

Fig 12: Comparative frequency response of QGMOS and FGMOS

The simulation has been implemented using two different techniques i.e. Floating gate and Quasi Floating gate. It can be seen from figure[6] and [9] that QGMOS and FGMOS technique require less voltage for operation .The comparative resistance simulation characteristics of VCR based on FGMOS and QGMOS shown in Figure [11] R_{eq} for FGMOS IS 1.30Kohm whereas it is 1.48Kohm for QGMOS-based XOR gate. The comparative frequency response of QGMOS and FGMOS based XOR gate is shown in Figure [14].The bandwidth of QGMOS-based XOR gate is found to be 3.62GHz, which is greater than that of FGMOS based XOR gate due to absence of large capacitance. From table [1] it can be seen that power dissipation for QGMOS technique is less as compared to FGMOS and power delay product of QGMOS based XOR gate is less as compared to FGMOS based XOR gate. As a consequence, QGMOS circuits are a better choice for being used in supply voltages in which the circuit involves threshold voltage, also these circuits on the basis of power dissipation are recommended to be used in this situation. Modern methods are recommenced to design Quasi floating gate circuits by which we could take advantages of floating gate technology while the disadvantages would be decreased.

Table1. Comparison of XOR gate with FGMOS and QGMOS technique

	Propagation Delay (n sec)	Power Dissipation(mWatt)	PDP (p-Watt)	R_{eq}(K ohm)	BW(M Hz)
XOR gate using FGMOS	0.490	673.9	330.21	1.30	490
XOR gate using QGMOS	0.530	10.56	5.59	1.48	3610

V. CONCLUSIONS

In this paper, we have briefly described FGMOS and QGMOS and used it to implement a XOR gate. The characteristics of QGMOS-based XOR gate is compared with those of FGMOS counterpart. It was found that QGMOS simulates a higher value of resistance, offers lager bandwidth as compared to FMOS version due to its inherent advantage and consumption of less power. The Pspice simulation results were found to be in conformity with the theory.

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