

Designing of High Frequency Analog Filter using 45nm CMOS based CCII

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Abstract— In VLSI, the design techniques are usually in voltage mode but several limitations are encountered like narrower bandwidth, lower linearity, high consumption of power, lesser gain and so on. We know the power consumption of any circuit is related to the product of the biasing voltage and current and, if we focus on current signal rather than the voltage signal, an effective and better control over the power is observed. So, current mode circuits like current conveyors are getting prominent consideration in the analog IC designs due to their broader bandwidth, higher flexibility, large dynamic range, low consumption of power and less area and hence more speed. In this paper a second generation current conveyor is designed and analyzed in the Cadence Spectra. Various analysis have been done for the design like transient and AC analysis. All the responses were realized in 45nm CMOS technology and simulated using Cadence (Virtuoso).

Keywords— Transient; Bandwidth; Cadence; CCII \pm ; Current mirror; Current mode

I. INTRODUCTION

Majority of the analog circuits are in voltage mode whose performance are evaluated in terms of voltage level [1]. But the major limitations of these circuits are like need for high supply voltage, decreased slew rate, and so on. They are also unsuitable when used in high frequency applications, thus restraining the bandwidth of the circuit [2]. However, a MOSFET based current conveyor circuit seems to be a better approach for analog VLSI regime. MOS devices have the power to efficiently process current over voltage because in both the amplifier configurations i.e. the common-source (CS) and the common-gate (CG), current is the desired output. The common-drain (CD) configuration of the amplifier gives voltage which has the disadvantage of a bulk-effect present in the CMOS processes. The current conveyors (CCIs) based on MOS transistors serves a good building block as it is capable of showing better performance in comparison to the previous designed operational amplifiers and they also act more or less equal to an op-amp and as a result it comes as an efficient and better replacement in the true real sense. The current conveyor (CCI) has some extra merits such as simple design, increased slew rate, higher bandwidth and small propagation delay. Such a current conveyor comprises one high input impedance and one low input impedance and also one high output impedance which make it favorable for both the voltage and current mode designs [3]. Many researchers have reported so many current conveyor circuits such as DDCC, CCCII, CDTA, so on, in the literature [4, 5]. Most of the circuits such as rectifiers, oscillators, filters, etc. have been analyzed using various types of current conveyors. The circuits which have been made using current conveyors gives impressive response showing broader

bandwidth, lower power consumption etc. So the researchers are being attracted towards the current conveyors for designing of various amplifier circuits. In this work, the introduction is discussed under section I. Section II gives a brief idea about all the types of current conveyors like first generation, second generation, and third generation i.e. how they work, node-matrix relationship between the input and the output. Section III sheds light on how the CCII is designed followed by its design and the matrix relations. Section III also deals with the various analysis of CCII done in the Cadence Spectra i.e. AC response and transient response. The simulation results have been shown in the same section. Lastly, the paper is ended by a conclusion followed by references.

II. TYPES OF CURRENT CONVEYOR

A. First generation current conveyor CCI

The CCI is mainly a three-terminal device marked as X, Y, and Z. The X end potential equals whatever voltage is being applied to the Y end. The current that flows into Y end also flows into X, and the same current is mirrored at Z end with a high output impedance, thus acting as a variable constant current source.

B. Second generation current conveyor CCII

The CCII can be realised as an ideal transistor, with perfect ideal characteristics. The current that flows into the gate or base (Y) is zero. There is negligible base-emitter or gate-source potential drop, so the source/emitter voltage (at X) equals the voltage at Y. The gate/base (Y) has an infinite input impedance, while the emitter/source (X) has a zero input impedance. Any amount of current out of the emitter or source (X) is mirrored at the collector or drain (Z) as current in, but with a very large impedance at the output.

C. Third generation current conveyor CCIII

The last but not the least configuration of the current conveyor is similar to the CCI, but here the current flowing into X terminal is reversed, so in a CCIII the current which flows into the Y terminal also flows out of X terminal.

III. SECOND GENERATION CURRENT CONVEYOR

A second generation current conveyor is easier to design since it does not need any highly accurate component and follows the principle of comparative biasing supply thus leading to the design and realises various applications like filter, rectifiers, etc. Fig. 1 depicts the block diagram of a typical CCII, where the terminal X is the low input impedance terminal, Y is the high input impedance terminal and Z+ and Z- are the desired in-phase and out-phase terminals of the current conveyor respectively [1, 2].

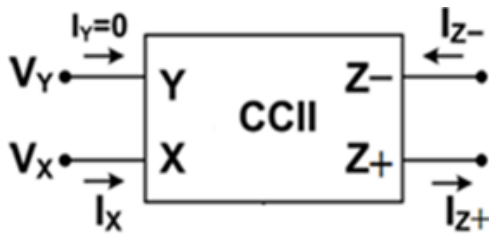


Fig. 1. Block diagram of a typical CCII

In Fig. 1, the Y terminal experiences infinite (very large) input impedance. The voltage at the X terminal follows the voltage that is applied to the terminal Y, thus making the terminal X exhibit zero impedance at the input. The input current to X terminal is conveyed or carried to the high impedance output terminal Z where it is supplied with either of the polarities, positive (CCII+) or negative (CCII-). The dependency between the currents and the voltages at the respective output input ports of CCII is shown in the following matrix:

$$\begin{bmatrix} 0 & 0 & I_y \\ 0 & 0 & V_x \\ 0 & 0 & I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \quad (1)$$

A. Design Approach of CCII

The simplicity in the design and structure of CCII helps it to possess a generalized nature, and therefore can be used as a prototype in the design of large amplifier systems. The transistor level circuit design of CCII± is given in Fig. 2.

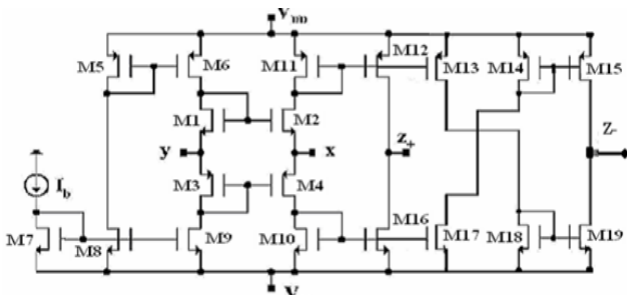


Fig. 2. Transistor level circuit diagram of CCII

The above circuit of CCII shown in Fig.2 comprises one input cell which has a mixed trans-linear loop (M1 to M4), a pair of current mirrors (M5, M6 and M8, M9) which permit us to produce reliable current at the output as the mirror of the current in the input of the circuit and also do allow the trans-linear loop with the help of current I_B [6, 7] to be dc biased. The MOS transistors M₆, M₁₁, M₁, M₂, M₃, M₄, M₉ and M₁₀ form a Trans-linear push-pull type output structure, which is symmetrical as well as balanced. This symmetry helps in alleviating many problems like channel-length modulation, temperature mismatch, and so on. For the production of the out of phase output, two MOS based current mirror circuits are cross coupled. In Fig.2, '+' sign means that the direction of current I_Z is the same as shown, '-' stands for the opposite direction of I_Z with respect to I_X. Terminal 'Y' is the node where voltage is controlled with negligible current. When looking into the

terminal, the impedance is ideally null. The current I_Z don't depend on the V_x. In this work, the CCII± circuit design shown in Fig. 2 is taken into use and is implemented in 45nm CMOS technology using Cadence Spectre (virtuoso).

B. Design analysis of CCII

The CCII Circuit shown in Fig. 2 is designed using Cadence by taking W/L ratio as 2/1. The circuit diagram is implemented in spectra as shown in Fig. 3, which serves as a strong active element. By running the transient and AC analysis, the performance of the circuit has been verified.

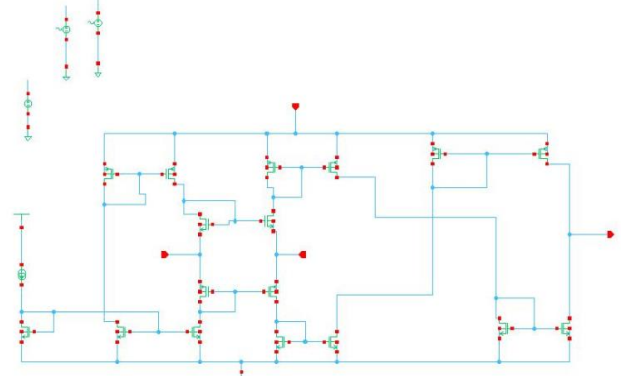


Fig. 3. Circuit diagram of CCII implemented in gpdK 045nm

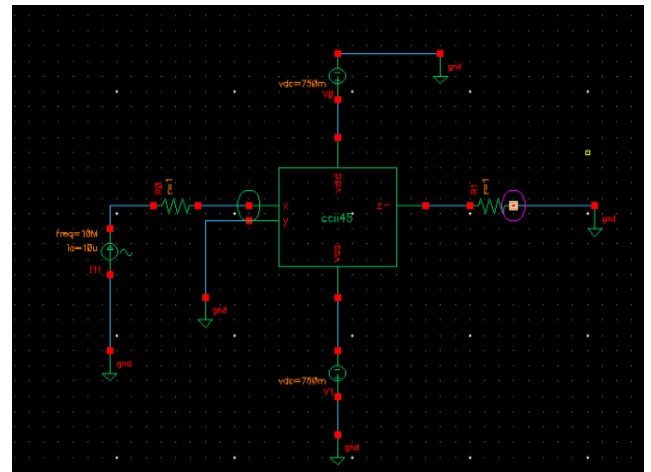


Fig. 4. Symbolic test diagram of CCII in gpdK 045nm

1) Transient Analysis

Transient analysis has been simulated by taking a sinusoidal input of frequency 1 MHz (Fig.5) & 10 MHz (Fig.6) shows the transient response for the CCII block implemented in Cadence using 45nm technology. It can be inferred that the output at Z- terminal is out of phase compared to the input at X terminal thus satisfying the Equation (1) cited above.

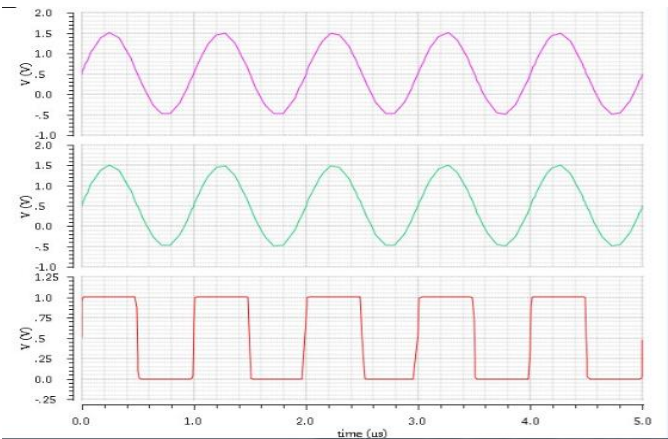


Fig. 5. Transient response of CCII circuit for 1 MHz

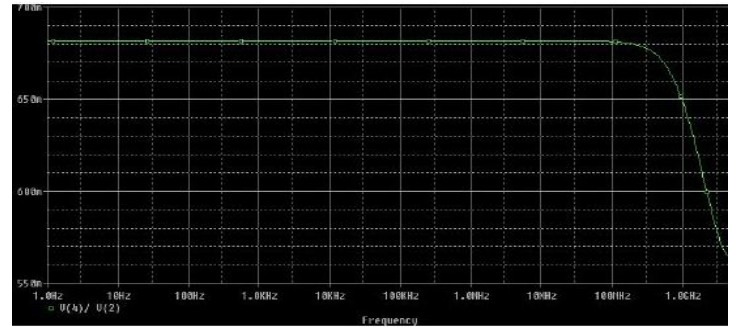


Fig. 8. Frequency response of voltage gain at 0.45nm

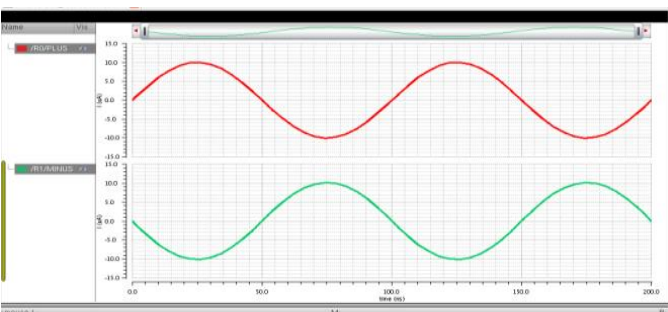


Fig. 6. Transient response of CCII circuit for 10MHz

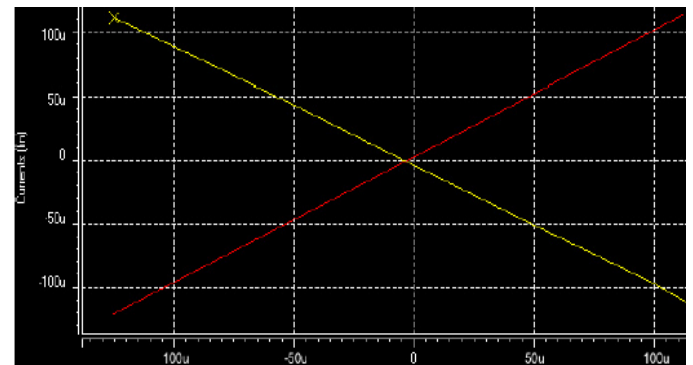


Fig. 9. Current I/O characteristics at 0.45nm

In Fig.5, the wave on the upper side (R1) is the input supplied at the input terminal X and the wave (R0) is the desired out of phase output provided to the input, measured at Z- terminal.

2) Ac Analysis

Fig.7 is showing the AC response of the CCII circuit block designed in Cadence. AC analysis provides excellent conformity between input and output up to 10 GHz according to the Equation (1).



Fig. 7. A.c response of CCII circuit for 10 GHz

In Fig.6 the wave for (I₀) is the input provided and the wave for (R₁) shows the AC (3db) response corresponding to the input provided. Hence the CCII block made is suitable for high frequency applications.

IV. ANALOG FILTER

Active filters are one of the most popular analog filters as they have a significant advantage that they do not contain any inductors, and hence reducing the problems associated with it and also the general filters responses i.e. low-pass, band-pass and high-pass can be obtained accurately[8-11]. A current mode active filter is implemented using a single CCII of Fig. 1, two resistors and two capacitors. The block diagram of the proposed filter is shown in Fig. 10. The filter designed using cadence is shown in Fig.11.

$$I_{R1} = \frac{s.C1.R1.R2.li}{s^2.C1.C2.R1.R2+s.C1.(R1+R2)+1} \quad (2)$$

$$I_{C2} = \frac{s^2.C1.C2.R1.R2.li}{s^2.C1.C2.R1.R2+s.C1.(R1+R2)+1} \quad (3)$$

The quality factor Q and angular frequency ω_0 are given by the following expressions.

$$Q = \frac{1}{R1+R2} \sqrt{\left(\frac{C2.R1.R2}{C1}\right)} \quad (4)$$

$$\omega_0 = \frac{1}{\sqrt{(C1.C2.R1.R2)}} \quad (5)$$

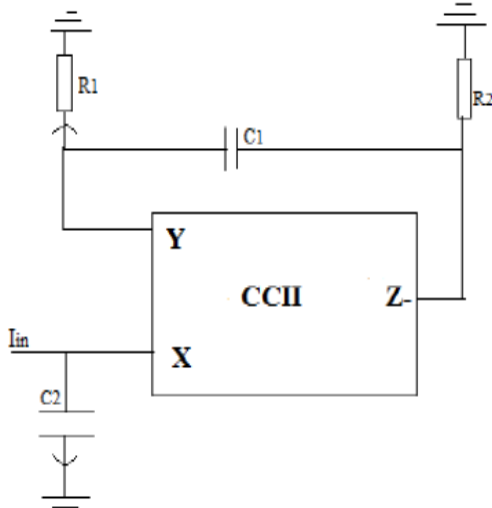


Fig. 10. Block of proposed analog filter.

V. SIMULATION RESULTS

The optimized results of the circuit implemented as shown in Fig.8 are obtained for the following values of the passive components; $R_1=20K\Omega$, $R_2=40\Omega$, $C_1=2f$ and $C_2=20f$. The biasing current is chosen to be $10\mu A$ and the power supplies are selected to be $\pm 0.75V$. The low-pass, band-pass and high-pass response of the filter designed is shown in Fig. 12,13 respectively.

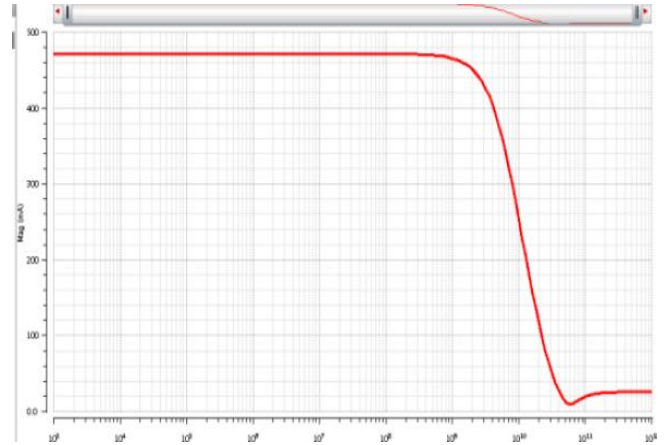


Fig. 12. Response curve of Low pass filter

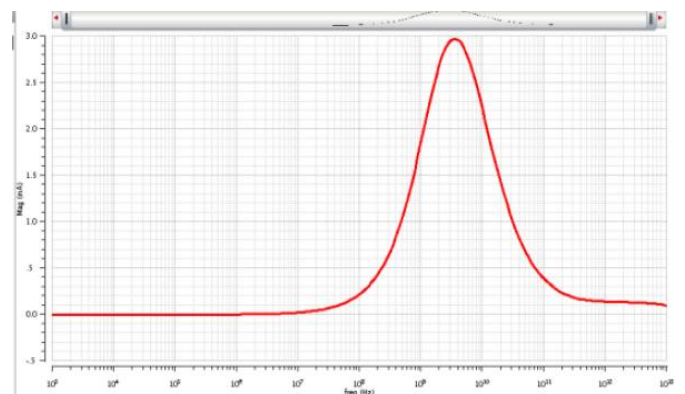


Fig. 13. Response curve of Band pass filter.

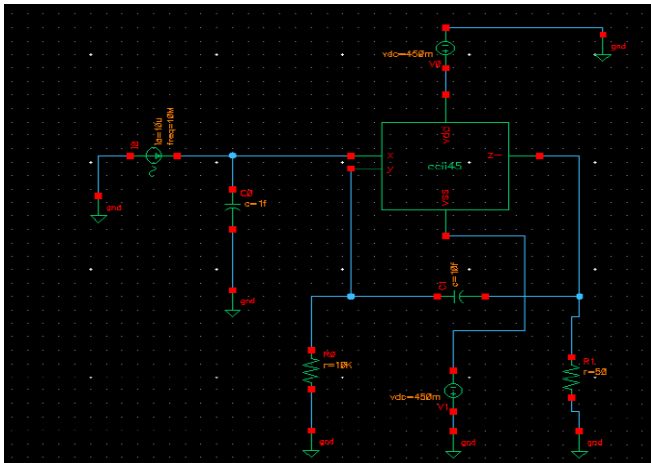


Fig. 11. Analogy filter design in gpdk045nm

TABLE 1: Comparison Table

	[9]	[10]	Proposed
Technology	CMOS	CMOS	CMOS
Technology node	180nm	500nm	45nm
No. of resistor	1	4	1
No. of active element	2	2	1
No. of capacitor	1	2	1
Type of active element	CCII±	CCII±	CCII-

CONCLUSION

The CCII is analysed and simulated for pre layout and post layout designs. It has very good gain and higher bandwidth. Also it needs low voltage has low power consumption. Here current gain can be increased by improving the trans-impedance at the X and Z terminals. Voltage gain may be improved by modifying the various topologies. After analyzing the results, it is assured that the circuits based on current mode give improved performance in low voltage low power applications when compared to circuits using voltage mode. The components values used in the simulation are $R_1=20 K$, $R_2=40\Omega$, $C_1=2f$. The circuit has a single current conveyor as an active block. Transient analysis has been performed that proves the relation between the input current I_X and output current I_Z . AC analysis reveals a very good conformity between input and output up to 10 GHz. The bandwidth of the B.P.F. is 1.34 MHz to 10.19 GHz & for L.P.F. cut-off frequency is 5.54 GHz & 28.198 GHz. Basically current conveyor can be used for various circuits such as, oscillator, function generator, rectifiers etc.

ACKNOWLEDGEMENT

I want to thank my Supervisor Dr. Vinay Kumar for is constant help and encouragement in doing this work .I also want to thank my parents and my friends for their constant support.

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