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Designing of VLSI Circuits with MOS and CMOS

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Abstract

In this paper discussed the development and design of VLSI. Modern day computers are getting smaller, faster, and cheaper and more power efficient every progressing second. The transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. There are two types of MOS transistors pMOS and nMOS. CMOS technology uses both MOS transistors. CMOS processing steps can be broadly divided into two parts. Transistors are formed in the Front-End-of-Line (FEOL) phase, while wires are built in the Back-End-of-Line (BEOL) phase.

Index terms*: IC, SSI, TTL, MSL, VLSI, CMOS, MOS, ULSI and MOSFET.*

1. Introduction

In the early days when huge computers made of vacuum tubes sat humming in entire dedicated rooms and could do about 360 multiplications of 10 digit numbers in a second. Modern day computers are getting smaller, faster, and cheaper and more power efficient every progressing second. But what drove this change? The whole domain of computing ushered into a new dawn of electronic miniaturization with the advent of semiconductor transistor by Bardeen (1947-48) and then the Bipolar Transistor by Shockley (1949) in the Bell Laboratory.

Since the invention of the first IC (Integrated Circuit) in the form of a Flip Flop by Jack Kilby in 1958, our ability to pack more and more transistors onto a single chip has doubled roughly every 18 months, in accordance with the Moore's Law [1].

The development of micro electronics spans a time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60's saw the low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60's when around 100 transistors could be placed on a single chip.

It was the time when the cost of research began to decline and private firms started entering the competition in contrast to the earlier years where the main burden was borne by the military. Transistor-Transistor logic (TTL) offering higher integration densities outlasted other IC families like ECL and became the basis of the first integrated circuit revolution [2]. It was the production of this family that gave impetus to semiconductor giants like Texas Instruments, Fairchild and National Semiconductors. Early seventies marked the growth of transistor count to about 1000 per chip called the Large Scale Integration.

By mid eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. Though many improvements have been made and the transistor count is still rising, further names of generations like ULSI are generally avoided. It was during this time when TTL lost the battle to MOS family owing to the same problems that had pushed vacuum tubes into negligence, power dissipation and the limit it imposed on the number of gates that could be placed on a single die [3].

The second age of Integrated Circuits(IC's) revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974. Today many companies like Texas Instruments, Infineon, Alliance Semiconductors, Cadence, Synopsys, Celox Networks, Cisco, Micron Tech, National Semiconductors, ST Microelectronics, Qualcomm, Lucent, Mentor Graphics, Analog Devices, Intel, Philips, Motorola and many other firms have been established and are dedicated to the various fields in "VLSI" like Programmable Logic Devices, Hardware Descriptive Languages, Design tools, Embedded Systems etc.

T-R-A-N-S-I-S-T-O-R = TRANsfer resiSTOR
1947: John Bardeen, Walter Brattain and William Schokley at Bell laboratories built the first working point contact

transistor (Nobel Prize in Physics in 1956).**1958**: Jack Kylby built the first integrated circuit flip flop at Texas Instruments (Nobel Prize in Physics in 2000).**1925**: Julius Lilienfield patents the original idea of field effect transistors.**1935**: Oskar Heil patents the first MOSFET.**1963**: Frank Wanlass at Fairchild describes the first CMOS logic gate (nMOS and pMOS).**1970**: Processes using nMOS became dominant.**1980**: Power consumption become a major issue. CMOS process is widely adopted.

2. VLSI Development

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known respectively as small-scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors [1].

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.

As of early 2008, billion-transistor processors are commercially available. This became more commonplace as semiconductor fabrication advanced from the then-current generation of 65 nm processes. Current designs, unlike the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality[3]. Certain high-performance logic blocks like the SRAM (static random-access memory) cell, are still designed by hand to ensure the highest efficiency. VLSI technology may be moving toward further radical miniaturization with introduction of NEMS technology.

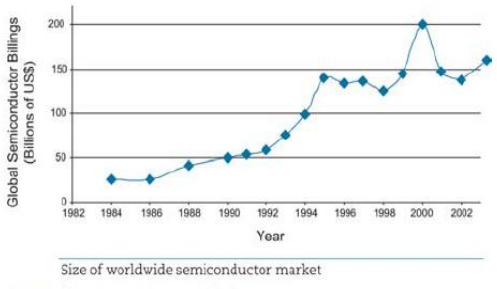


Figure-1: VLSI growth

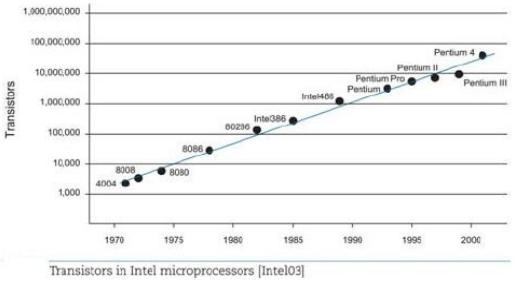


Figure-2: VLSI usage

Moore's Law

In 1963 Gordon Moore predicted that as a result of continuous miniaturization transistor count would double every 18 months.53% compound annual growth rate over 45 years. No other technology has grown so fast so long. Transistors become smaller, faster, consume less power, and are cheaper to manufacture Clock Frequencies of Intel Processors Transistor count is not the only factor that has grown exponentially, e.g. clock frequencies have doubled roughly every 34 months [2]

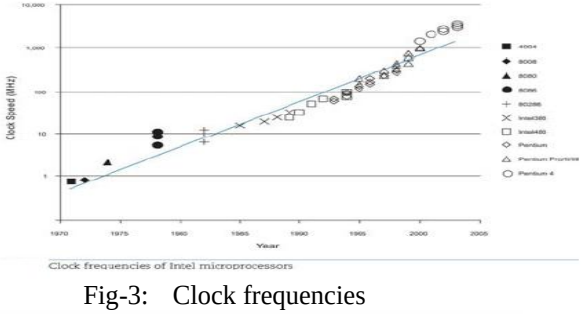


Fig-3: Clock frequencies

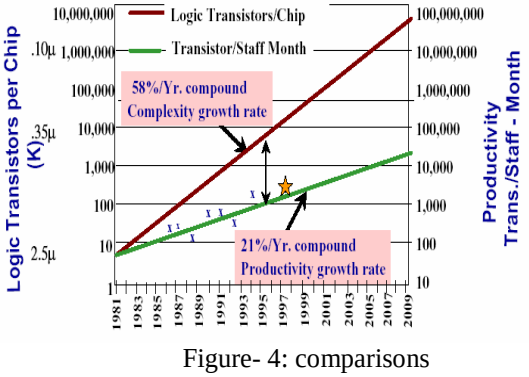


Figure- 4: comparisons

Chip Integration Level
SSI (up to 10 gates), MSI (up to 1000 gates), LSI (up to 10000 gates) and VLSI (over 10000 gates)
Technology Scaling
1971: Intel 4004 transistors with minimum dimension of 10um, 2003: Pentium 4 transistors with minimum dimension of 130 nm, Scaling cannot go on forever because transistors cannot be smaller than atoms the productivity Gap

3. VLSI Design

Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment [1].
Structured VLSI design had been popular in the early 1980s, but lost its popularity later because of the advent of placement and routing tools wasting a lot of area by routing, which is tolerated because of the progress of Moore's Law. When introducing the hardware description language KARL in the mid' 1970s, Reiner Hartenstein coined the term "structured VLSI design" (originally as "structured LSI design"), echoing Edger Dijkstra's structured programming approach by procedure nesting to avoid chaotic spaghetti-structured programs. VLSI chiefly comprises of Front End Design and Back End design these days. While front end design includes digital design using HDL, design verification through simulation and other verification techniques, the design from gates and design for testability, backend design comprises of CMOS library design and its characterization [1].

The major design steps are different levels of abstractions of the device as a whole:

1. Problem Specification: It is more of a high level representation of the system. The major parameters considered at this level are performance, functionality, physical dimensions, and fabrication technology and design techniques. It has to be a trade-off between market requirements, the available technology and the economical viability of the design. It includes the size, speed, power and functionality of the VLSI system [2].

2. Architecture Definition: Basic specifications like Floating point units, which system to use, like **RISC** (Reduced Instruction Set Computer) or **CISC** (Complex Instruction Set Computer), number of ALU's cache size etc.

3. Functional Design: Defines the major functional units of the system and hence facilitates the identification of interconnect requirements between units, the physical and electrical specifications of each unit. A sort of block diagram is decided upon with the number of inputs, outputs and timing decided upon without any details of the internal structure.

4. Logic Design: The actual logic is developed at this level. Boolean expressions, control flow, word width, register allocation etc. are developed and the outcome is called a Register Transfer Level (RTL) description. This part is implemented either with Hardware Descriptive Languages like VHDL and/or Verilog. Gate minimization techniques are employed to find the simplest, or rather the smallest most effective implementation of the logic.

5. Circuit Design: While the logic design gives the simplified implementation of the logic, the realization of the circuit in the form of a net list is done in this step. Gates, transistors and interconnects are put in place to make a net list. This again is a software step and the outcome is checked via simulation.

6. Physical Design: The conversion of the net list into its geometrical representation is done in this step and the result is called a layout. This step follows some predefined fixed rules like the lambda rules which provide the exact details of the size, ratio and spacing between components. This step is further divided into sub-steps which are:

6.1 Circuit Partitioning: Because of the huge number of transistors involved, it is not possible to handle the entire circuit all at once due to limitations on computational capabilities and memory requirements. Hence the whole circuit is broken down into blocks which are interconnected.

6.2 Floor Planning and Placement: Choosing the best layout for each block from partitioning step and the overall chip, considering the interconnect area between the blocks, the exact positioning on the chip in order to minimize the area arrangement while meeting the performance constraints through iterative approach are the major design steps taken care of in this step [2].

6.3 Routing: The quality of placement becomes evident only after this step is completed. Routing involves the completion of the interconnections between modules. This is completed in two steps. First connections are completed between blocks without taking into consideration the exact geometric details of each wire and pin. Then, a detailed routing step completes point to point connections between pins on the blocks [7].

6.4 Layout Compaction: The smaller the chip size can get, the better it is. The compression of the layout from all directions to minimize the chip area thereby reducing wire

lengths, signal delays and overall cost takes place in this design step.

6.5 Extraction and Verification: The circuit is extracted from the layout for comparison with the original net list, performance verification, and reliability verification and to check the correctness of the layout is done before the final step of packaging.

7. Packaging: The chips are put together on a Printed Circuit Board or a Multi Chip Module to obtain the final finished product.

3.1 Silicon Lattice

Silicon is a semiconductor. Transistors are built on a silicon substrate. Silicon is a Group IV material. Forms crystal lattice with bonds to four neighbours

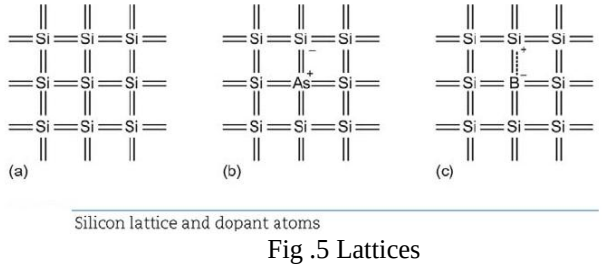


Fig .5 Lattices

3.2 Dopants

Pure silicon has no free carriers and conducts poorly. Adding dopants increases the conductivity. Group V extra electron (n-type). Group III missing electron, called hole (p-type)

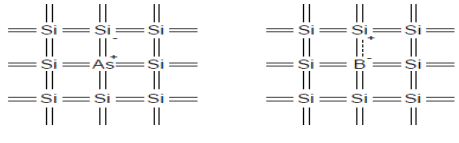


Figure-6: Dopants

3.3 Transistor Types

Bipolar transistors. npn or pnp silicon structure. Small current into very thin base layer controls large currents between emitter and collector. Base currents limit integration density. Metal Oxide Semiconductor Field Effect Transistors MOS and pMOS MOSFETS. Voltage applied to insulated gate controls current between source and drain. Low power allows very high integration [3]

3.4 MOS Transistors

Four terminals devices: gate, source, drain, body (= bulk = substrate). The gates controls whether a current flow between source and drain can be established. Source and drain are physically equivalent and depends on the direction of current flow.

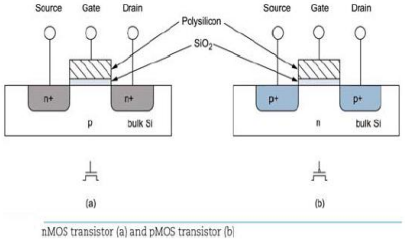


Figure-8: MOS

3.4.1 nMOS Operation

Body is commonly tied to ground (0 V).When the gate is at a low voltage P-type body is at low voltage. Source-body and drain-body diodes are OFF. No current flows, transistor is OFF[R1].

When the gate is at a high voltage:

Positive charge on gate of MOS capacitor. Negative charge attracted to body. Channel under gate gets "inverted" to n-type. Now current can flow through n-type silicon from source through channel to drain, transistor is ON

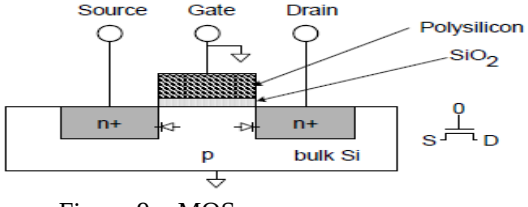


Figure-9: nMOS

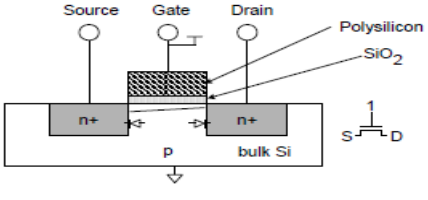


Figure-10: nMOS

3.4.2 pMOS Transistor

Similar, but doping and voltages reversed

Body tied to high voltage (VDD).Gate low: transistor ON. Gate high: transistor OFF. Bubble indicates inverted behaviour

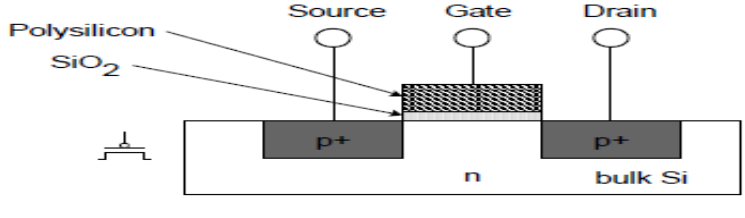


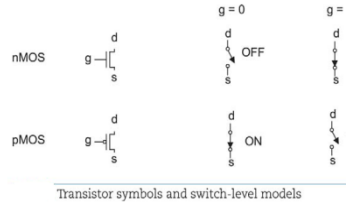
Figure-11: pMOS

Power Supply Voltage

GND = 0 V. In 1980's, VDD = 5V. VDD has decreased in modern processes. High VDD would damage modern tiny transistors. Lower VDD saves power.VDD = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0..

3.4.3 MOS Transistors as switches

We can model MOS transistors as controlled switches .Voltage at gate controls path from source to drain [4]



Transistor symbols and switch-level models

Figure-12: switch levels Table-1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table- 2 nMOS vs pMOS

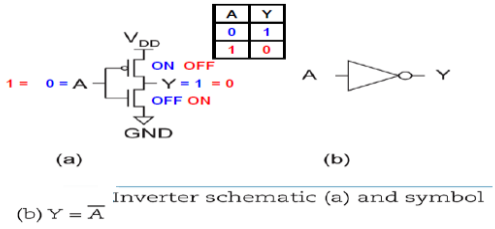
Table 1.1. Characteristics of nMOS and pMOS transistors

Transistor Types / Attributes	nMOS	pMOS
Majority carriers	*Electrons*	*Holes*
Mobility of majority carriers (typical value for 1 um process)	*500 cm^2/V-sec*	*180 cm^2/V-sec*
Substrate doping (light)	p^+	n^+
Source/drain doping (heavy)	n^+	p^+
Substrate(well) contact doping (heavy)	n^+	n^+
Substrate(well) contact connection	*Vss*	*Vdd*
Threshold voltage(Enhanced mode)	*Vtn>0*	*Vtp<0*
Logic value of the gate to turn on transistor	*1*	*0*
Capability of passing logic value	*poor 1, good 0*	*good 1, poor 1*

3.5 CMOS Technology

CMOS technology uses both nMOS and pMOS transistors. CMOS processing steps can be broadly divided into two parts. Transistors are formed in the Front-End-of-Line (FEOL) phase, while wires are built in the Back-End-of-Line (BEOL) phase[R1]. The basic raw material used in CMOS fabs is a wafer or disk of silicon, roughly 75 mm to 300 mm (12 mm a dinner plate!) in diameter and less than 1 mm thick. Wafers are cut from boules , cylindrical ingots of single-crystal silicon, that have been pulled from a crucible of pure molten silicon. This is known as the Czochralski method and is currently the most common method for producing single-crystal material. Controlled amounts of impurities are added to the melt to provide the crystal with the required electrical properties [7]. The transistors are arranged in a structure formed by two complementary networks. Pull-up network is complement of pull-down. Parallel -> series, series -> parallel [1]

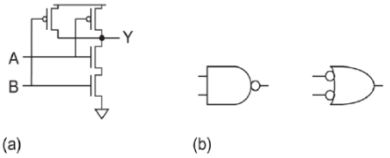
3.5.1 CMOS Logic Inverter



Inverter schematic (a) and symbol (b) $Y = \overline{A}$

Figure-13: Inverter

3.5.2 CMOS Logic NAND



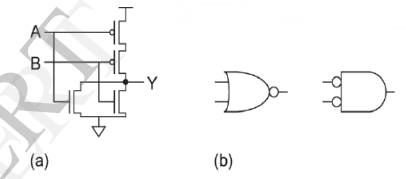
2-input NAND gate schematic (a) and symbol (b) $Y = \overline{A \bullet B}$

Figure-14: NAND

3.5.3 CMOS Logic NOR

Table- 3

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



2-input NOR gate schematic (a) and symbol (b) $Y = \overline{A + B}$

Figure-15: NOR gate

3.5.4 CMOS Logic Gates (a.k.a. Static CMOS)

Table -4 CMOS

Output states of CMOS logic gate		
	Pull-up OFF	Pull-up ON
Pull-down OFF	Z	1
Pull-down ON	0	Cross barred(X)

Example: $Y = \overline{(A+B+C)\cdot D}$

Table-5

A	B	C	D	Y
-	-	-	0	1
0	0	0	1	1
1	-	-	1	0
-	1	-	1	0
-	-	1	1	0

3.5 Compound Gates

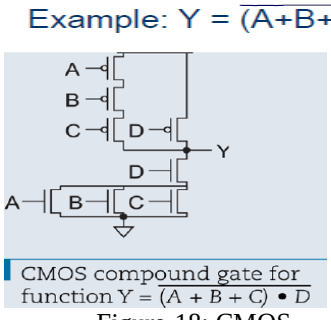


Figure-18: CMOS

3.6 Pass Transistors

Transistors can be used as switches

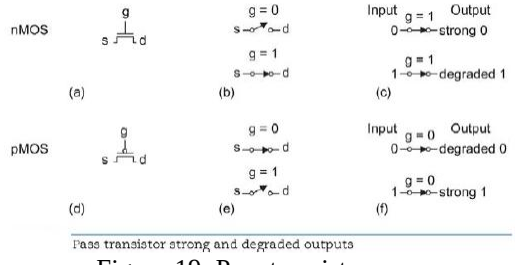


Figure-19: Pass transistor

Static CMOS gates are fully restored. In static CMOS, the nMOS transistors only need to pass 0's and the pMOS only pass 1's, so the output is always strongly driven and the levels are never degraded. This is called a fully restored logic gate Static CMOS is inherently inverting. CMOS single stage gates must be inverting. To build non inverting functions we need multiple stages [5]

3.7. Tristates

Tristate buffer produces Z when not enabled. Table.7

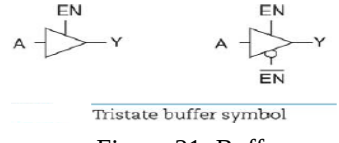


Figure-21: Buffer

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

3.7.1 Tristate Inverter

Tristate inverter produces restored output
For a non inverting tristate add an inverter in front

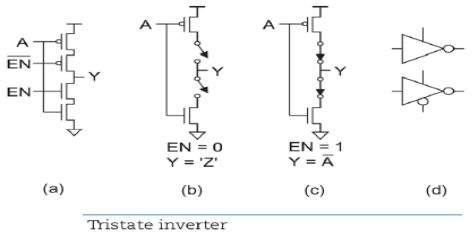
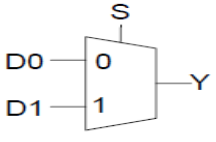


Figure-23: Tristate Inverter

3.8 Multiplexers

2:1 multiplexer chooses between two inputs Table-6



S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

Figure-24: Mux

3.8.1 Gate-Level Mux Design

Y = S D0 + S D1

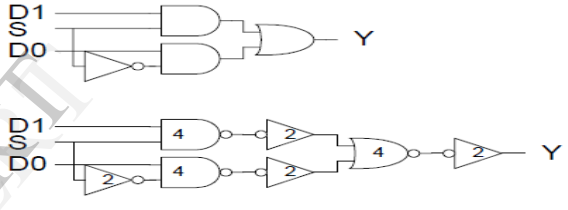


Figure-25: Gate-level

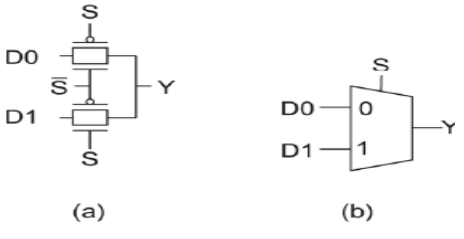


Figure-26: Transmission Gate Mux

3.8.3 Inverting Mux

Inverting multiplexer, use compound gate or pair of tristate inverters, essentially the same thing & for non-inverting multiplexer add an inverter

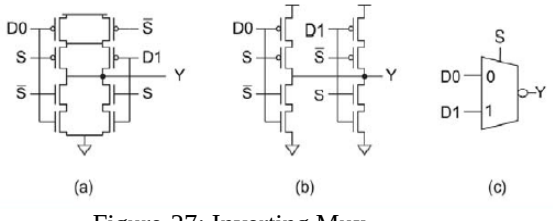


Figure-27: Inverting Mux

3.9 D Latch

When CLK = 1, latch is *transparent*, D flows through to Q like a buffer, When CLK = 0, the latch is *opaque*, Q holds its old value independent of D, a.k.a. *transparent latch* or *level-sensitive latch [6]*

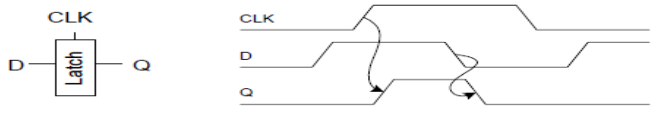


Figure-28: D Latch

3.9.1 D Latch Design

Multiplexer chooses D or hold Q

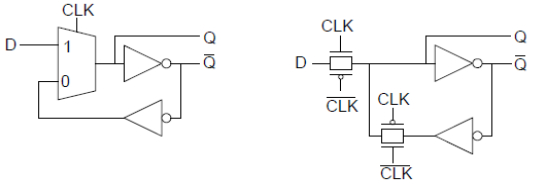


Figure-29: D Latch Design

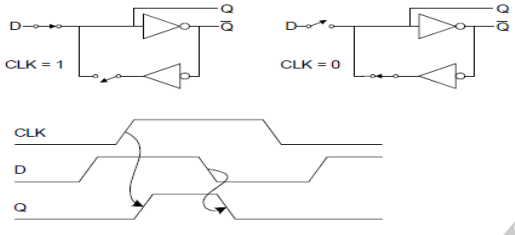


Figure-30: D Latch Operation

3.9.2 D Flip-flop

When CLK rises, D is copied to Q, at all other times, Q holds its value, a.k.a. *positive edge-triggered flip-flop, master slave flip-flop*

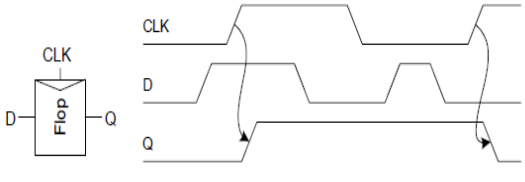


Figure-31: D Flip-flop

3.9.4 D Flip-flop Design Built from master and slave D latches

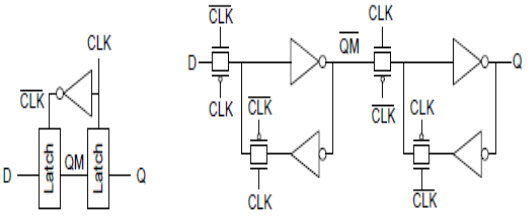


Figure-32: D Flip-flop

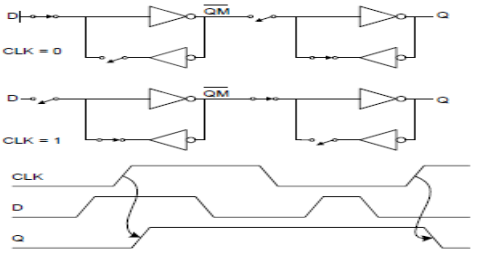


Figure-33: D Flip-flop Operation

4. Future of VLSI

Initially, design can be done with three different methodologies which provide different levels of freedom of customization to the programmers. The design methods, in increasing order of customization support, which also means increased amount of overhead on the part of the programmer, are FPGA and PLDs, Standard Cell (Semi Custom) and Full Custom Design.

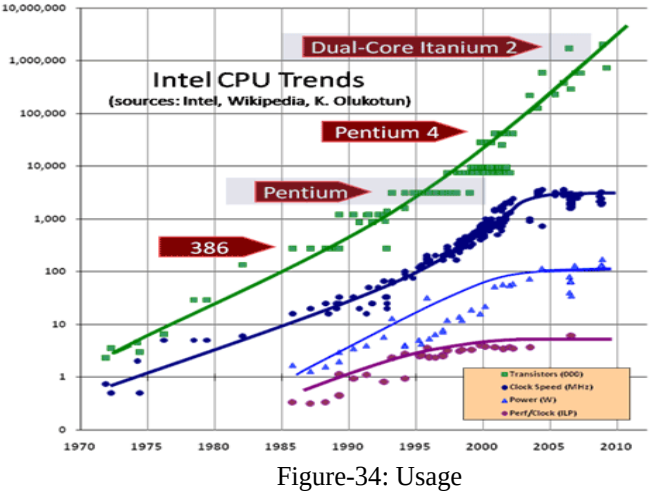


Figure-34: Usage

VLSI technology may be moving toward further radical miniaturization with introduction of NEMS technology. In coming decades VLSI design which currently enables us to build million-transistor chips will become Giga scale (GSI) design and Tera scale Integration (TSI) design, respectively. It is plausible that new nanotechnologies will be used to complement or replace CMOS [1].

5. Conclusion

VLSI is dominated by the CMOS technology and much like other logic families, this too has its limitations which have been battled and improved upon since years. Taking the example of a processor, the process technology has rapidly shrunk from 180 nm in 1999 to 60nm in 2008 and now it stands at 45nm and attempts being made to reduce it further (32nm) while the Die area which had shrunk initially now is increasing owing to the added benefits of greater packing density and a larger feature size which would mean more number of transistors on a chip[R7].

High speed clocks used now make it hard to reduce clock skew and hence putting timing constraints. This has opened up a new frontier on parallel processing. And above all, we seem to be fast approaching the Atom-Thin Gate Oxide layer thickness where there might be only a single layer of atoms serving as the oxide layer in the CMOS transistors.

6. References

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