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Development of Higher Efficiency Mono Crystalline Silicon Solar Cells

Nanda kiran S, M. L. S Deva kumar, S. Ravi, Silika Mahapatha, Pratha Jhawar

M. Tech (Energy Systems), Jawaharlal Nehru Technological University Anantapur

Abstract: At present mono crystalline silicon solar cells are more established and mostly used to generate electricity rather than using thin films crystalline silicon solar cells, amorphous silicon solar cells, because they attain less efficiency. Improvement in efficiency of mono crystalline silicon solar cells is very much relevant today from the point of view of cost reduction.

Some of the very promising approaches for efficiency improvement for conventional silicon solar cells manufactured with screen printing technology are modification in the existing screen printing, Al BSF process, selective emitter, back surface passivation, HIT cells, multilayer Anti-reflection coating and other technologies etc. These technologies boost the efficiency of a solar cell by 1-2%.

This paper discussed and investigated for improving efficiency in mono crystalline silicon solar cells with uniform texturization, multilayer ARC, front grid optimization, metallization and increasing aspect ratio which decreases shadow effect and also lowers the series resistance, in the manufacturing process of mono crystalline silicon solar cells.

Key words: silicon solar cells, standard Test condition (STC), phosphorous oxy-chloride, alkali solution, silicon nitride.

1. Introduction

Bharat Heavy Electricals Limited has established semiconductor manufacturing facilities at its Electronics Division, Bangalore wherein it manufactures 125-mm / 156-mm pseudo square mono crystalline silicon solar cells with power output of 2.5 / 3.9 watts and solar cell conversion efficiency of 17.5 %. Photovoltaic modules are constructed with 36/60/72 (for 12/20/24 V) solar cells which are interconnected in series configuration and yield a power output of 80 to 270 watt. PV modules of 170-watt / 220 -watt rating are interconnected in series (PV array) – parallel configuration in the case of a grid interactive power plant to obtain the required voltage and power output for the power plant.

The most important challenges in improving solar cell efficiency include meeting the contradictory requirements of having high Voc and high current since both are dependent on the surface condition in crystalline silicon solar cells, reducing the series resistance in low temperature process and optimizing the front contact for both conduction and transmission. Resistive effects in solar cells reduce the efficiency of the solar cell by dissipating power in the resistances. The most common parasitic resistances are series resistance and shunt resistance. The impact of parasitic resistance is to reduce the fill factor.

2. Manufacturing Process of solar cells

2.1 Texturisation

The silicon wafers are manufactured through CZ pulling process for mono crystalline or metal casting process for multi crystalline wafers. The as-cut p-type boron-doped silicon wafers are chemically etched in concentrated alkali solution to remove saw damages followed by a dilute alkali texturising step to form pyramid-like structures on the wafer. Process parameters such as alkali concentration, solution temperature and process time are optimised to get well-defined normal random pyramids which enhance the surface area of the wafer for greater light absorption and at the same time, facilitate total internal reflection of light. Another main purpose of the texturisation is to reduce the reflection of light incident on the cell surface. This purpose is achieved by making the wafer surface more sensitive to absorption of photons by increasing the path of reflection.

On solar cell, without texturisation process 30% of sunlight is reflected back. With texturisation 11% of sunlight is reflected.

2.2 Pre-diffusion cleaning

This process is done immediately after the Texturisation, so that Alkali is neutralized with the Acid. HF and HCL in proper proportion are used. HF removes oxide layer and cleans the surface, this is important before Diffusion process. After the process wafers are thoroughly rinsed in DI running (air agitated) and dried before sending them to Diffusion.

2.3 P-N Junction formation by thermal Diffusion

Junction formation is the process in which the required impurities are deposited / penetrated in the wafer surface in such a way that the minority carriers in the starting material are not degraded. This process is also called “Diffusion of Impurities” the impurity profile has to be tailored for highest conversion efficiency. The required n-type layer is deposited over the p-type silicon wafer to get a simple P-N junction. The n-type dopant generally added will be phosphorous in the form of liquid. Diffusion in the gaseous phase at around 850 to 950 ºC is maintained.

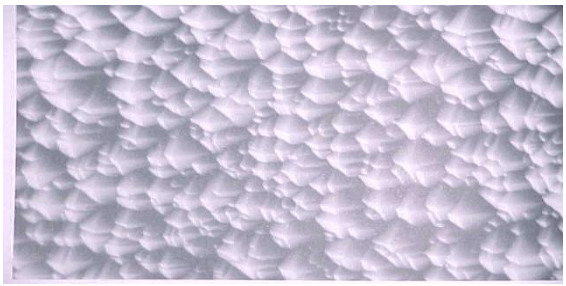

Fig 1: *SEM photograph of pyramidal structure formed on the silicon wafers*

A p-n junction is then formed on the textured silicon wafer through a high-temperature, solid- state diffusion process in a quartz furnace. In this process, phosphorous oxy-chloride ($POCl_3$) liquid dopant is deposited on the wafers and is driven in when a thin n-type layer is formed.

2.4 Sheet Resistance (Ω/sq.)

After Thermal diffusion, Silicon wafer is placed in sheet resistance equipment, sheet resistance equipment shows wafer as n-type (i.e. wafer was changed into p-type to n-type wafer in thermal diffusion). If sheet resistance is more power generation is more.

2.5 Edge Isolation & PSG Removal

The junction formed in diffusion process has to be isolated with the edge of the wafer. This can be done either by chemical (wet) process or through Plasma Etching (Dry) process The wafers are coin-staked and etched using Freon-oxygen gas mixture in dry plasma etch machine so as to remove the junction regions created on the edges, is done for Edge Isolation process. The wafers are then chemically etched to remove the oxides and phosphorous glass from the surface, is done for PSG Removal.

By the Edge Isolation Process shunt resistance of solar cells is increased.

2.6. Multi layer ARC

Further Reflection of sunlight is reduced by the process of PECVD (Plasma Enhanced Chemical Vapour Deposition) this is done in Anti-Reflection coating equipment. A thin film of silicon nitride (anti-reflection coating) is deposited on the wafer to lower the reflection of light further and to passivate the solar cell against harmful environment such as humidity, ionizing radiation and reactive module lamination materials.

A graded Refractive index with two layers of silicon nitride was optimized by varying the composition of reactive gases (Silane and Ammonia) and deposition time. This process enhances the solar cell conversion efficiency to 16%. The silicon nitride anti-reflection coating enhances the solar cell conversion efficiency by almost 1 %.

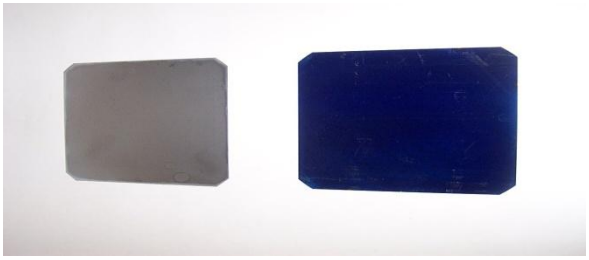

Fig 2.a: *Photograph of Non-AR coated and AR Coated Silicon wafer*

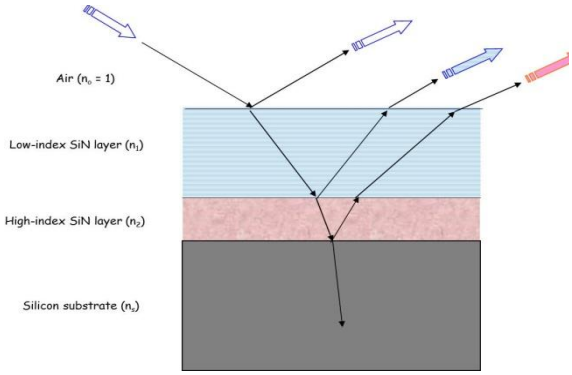

Fig 2.b: *Destructive interference among reflected optical rays for minimum reflectance in 2-layer arc system with high-index (n_2) and low-index (n_1) SiN.*

In ARC, single layer ARC, Dual layer ARC and Five layers ARC are performed. The refractive index of layers was measured by Ellipsometer.

2.7 Screen Printing

For taking the electrical contacts from the PV cells, three different printings is done on the PV cells. Silver (Ag) / Aluminium (Al) bus bar for soldering purpose at the back, 'Al' at the back as back surface field and 'Ag' grid pattern in the front side. After each printing drying is done at 230˚c in a conveyor furnace for drying solvent which is present in the paste.

Series Resistance of solar cell can be decreased by the Screen Printing process.

Front Contact printing:

The requirement for the front metallization are low contactresistance to silicon, low bulk resistivity, low line width with high aspect ratio, good mechanical adhesion, solderability and compatibility with the encapsulating material. Resistivity, price& availability consideration makes silver, the ideal choice as the contact metal.

Fig 3.a: *Front side pattern comparison – 2 Busbar vs 3 Busbar*

Back contact print:

Same operations are performed on the back side of the cell exceptthe paint contains both silver and aluminium & the print pattern is different. Aluminium is required because silver does not form ohmic contact to silicon, but cannot be used alone because it cannot be soldered. Above two steps are carried in specially designed automated equipment.

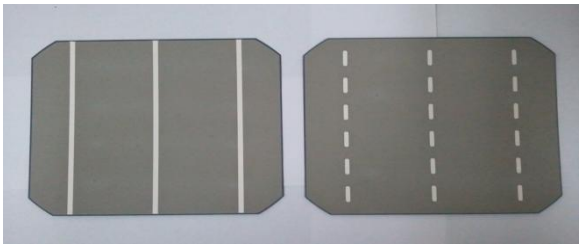

Fig 3.b: *Solar cell - Back side pattern with 3 split Bus bars*

2.8 Firing

After all three printings, and drying, Co-firing is done for burning the binders and additives so that only pure metals remains on the cell. Firing is the process in which the wafers are baked for short

time in order to increase the adherence and ohmic contact. In this process wafers are passed through a conveyors chain at high temperature (800 - 900˚c) for a short time. The temperature and the time duration of process is to optimize between the good contact resistance and junction shorting. During the manufacturing of paste, different compounds like, additives, binders, solvents are added to keep the metal in semi-solid condition to aid screen printing which are highly di-electric in nature. These binders are burnt firing process and there by decrease the series resistance. It is continuous process and has a throughput of 1000 cells/ hour at a belt speed of 120-150 IPM. Fired cells collected and subjected for electrical current measurement.

2.9 Testing

Testing is the process of evaluating the voltage-current (V-I) characteristics of the solar cell under the simulated light intensity condition. Here the illumination of the sun simulator is set to Air-mass 1.5 (AM 1.5) in which the actual intensity is 1 K w per sq. meter area. Terrestrial solar cells are evaluated for their V-I characteristics from which open circuit voltage (Voc), short circuit (Isc), maximum power (Pmax), Fill Factor, efficiency, and series resistance (Rs) are measured under the simulated intensity.

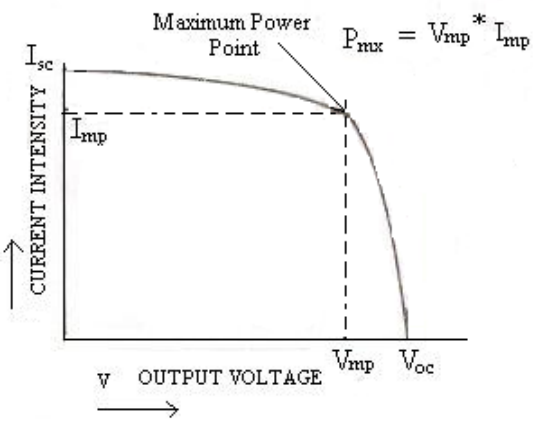

Fig 4: *A typical I-V plot for solar cell*

3. Experimental Analysis

To improve the efficiency and output wattage of solar cell some experimental analysis has done in Thermal Diffusion, some wafers with sheet resistance is restricted to 30Ω/sq. and other with 55-60 Ω/sq.

In Multi Layer ARC, Single layer ARC, Dual layer ARC, Five layer ARC was performed with different composition of Silane and equal composition of Ammonia and with different deposition time.

At 1.5, Air mass, 25˚C, temperature, 1000W/m² Irradiance.

Fill Factor (FF) = $\frac{\mathbf{Imp} * \mathbf{Vmp}}{\mathbf{Isc} * \mathbf{Voc}} * 100.$

Efficiency (η) = $\frac{\mathbf{Isc} * \mathbf{Voc} * \mathbf{FF}}{\mathbf{A}(\text{cm } 2) * \frac{\mathbf{100\ MW}}{\text{cm } 2}} * 100.$

A = 156 mm * 156 mm (Or)

A= 125 mm *125 mm

4. Conclusion

It is optimistic to believe that pursuit of new diagnostic tools and innovative refinements in manufacturing practices such as above is likely to evolve modified technological processes for the silicon solar cell.

At STC, 1.5 Air mass, 25˚C temperature, 1000W/m² Irradiance, the mono crystalline silicon solar cells with Sheet Resistance of 55-60 Ω/sq has high efficiency and high output wattage compared with Sheet Resistance of 30 Ω/sq. High sheet resistance results high cell wattage and high efficiency.

Dual layer ARC results good improvement in cell efficiency and cell wattage compared with single layer ARC and five layers ARC. Dual layer ARC with V_{mp} = 0.525V results cell efficiency (η) = 17.43%, Fill Factor (FF) = 77.65% and cell wattage = 4.243W where as Dual layer ARC with V_{mp} = 0.5V results cell efficiency (η) = 17.02%, Fill Factor (FF) = 74.97% and cell wattage = 4.142W. Single layer ARC results cell efficiency (η) = 17.30%, Fill Factor (FF) = 78.3% and cell wattage = 4.211W and five layer ARC results cell efficiency (η) = 17.35%, Fill Factor (FF) = 78.59% and cell wattage = 4.224W.

Bus grid line height increases means current generation will increases but it increases beyond critical height, shadow effect will be more and current generation will decreases. So Aspect ratio was also main factor in development of higher efficiency of solar cells. Aspect ratio (height/width) was maintained to 0.25. Whereas in aspect ratio height = 0.25µ and width = 85- 90 µ.

With these efforts at BHEL Electronics Division Bangalore, the highest efficiency of crystalline silicon solar cells reached over 18%. Further R & D work has been planned in this area to push the efficiency to around 19% in near terms.

5. Acknowledgement

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