Digital DC-DC Converter With Predictive and Feed forward Control for Fast-Transient Integrated

Abhishek Choudhary[1], Vivek Patel(Assistant Professor)[2]
Department of Electrical Engineering [1, 2]
Technocrats Institute of Technology, Bhopal[1, 2]

Abstract:- This paper studies dual-mode digital dc-dc converters combining the predictive and feedforward control with the conventional PID controller to achieve fast transient response and low overshoot. An additional predictive or jerk component is added to the conventional PID controller to speed up the transient response. This predictive term is based on the second derivative of the error signal and introduces zero to the loop response which leads to increased bandwidth and improved phase margin. In addition, a feedforward control is also employed to further improve the transient by evaluating the change in the inductor current during the on and off time of the power transistors. Theoretical analysis and simulations were carried out to analyze the proposed design and algorithm. The proposed design is verified on silicon with a prototype of a digital dc-dc converter fabricated in CMOS 0.20 m process. The digital dc-dc converter achieved a settling time of 5s and an overshoot of 20 mV for a step-load transient of 500 mA, which are improved significantly as compared to the prior arts.

I. INTRODUCTION

Conventional offline design of controllers for dc–dcpower converters is complicated by unknown load characteristics, as well as uncertainties within the converter itself.The converter component values are subject to manufacturingtolerances, and converter parasitic are notoriously difficultto model. In light of these uncertainties, the designer mustmake some assumptions regarding the expected range of loadand core converter dynamics, and design a controller thatwill maintain acceptable stability margins under worst-caseconditions. A robust design capable of handling wide variationsin dynamics will be overly conservative by design over mostof the expected range, resulting in degraded performance. The benefit of an autotuning controller is the ability to performonlinecontroldesigninthepresenceofactualsyste m dynamics, resulting in a more optimal design over the full range of systemcharacteristics. The ability to embed such algorithms into theexisting feedback controller represents a significant advantageofdigitalcontrollersforswitched-modepowersupplies (SMPS) over their analog counterparts.A high performance VLSI system requires a fast transientdc-dc converter to frequent load changes due to the nature of a multimode system [6]. Thus, both academics and industries put a lot of efforts into the research of the control schemes of the digital dc-dc converter to achieve good transient response and high robustness with a simple architecture. A typical dc-dc converter has a right-half-plane (RHP) zero in its control-to- output transfer function. This property introduces phase lag inthe system response and limits the unity-gain frequency of the converters [7]. In addition, the time-delay or latency of the dig- ital controller further increases the phase lag and degrades the robustness of the converter. As such, this increases the difficulty in the design of the controller using the conventional PID approach to achieve ability and fast dynamic response over input and load perturbation.

The main objective of this paper is to address the problemsof dynamic response and complexity with the introduction of a digital dc-dc converter adopting a predictive controller to enhance the transient performance. The proposed digital controller is based on a novel predictive feedforward PID (PFPID) approach to achieve fast settling time and limited overshoot of the integrated dc-dc buck converter during load transient. The PFPID control is realized by combining the predictive and feedforward control with the conventional PID control. The predictive control is based on the second derivative of the errorsignal and introduces zero to the loop response which leads to increased bandwidth and improved phase margin. To limit the overshoot, the feedforward control is implemented by evaluating the change in the inductor current during the on and offtime of the power transistors within a switching cycle. The proposed design has a simple architecture, which leads to a small l IC area. Theoretical analysis is further verified on silicon with a prototype of a digital dc-dc converter fabricated in the CMOS0.18μm process.

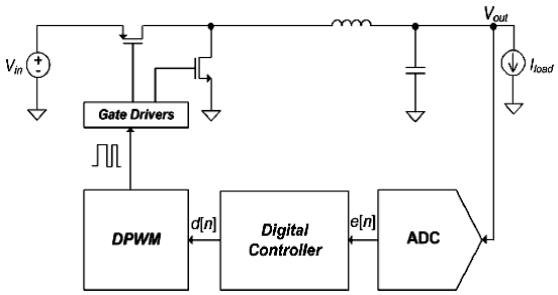

Fig. 1. Block diagram of a conventional dc-dc buck converter with its control peripherals.

II. PROPOSED DIGITAL HYSTERETIC VOLTAGE-MODECONTROL

In this section, the architecture of the proposed control will be presented in its basic form. An analog realization of the control will be considered first, leaving the details of its digital implementation to a next section. The reason behind this presentation is to separate the concept of the controller behavior, which is better grasped if treated in the analog domain from the actual, digital realization of the technique, which calls for a whole set of implementation details but keeps unchanged the underlying ideas. Preliminary to the description of both the analog and digital versions of the proposed compensator, the most important building block, namely the high-bandwidth hysteretic differentiator, is introduced.

A. *High-Bandwidth Hysteretic Differentiator*

The derivation of the proposed hysteretic voltage-mode control is based on the hysteretic differentiator concept. To illustrate the idea, let us first consider Fig. 1. Any ideal differentiator with gain Kd can be approximated with a negative-feedback system that employs a high gain K in the direct path and an integrator with gain $1/Kd$ in the feedback path. The higher the gain K, the better the derivative action is emulated. Beside the problems related to its actual implementation, the feedback system in Fig. 1 has the major disadvantage of not producing a modulated ON/OFF signal suitable for driving a power converter. Thus, its employment in an analog control scheme for a switching converter would still require a modulator.

However, it is indeed possible to obtain a differentiator, which *inherently* modulates the derivative $Kd(\mathrm{d}x/\mathrm{d}t)$ of the input signal into a switching waveform, by replacing the linear gain K with a noninverting hysteretic comparator, as shown in Fig. 2.

The comparator has symmetric hysteresis thresholds, located at $+\beta/2$ and $-\beta/2$, β being the hysteresis window, and generates the switch ON/switch OFF signal $S(t)$, here defined in a logic sense, i.e., S switches from 0 to 1 when the comparator input crosses the threshold $-\beta/2$, whereas a 1-to-0 transition occurs when the comparator input crosses the threshold $+\beta/2$. Moreover, we shall denote with $\bar{S}$ the logic negation of the switch signal. In Fig. 2, we introduce a notation that will be adopted several times in the text and figures, namely that of indicating with $(2S(t) - 1)A$ the operation that generates the number $+A$ or $-A$ according to the logical state S being 1 or 0, respectively.

$$md(t) = (2S(t) - 1)1/2Kd = 1/2KdS(t) - 1/2KdS(t).$$

In steady-state conditions, i.e., with a constant input signal $x(t) = X$, it is easily found that $md(t)$ is a periodic square wave with zero average value and 50% duty cycle. The switching period Ts is given by

$$Ts = 4\beta Kd . \quad (2)$$

On the other hand, the integrator output $vR(t)$ is a piecewise linear signal that ramps up and down between the values $X + \beta/2$ and $X - \beta/2$. Thus, in steady-state conditions, the hysteretic differentiator oscillates with a well-defined switching frequency. For small perturbations $\hat{x}(t)$ of the input signal $x(t)$, the action of the integrator and the hysteretic comparator is that of maintaining the integrator output v_R to within $\pm\beta/2$ with respect to $x(t)$. An approximate averaged small-signal analysis, commonly adopted when treating analog hysteretic control loops, starts with the assumption that the average value of v_R and the average value of x are equal. This yields

$$v_R(s) = 1/sK_dS(s) \sim= x(s) \Rightarrow S(s)x(s) \sim= sK_d$$

B. *Overall Architecture*

A digital dc-dc buck converter typically consists of four blocks, namely an analog-to-digital converter (ADC), a digital controller, a digital pulsewidth modulator (DPWM), and a power stage consists of power transistors with gate drivers and output filter as depicted in Fig. 1. The ADC is employed to sample the output voltage and convert it into a digital code forthe controller. The controller then executes the control algorithm and produces a digital command for the DPWM. Based on the digital command, the DPWM generates a pulsewidthmodulated (PWM) pulse voltage to drive the power transistors.

The PWM pulse voltage is eventually filtered by the external low-pass filter to produce the output voltage. Fig. 2 depicts the architecture of the proposed digital dc-dc converter and its PFPID control scheme. The proposed digital dc-dc converter comprises four main blocks, namely a hybridsegmented digital pulsewidth modulator, a dual-mode (PWM/PFM) PFPID controller, a window successive approximation (SAR) ADC and a power stage consisting of power transistors with input buffers and external low-pass filter.

The principles of operation are as follows. First, the hybrid segmented DPWM generates the PWM signal for the gate drive of the power transistors with a combination of the segmented tapped delay-line and the counter-comparatortechnique to achieve high resolution. Second, the dual-mode digital controller selects the appropriate mode of operation, pulse width modulation (PWM), which is of fixed-frequencyoperation, or pulse-frequency modulation (PFM), which is of variable frequency operation to achieve high efficiency. For high load current operation, as the dominant loss is the conduction loss due to parasitic resistances, such as the equivalent series resistance (ESR) of the inductor and the on-resistance ofthe power transistors, the dc-dc converter should operate in the PWM mode with constant switching frequency. On the other hand, when the load current is low, PFM is the preferred mode of operation to reduce switching loss. Essentially, the controller compensates the frequency response of the dc-dc converter to achieve stability and fast transient response. Third, the power stage is composed of the parallel power transistors, consistingof the on-chip PMOS and NMOS transistors, and the external (off-chip) low-pass filter. For the feedback loop to be closed, an ADC is needed to convert the output voltage into the digitaldomain. In this case, we propose a window SAR ADC that is able to achieve moderate speed with small IC area. This is sufficient for the dc-dc converter application. Although the dual-mode PWM and PFM control is sufficient to achieve moderately high efficiency, further control strategies are needed to optimize the transient response. Therefore, feed forward control and predictive or jerk control are adopted to achieve ultra-fast transient response. These two control circuits are added in parallel with the original PID control circuits. The feed forward control augments the feedback control by detecting and processing the input current value from the current detector. This will significantly improve the overshoot performance and the noise disturbance as a desired limit can be imposed directly on the output signal. Another control method,

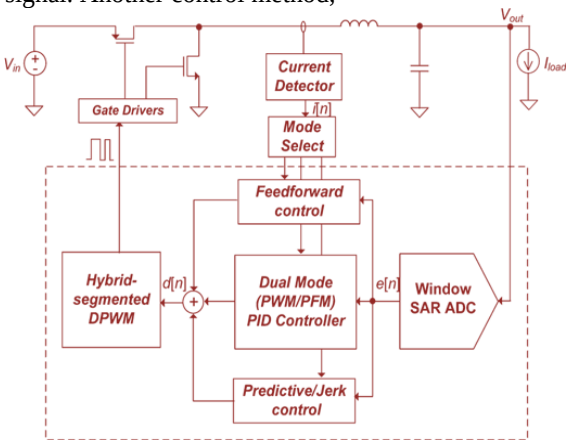

Fig. 2. Architecture of the proposed digital dc-dc converter with feed forward and predictive/jerk control.

the so-called "jerk control," is an additional predictive component,which is, in fact, the coefficient of the "derivative of thederivative" of the error signal of the feedback and the referencevoltages. It is used to optimize the rate of change of the outputvoltage so that no abrupt changes in the output voltage are allowedto occur and induce voltage spikes. Similar to the effectof the derivative term, it will gen
erate additional phase lead forthe loop response of the system in the frequency domain.

C. *Analog-to-Digital Converter (ADC)*

The ADC employed in our design is a window successive approximation (SAR) ADC using an ultra-fast, auto-zero comparator as depicted in Fig. 3. The SARADC has a dynamic reference voltage range to reduce power consumption. The auto-zero scheme of the comparator is realized internally with a preamplifier stage and a latch stage. Since the error signal is small most of the time, a full-range ADC is not necessary. This is because the output voltage is generally constant except during transient. Even in the transient period when there are changes in the load or line voltage, the output voltage will typically vary in a limited range around the desired output voltage. Therefore, the input range of the ADC is defined between an upper limit, and a lower limit, . This has the significant advantage of reducing the power consumption as the voltage across the capacitors is smaller.

The window SAR ADC requires eight clock cycles for data conversion. During the first clock cycle, data are sampled at the input ports. For the second clock cycle, data are being held.

Next is the bit cycling process: output bits are being determined for each clock cycle from MSB to LSB. Finally, at the eighth clock cycle, data are being output and the conversion process iterates. In this case, the clock frequency is 32 MHz and thus, the conversion rate is 4MSPS. This conversion rate is chosen to reduce the delay that causes phase lag to the frequency response while maintaining low dynamic power consumption.

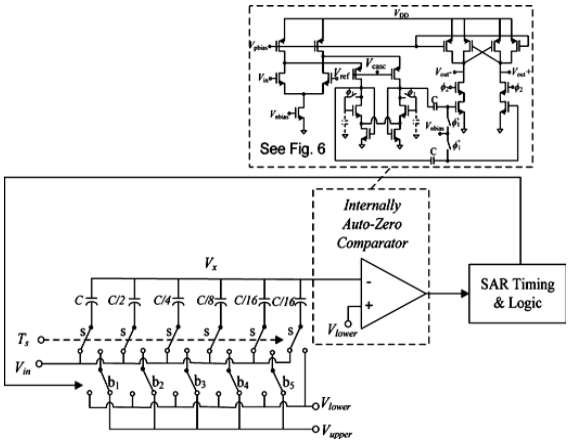

Fig. 3. Architecture of the window SAR ADC with an internally auto-zero comparator.

III. PFPID CONTROL FOR FAST-TRANSIENT DIGITAL DC-DC CONVERTER

In the conventional PID controller, there are three gain coefficients, namely, the proportional gain, the derivative gain, and the integral gain. First, the proportional gain directly affects the loop gain of the dc-dc converter and the derivative gain, directly influences the settling time and the overshoot. Third, the integral gain reduces the steadystateoffset errors. These three gain coefficients are tuned to achieve the desired transient performance. However, there are several limitations associated with PID control. It generally does not provide the optimal transient response, and the overshoot in PID control is typically high if the loop gain is large. Besides,when PID control is adopted in a non-linear system, it is generally overdamped to reduce overshoot which, in turn, increases the settling time. Put differently, the PID control trades off settling time for reduced overshoot or vice versa in the control of non-linear system. As dc-dc converter is inherently non-linear, the use of PID control in the digital dc-dc converter yields suboptimal performance. Thus, to circumvent the limitations of the conventional PID control, a PFPID control that is a combination of two control schemes: the predictive PID (PPID) control and the feedforward (F) control, is proposed for the control of dc-dc converter.

Predictive PID Control

In the proposed predictive PID control algorithm, we have introduced an additional predictive or jerk term and the corresponding gain coefficient. Fig. 3 depicts the waveforms of the output voltage and output current, during a load transient. We note that the effect of the jerk term is to push the perturbed waveform of the output voltage back to the original ripple-like waveform. Thus, by introducing the jerk term in additionto the conventional PID, the dc-dc converter is able to achieve a faster settling time. In the continuous time domain, the new control output is

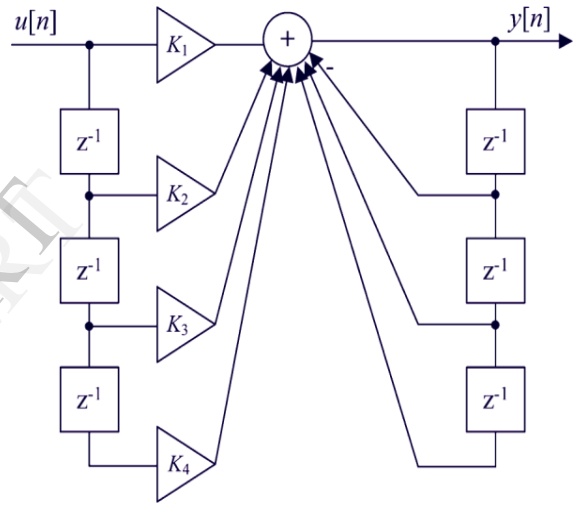

Fig. 4. Implementation of predictive PID control.

$$K_1 = K_P + K_D\frac{2}{T} + K_I\frac{T}{2} + K_J\frac{4}{T^2}$$
$$K_2 = K_P - K_D\frac{2}{T} + 3K_I\frac{T}{2} - 3K_J\frac{4}{T^2}$$
$$K_3 = -K_P - K_D\frac{2}{T} + 3K_I\frac{T}{2} + 3K_J\frac{4}{T^2}$$
$$K_4 = -K_P + K_D\frac{2}{T} + K_I\frac{T}{2} - K_J\frac{4}{T^2}$$

Where is the clock period. In Fig. 3, is the control input and is the control output of the PPID controller. The coefficients, and are implemented using a look-up table instead of multiplication circuits to achieve lower power consumption and smaller IC area. there are four parameters to be designed as opposed to the three gain coefficients of the conventional PID. This introduces

one more degree of freedom which can be leveraged to mitigate the settling-time problem of the conventional PID. is typically selected such that the location of the zero is approximately 50 times smaller than the switching frequency. This is because if is too small, the effectof the zero is negligible at the system bandwidth. On the other hand, if is too large, the zero will affect the system stability by allowing noise and ripple to fall into the increased bandwidth, and thus the system becomes noise-sensitive.

IV. EXPECTED SIMULATION RESULTS

Simulation results of the step-load transient of the dc-dc converter with the predictive and feed forward PID controller against the conventional PID are depicted in Fig. 13. The simulations are run in Simulink, MATLAB with the developed model of the predictive and feed forward controller. The values for output filter are: 20µ F, 15 m H, and 200 mΩ . Note that the settling time is reduced by approximately 55% and that the new overshoot is one-third of the overshoot achieved by the conventional PID. The improvement can be explained by the Bode plot of the control-to-output transfer function of the dc-dc converter.

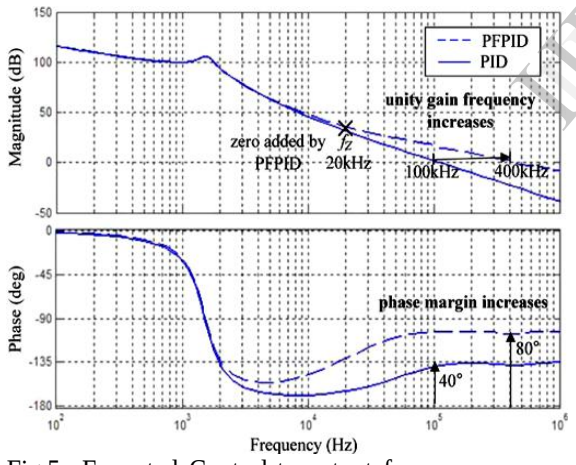

Fig.5 Expected Control-to-output frequency response of the dc-dc buck converter with the PFPID control against conventional PID control.

With the PFPID controller against the conventional PID controller, which is depicted in Fig. 5. In the Bode plot, both the unity-gain frequency and the phase margin have increased due to the additional LHP zero introduced by the predictive control (term) at 20 kHz, which is 1/50 of the switchingfrequency of 1 MHz. Therefore, a faster transient response canbe achieved.

In particular,we note that in the gain plot,with the presence ofan additional zero at 20 kHz, the unity gain frequency increasesfrom 100 kHz to 400 kHz. This is because the additional zeroreduces the roll-off of the magnitude plot from dB todB after 20 kHz, which results in the increase of unity-gain frequency.

However, further increase of the unity-gain frequencybeyond 400 kHz will result in the increase of noise due tothe output ripple at the switching frequency of 1 MHz beingfed back to the system. In the time domain, the increase of theunity-gain frequency to 400 kHz translates to a reduction in risetime during the transient period of the dc-dc converter.From the phase plot, it is noted that the phase margin increasesfrom 40 to 80 with the additional LHP zero. This yields a faster settling time and a reduced overshoot during transient because the closed-loop Q factor is related to the phase margin. Note that although the zero introduced by the PPID control generates a phase change, the feed forward control cancels part of it in the vicinity of the switching frequency of 1 MHz due to the 180 out of phase of the feedforward signal and the feedback error signal, which results in the overall increase of phase margin of 40 . However, this is sufficient for the dc-dc converter and further increase of the phase margin will result in an overdamped response.

V. EXPECTED EXPERIMENTAL RESULTS

The digital dc-dc converter based on the architecture in Fig. 2 was designed and fabricated with Global Foundries CMOS 0.18m process. The microphotograph of the test chip is shown in Fig. 15. The core area of the digital dc-dc converter including the power transistors is 1 mm (1 mm 1 mm). The values foroutput filter: H and F, m . Thetest printed circuit board is depicted in Fig. 16. The overallperformanceof the digital dc-dc converter test chip was measuredin terms of: 1) steady-state response, and 2) dynamic or transientresponse.

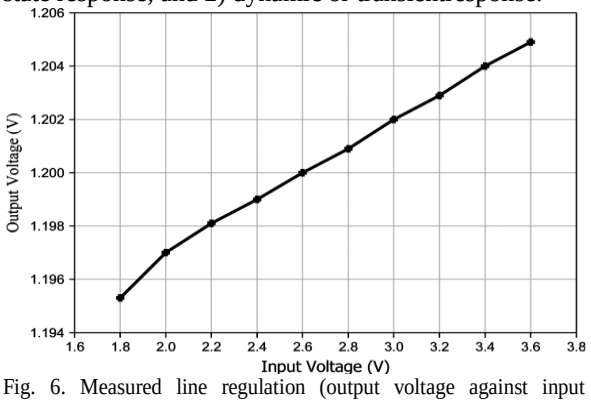

Fig. 6. Measured line regulation (output voltage against input voltage) at load current of 500 mA.

VI. CONCLUSION

This paper presented a digital dc-dc converter with predictive and feed forward control. Expectedcomparison with the conventional PID controller, the proposed PFPID controller has a lower overshoot and a shorter settling time. This is because the predictive term and its corresponding gain coefficient introduce LHP zero to increase the unity-gain frequency and improve the phase margin of the control-to-output response of the digital dc-dc converter.

We have also proposed a feed forward control by evaluating the change in the inductor current during the on and off time of the power transistors. This feed forward control with its coefficient limits the overshoot and undershoot during the transient period of the digital dc-dc converter. The design was verified on silicon with a prototype of a digital dc-dc converter fabricated in CMOS 0.18 m process.

REFERENCES

1. A. P. Dancy, R. Amirtharajah, and A. P. Chandrakasan, "High-efficiencymultiple-output DC-DC conversion for low-voltage systems,"*IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 3, pp.252–263, Jun. 2000.
2. G. Wei and M. Horowitz, "A low power switching power supply forself-clocked system," in *Proc. IEEE Int. Symp. LowPower Electron.Design*, Monterey, CA, 1996, pp. 313–317.
3. L. Corradini, A. Babazadeh, A. Bjeletic, and D. Maksimovic, "Currentlimited time-optimal response in digitally controlled DC-DC converters,"*IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2869–2880,Nov. 2010.
4. M. Shirazi, R. Zane, and D. Maksimovic, "An autotuning digital controller for DC-DC power converters based on online frequency responsemeasurement," *IEEE Trans. Power Electron.*, vol. 24, no. 11,pp. 2578–2588, Nov. 2009.
5. O. Trescases, G. Wei, A. Prodic, and W. T. Ng, "Predictive efficiencyoptimization for DC-DC converterswith highly dynamic digital loads,"*IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1859–1869, Jul. 2008.
6. F. Luo and D. Ma, "An integrated switching DC-DC converter withdual-mode pulse-train/PWM control," *IEEE Trans. Circuits Syst. II,Exp. Briefs*, vol. 56, no. 2, pp. 152–156, Feb. 2009.
7. R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*,2nd ed. Norwell,MA:KluwerAcademic, 2001, pp. 293–321.
8. F. Guinjoan, J. Calvente, A. Poveda, and L. Martinez, "Large-signalmodeling and simulation of switching DC-DC converters," *IEEETrans. Power Electron.*, vol. 12, no. 3, pp. 485–494, May 1997.
9. R. D. Middlebrook and S. Cuk, "Modelling and analysis methods forDC-to-DC switching converters," in *Proc. IEEE Int. Semicond. Power Converter Conf.*, 1977, pp. 90–111.
10. R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching-converter power stages," *Int. J. Electron.*, vol. 42, no.6, pp. 521–550, Jun. 1977.
11. R.Naim, G. Weiss, and S. Ben-Yaakov, " control applied to boostconverters," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 677–683,Jul. 1997.
12. D. Ma,W. Ki, and C. Tsui, "An integrated one-cycle control buck converterwith adaptive output and dual loops for output error correction,"*IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 140–149, Jan. 2004.
13. K. Smedley and S. Cuk, "One-cycle control of switching converters,"*IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 625–633, Nov. 1995.
14. L. Rossetto, G. Spiazzi, P. Tenti, B. Fabiano, and C. Licitra, "Fastresponsehigh-quality rectifier with sliding mode control," *IEEE Trans.Power Electron.*, vol. 9, no. 2, pp. 146–152, Mar. 1994.
15. L. Corradini, E. Orietti, P. Mattavelli, and S. Saggini, "Digital hystereticvoltage-mode control for DC-DC converters based on asynchronoussampling," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp.201–211, Jan. 2009.
16. W. Burns and T.Wilson, "State trajectories used to observe and controlthe behavior of a voltage step-up DC-to-DC converter," *IEEE Trans.Aerosp. Electron. Syst.*, vol. AES-12, no. 6, pp. 706–717, Nov. 1976.
17. G. Feng, E. Meyer, and Y. F. Liu, "A new digital control algorithm toachieve optimal dynamic performance in DC-to-DC converters," *IEEETrans. Power Electron.*, vol. 22, no. 4, pp. 1489–1498, Jul. 2007.
18. M. Barai, S. Sengupta, and J. Biswas, "Digital controller for DVS-enabledDC-DC converter," *IEEE Trans. Power Electron.*, vol. 25, no. 3,pp. 557–573, Mar. 2010.
19. A. Babazadeh and D. Maksimovic, "Hybrid digital adaptive control forfast transient response in synchronous buck DC-DC converters," *IEEETrans. Power Electron.*, vol. 24, no. 11, pp. 2625–2638, Nov. 2009.
20. V. Michal, C. Premont, G. Pillonet, and N. Abouchi, "Zero-derivativemethod of analog controller design applied to step-down DC-DC converters,"in *Proc. IEEE ISCAS Conf.*, 2010, pp. 2920–2923.
21. J. Xiao, A. V. Peterchev, J. Zhang, and S. R. Sanders, "A 4- A quiescentcurrent dual-mode digitally controlled buck converter IC for cellularphone applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 12,pp. 2342–2348, Dec. 2004.
22. B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequencyPWM controller IC for DC-DC converters," *IEEE Trans.Power Electron.*, vol. 18, pp. 438–446, Jan. 2003.
23. A. V. Peterchev and S. R. Sanders, "Quantization resolution and limitcycling in digitally controlled PWM converters," in *Proc. IEEE PowerElectron. Spec. Conf.*, 2001, vol. 2, pp. 465–471.
24. E. G. Soenen, A. Roth, J. Shi, M. Kinyua, J. Gaither, and E. Ortynska,"A robust digital DC-DC converter with rail-to-rail output range in 40nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2010,pp. 198–199.
25. O. Trescases, A. Prodic, and W. T. Ng, "Digitally controlled currentmodeDC-DC converter IC," *IEEE Trans.Circuits Syst. I, Reg. Papers*,vol. 58, no. 1, pp. 219–231, Jan. 2011.