Dual-Buck Structured High-Reliability and High-Efficiency Buck-Boost Inverter

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Abstract— In this paper, dual-buck structured single-stage, single-phase buck–boost inverters that use power MOSFETs are presented. The proposed inverters require fewer number of switches, and achieve inverting action through single stage operation. They have no shoot-through problem; therefore, high system reliability can be obtained. The dead time in PWM signals can be minimized or eliminated, which improving the quality of the output ac voltages and increasing the efficiency. In the proposed inverters, MOSFETs can be used without reverse-recovery issues of their body diodes to boost the efficiency and increase the switching frequency. The Simulation results of this system indicates small distortion in ac voltage form due to no or small dead time requirements in the switching signals. To regulate the ac voltage waveform a cuk converter topology along with a controller section is introduced. The constant output voltage is obtained for a wide variation of inputs which is essential for renewable farm-based AC micro-grids.

Index Terms— *Buck-Boost inverter, Dual-Buck, high efficiency, high reliability, single-stage.*

I. INTRODUCTION

The full-bridge inverter is a popular topology used for power inversion applications. However, its output peak ac voltage does not exceed the input DC voltage. Therefore, for applications in which the output peak ac voltage needs to be greater than the input DC voltage, an additional boost or buck–boost DC–DC converter is needed at the front end for voltage boosting. This forms a two-stage inverter system which makes the system bulky. Two-stage inverters are time-tested and work well. However, they have certain disadvantages such as a large number of power processing stages, complex control, high cost, low reliability and low efficiency. In a single-stage, an output peak ac voltage greater than the input DC voltage can be obtained by using a full-bridge inverter followed by a low frequency step-up transformer. However, the bulky transformer increases the volume, loss, and system cost. To overcome some of the mentioned drawbacks, single-stage buck-boost inverters were introduced. The Dual - Buck based topology guarantees increased robustness since the dc link cannot be short circuited by a shoot through event. The Dual Buck structure is given below,
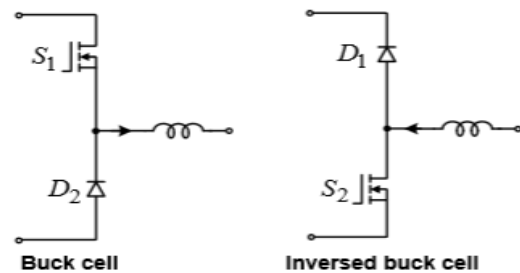

Fig.1: Dual Buck Structure

The basic concept of a dual-buck inverter is introduced in this paper. Its basic switching cell is a unidirectional buck circuit, which consists of one switch and an external diode connected in series to it. Therefore, no short circuit is possible, and high reliability can be achieved. The inductor current does not flow through the body diodes of the switches, but freewheels through the external diodes (D1 and D2). Therefore, the reverse-recovery issues and related losses can be reduced by choosing external freewheeling diodes with good reverse-recovery features, and a MOSFET can be used to boost the efficiency and increase the switching frequency without reliability issues. In this circuit, the body diodes of switches are not shown because they do not conduct current. Dual-buck structured converters use the structures shown in Fig. 2 as the basic switching cells. In recent years, dual-buck structured dc–ac inverters, and multilevel converters have been proposed, through significant efforts in research and development. In this paper, novel dual-buck structured buck–boost inverters are proposed to realize high efficiency and reliability. They are symmetrical single-stage inverters.
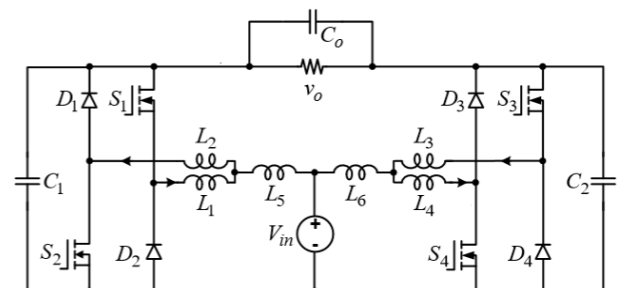

Fig 2-Single phase single stage dual buck inverter

Fig. 2 shows the circuit diagram of the dual buck single stage single-phase inverter. It is developed using the half-bridge dual-buck structure and boost inverter. The single-

phase inverter can be further expanded into a three-phase inverter in future. It consists six inductors (L1–L6), two leg capacitors (C1, C2), four switches (S1–S4) (mosfets), four diodes (D1–D4), and one output capacitor (Co). C1 and C2 serve both as filter and snubber capacitors, and Co filters the voltage ripples of output voltage. L1–L6 are filter inductors; in addition to filtering, L1–L4 also protect against shoot-through problem; therefore, the dead time between the switches can be minimized or eliminated. In addition, L1–L4 prevent inductor currents from flowing through the body diodes of S1–S4. The inductor current freewheels through D1–D4, which are chosen externally.
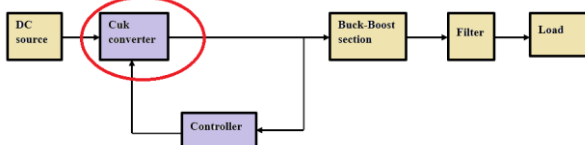
II. PROPOSED SYSTEM

Fig.3: Block diagram representation of the proposed system

In the proposed system the series inductors are removed and an additional cuk converter is introduced. The dc source is given to the input of cuk converter. The wide variation of input dc is controlled by cuk converter controlling section. The controlled output is provided for the single stage buck boost operation. Filter capacitor is used to reduce ripples. An equational controller is additionally used to control the varying input of cuk topology in order to obtain the constant output (Vin2). The figure below shows the circuit diagram of the proposed system.
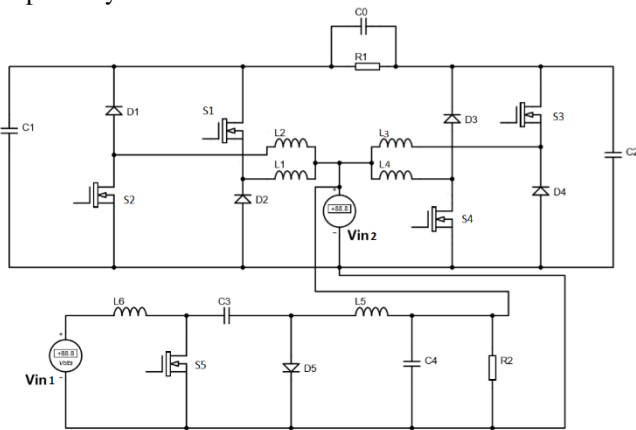

Fig.4: Proposed system circuit diagram.

At any given time, two switches operate complementarily at high frequency and with a finite dead time for the buck boost section. The dead time is needed to decrease the circulating currents. For the positive half-cycle of the output voltage (Vo > 0), S1 and S2 operate at high frequency, whereas S3 is kept ON, and S4 is kept OFF. For Vo< 0, S3 and S4 operate at high frequency, whereas S1 is kept ON, and S2 is kept OFF. Within a switching cycle, the inverter has three switching modes, as discussed below,

1. Mode 1: S2 is ON, and L2 stores energy from the input source.
2. Mode 2: This is the dead-time mode; S1 and S2 are both OFF.
3. Mode 3: S1 is ON, and L2 delivers the stored energy to the load and C1.

During the positive half cycle of the AC output voltage, Vo>0

$$v_{C_1} = V_{in} + V_o \sin(\omega t) = \frac{V_{in}}{1 - d_1(t)} \quad (1)$$

$$v_{C_2} = V_{in} \quad (2)$$

Similarly, for V0<0 we obtain,

$$v_{C_1} = V_{in} \quad (3)$$

$$v_{C_2} = V_{in} + V_o \sin(\omega t - \pi) = \frac{V_{in}}{1 - d_2(t)} \quad (4)$$

where Vc1 and Vc2 are the voltages of C1 and C2, respectively; Vin is the input DC voltage, Vo is the peak of vo, and d1(t), d2(t) are the duty ratios of S2 and S4, respectively

From (1)-(4) the duty ratios become,

$$d_1(t) = \frac{V_o \sin(\omega t)}{V_{in} + V_o \sin(\omega t)} , \quad v_o > 0 \quad (5)$$
$$d_2(t) = 0$$

$$d_1(t) = 0$$
$$d_2(t) = \frac{V_o \sin(\omega t - \pi)}{V_{in} + V_o \sin(\omega t - \pi)} , \quad v_o < 0 \quad (6)$$

The output voltage is the difference between two capacitor voltages.

$$v_o = v_{C_1} - v_{C_2} = V_o \sin(\omega t)$$

III. SIMULATION RESULTS OF THE SYSTEM

The existing dual buck stand- alone single- stage single-phase inverter is simulated in MATLAB/SIMULINK. The switches are triggered by means of PWM switching strategy having no dead time. The output AC waveform is distorted in buck and boost action. The simulation model of existing system is shown in Fig.5.
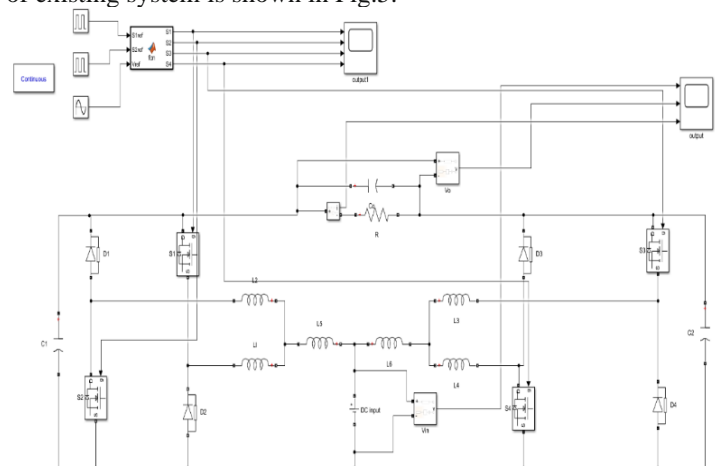

Fig-5: Simulink model of existing system

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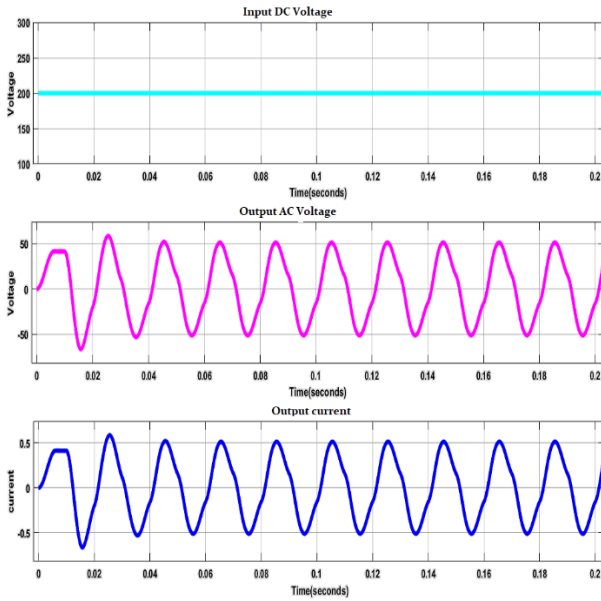205

Fig-6: Input and output waveforms of existing system

The modified dual buck stand- alone single- stage single-phase inverter is also simulated in MATLAB/SIMULINK. Here an additional cuk converter and a controller section is introduced. The switches are triggered by means of PWM switching strategy having no dead time. The output AC waveform is not distorted in both buck and boost action. For comparing buck operation is explained here. The simulation model is shown in Fig.7.
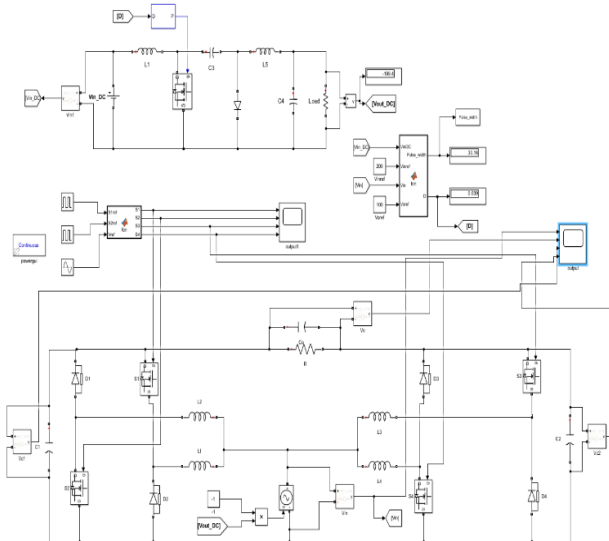

Fig-7: Simulink model of the proposed system.

Here series inductors are removed from main circuit as modification which have less effect in the overall buck boost action. The input used is 200V dc and output is of 100V ac. The input and output waveforms are follows,
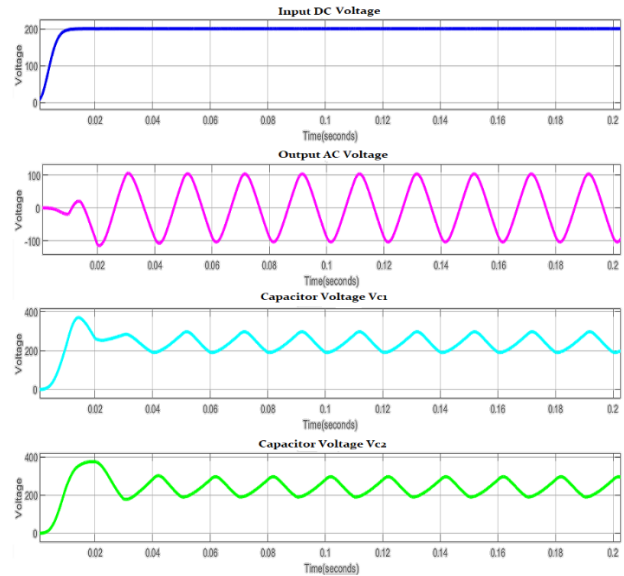

Fig-8: Output waveforms of proposed system.

The varying input is provided to the cuk converter with Vin reference is chosen as 200V and Vo reference as 100V.The output of cuk converter is provided as the input to buck boost section (Vin reference value is 200V DC). Duty ratio is less than 0.5 for buck action and greater than 0.5 for boost action. From the figure the capacitor voltage is initially charged to 200V (input voltage). During the positive half cycle of AC output voltage Vc1 goes positive(charges)and during the negative half cycle of output AC voltage capacitor Vc2 goes positive. The operation of cuk topology is based on capacitive energy transfer which is more energy efficient. By THD improvement the power quality of the system is made higher. The THD analysis of the existing and proposed single-stage inverter is given below,
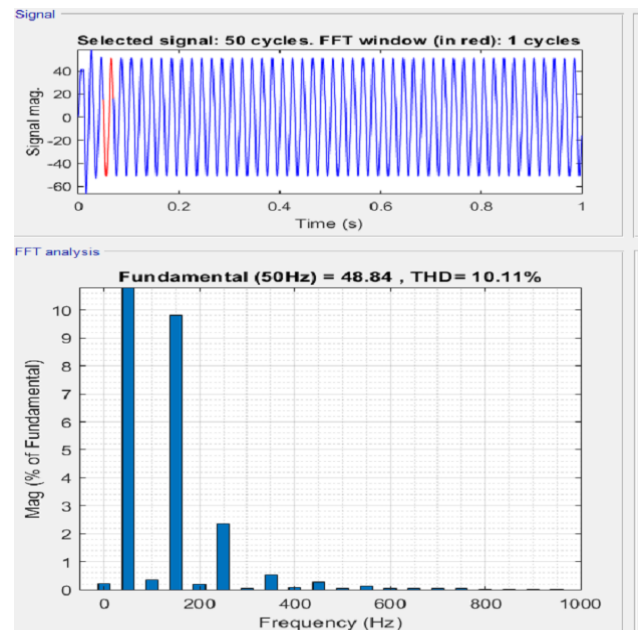

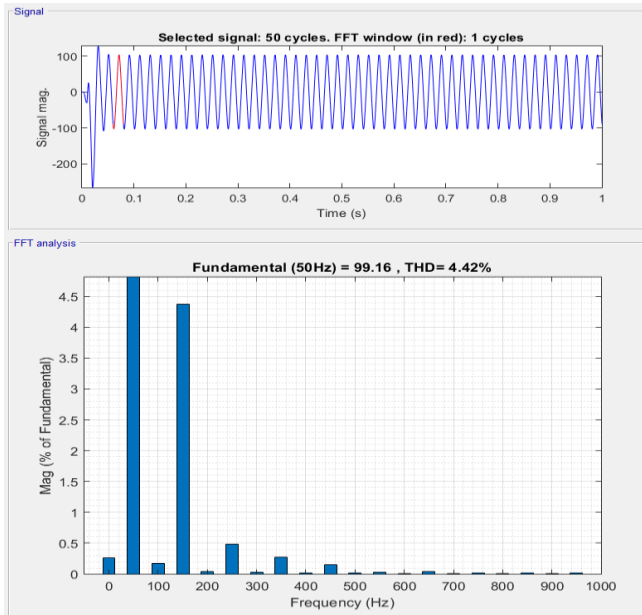Fig-9: FFT analysis of the existing system.

Fig-10: FFT analysis of proposed system

From the FFT analysis the total harmonic distortion of the proposed system is reduced to 4.42% from 10.11%. The inverter output shows no distortions and it is controllable which is essential for various applications.

DESIGN PARAMETERS

Parameters	Values
C_1-C_2	20mF
C_0	8μF
C_3-C_4	5μF
R_1	100Ω
R_2	0.5Ω
L_1-L_4	0.6mH
L_5-L_6	500μH

IV.   CONCLUSION

In this paper, a single-stage single -phase dual buck structured buck–boost inverter is presented. The single-phase inverter is studied and analyzed various features like high reliability, low output ac voltage distortion and high efficiency. The converter can be designed to work at higher switching frequencies to decrease the volume of passive components and a small high-frequency common-mode voltage, which makes the proposed topology suitable for PV inverter applications. The existing system shows little distortions in its output voltage waveform (THD-10.11). To reduce these distortions, a controller section is introduced. In addition to this a cuk converter is provided to the input section of buck boost inverter to get constant output with a wide variations in input. This is applicable to photo voltaic stand-alone power systems which require stable output.

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