Dual-Inverter Fed Induction Motor Drive using Optimal Pulse Width Modulation

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***Abstract*— This paper presents the synchronous optimal pulse width modulation (SOP) for control of medium–voltage induction motor drives using dual inverters at low switching frequency. In case of medium voltage high-power drives, low device switching frequency is preferred to reduce the switching losses of power semiconductor devices and also the system efficiency. The goal of our study is to achieve low device switching frequency, minimal harmonic distortion of machine stator currents using SOP technique. The aim is to select the switching angles of two inverters for performing optimization and thus the harmonic distortion of stator current can be minimized. This paper discusses about three-level dual inverter fed induction motor drives and five-level dual inverter fed induction motor drive.**

Keywords- Medium voltage drives, Dual Inverter, Synchronous Optimal Pulse Width Modulation (SOP), Space Vector Modulation (SVM).

I. INTRODUCTION

Medium-voltage ac drives produce hundreds of times greater power output than the smaller drives. Medium voltage drives operate at higher supply voltages to obtain lower losses and use smaller cabels that add up to better overall drive efficiency, hence lower system cost. A major advantage of medium voltage over lower voltage drives is lower current flow for a given power output. Medium voltage ac drives based on voltage source inverters are in increasing demand for various industrial applications. Inverters for medium voltage drives operate at reduced switching frequency so as to restrain the dynamic losses of the power semiconductor devices.

Multilevel converters (MLCs) have developed as popular choice for medium voltage (MV) high-power applications due to several obvious advantages [1]–[5]. The popular MLC topologies are neutral-point or diode-clamped converters (NPC), flying-capacitor converters and cascaded H-Bridge converters (CHB). With this topology, it is probable to achieve three-level (3L) operation with half of dc-link voltage and without

any neutral-point fluctuations compared to 3L-NPC topology. Similarly, dual three-level (D3L) inverter configuration with a single dc-link voltage was proposed for five-level (5L) operation. The circuit diagram for dual 3L and 5L is as shown in Figure.1. The major advantage of dual-inverter topologies over other topologies is minimal requirement of dc sources. Additional merit of dual-inverter fed drives is the availability of higher redundant switching state [6]-[10] combinations compared to single-inverter fed drives for similar output voltage levels. The main drawback of dual-inverter topologies is requirement of a common-mode inductor in series with machine phase windings.

Space vector modulation (SVM) is considered as a powerful technique to inflict low harmonic content in machine windings. Using SVM at low switching frequency leads to improper high harmonic distortion of the machine currents [11], [12]. A method to obtain very low switching frequency operation simultaneously reduces low harmonic distortion using synchronous optimal modulation (SOP) [13]-[15] to 20 percentages without sacrificing the harmonic content. The application to a five level inverter is discussed in this paper

Section II discusses the Synchronous optimal PWM control and the appropriate objective function. Optimization strategies for three- and five-level inverters Induction Motor are developed in section III. The performances of three-level and five-level inverters fed Induction Motor are shown in section IV. Section V discusses the conclusion of five-level inverter drive using synchronous optimal control.

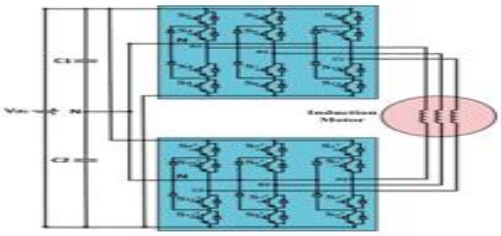

Figure 1. D3L inverter

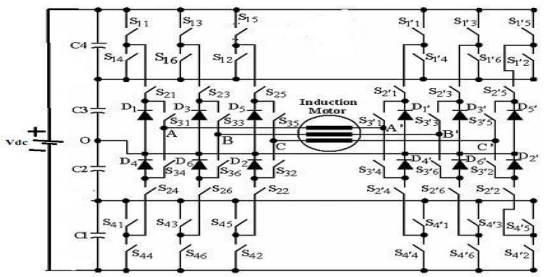

Figure 2. D5L inverter.

II. SYNCHRONOUS OPTIMAL PWM CONTROL

Synchronous optimal PWM is an emerging strategy for the control of medium-voltage drives. In this method, the pulse patterns (sets of switching instants or angles) are designed in an offline procedure assuming steady-state conditions. The switching frequency is synchronized with the fundamental frequency of the voltage waveform. Hence, the pulse number

$$N = \mathrm{mod}\left(\frac{f_{s\,max}}{f_1}\right)$$

$f_{s,max}$ is the maximum switching frequency, f_1 is the fundamental frequency of the voltage waveform.

The switching angles over one fundamental period are optimized for each steady-state operating point while minimizing the currentdistortion. Synchronous optimal PWM is adopted for modulation index values above 0.3. For modulation index values below 0.3, the number of commutations per fundamental period is very high. This makes a performance difficult. Also, the difference in distortion between SVM and synchronous optimal control is negligible in this range. Therefore, SVM is adopted for modulation index values below 0.3.

To generate the optimal pulse patterns, the optimum values of switching angles are calculated offline using computer programming. The following conditions are satisfied:

1. Harmonic distortion to be minimal
2. Consecutive switching angles to be sufficiently separated for the minimum on and off times of the switches
3. Continuity of the switching angles within the modulation index range associated to a given pulse number.

The pre-determined optimal switching angles are stored in a memory table as complete patterns P(m, N). These patterns are functions of the modulation index m and the pulse number N. The modulation index m is proportional to the magnitude u* of the reference voltage vector u*. A parameter pair (m, N) selects the corresponding pulse pattern P(m, N). This pattern is fed to the modulator as shown in Fig. 2. The modulator converts the switching angles α_i defined by P(m, N) to discrete switching state vectors u_k. This requires the phase angle arg(u*) of the reference voltage vector as an input in the switching transitions. The fundamental frequency signal f_1 translates the resulting switching transitions within the fundamental period. The fundamental frequency signal f_1 translates the resulting switching angles α_i to switching instants $t_i = \alpha_i /(2\pi f_1)$. The modulator thus creates the sequence of switching vectors u_k as prescribed by the optimal pattern P(m,N).

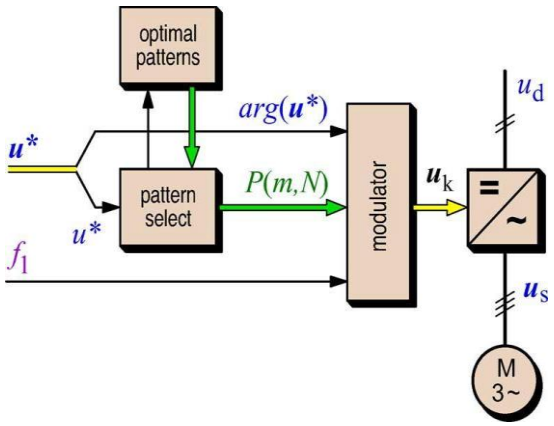

Figure 3. Synchronous optimal modulation, signal flow graph

III. PROPOSED SOP

The pulse generation for the switch is as shown in the Figure 3. based on SOP technique. The pulses are named as P1, P2 and the generated pulses are send into an Boolean function called AND operator. The pulses which are generated can be of multiple pulses or single pulse based on the time period such that in this SOP technique number of pulses can be changed. Fig3 (a),(b) represents the comparison waveform of three level and five level dual inverter.

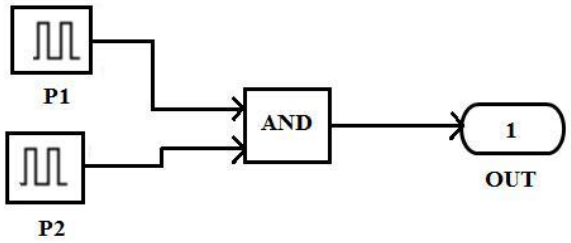

Figure 4. Pulse generation

V1 and V2 are the carrier signals, Va is reference signal is as shown in fig.3.(b). When V1 is greater than Va and V2 is greater than V2, positive pulses are generated. And the negative pulses will be generated as vice-versa.

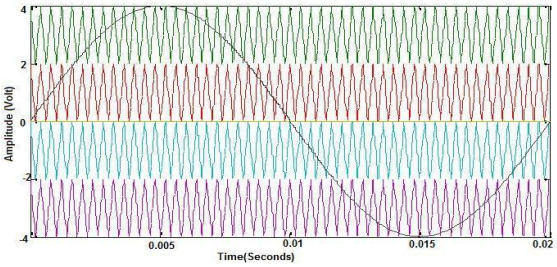

Figure 5. Signal Generation for dual 5L inverter

IV. PERFORMANCE OF THREE AND FIVE LEVEL DUAL INVERTER FED INDUCTION MOTOR DRIVE

A. Dual 3L inverter

Synchronous optimal control of the induction motor drive was verified using a three-level inverter, as shown in Figure 1(a). SOP technique generates optimal switching angles for three-level dual inverter. Optimal switching angles calculated using computer programming was stored in a microcontroller. The switching states of the switches were programmed for a modulation factor m of 0.78 and N=5.

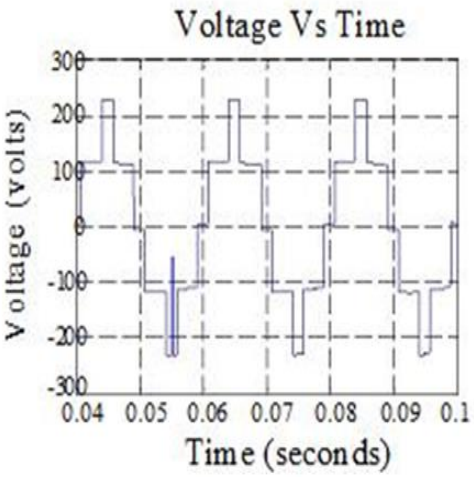

Figure 6. Voltage waveform

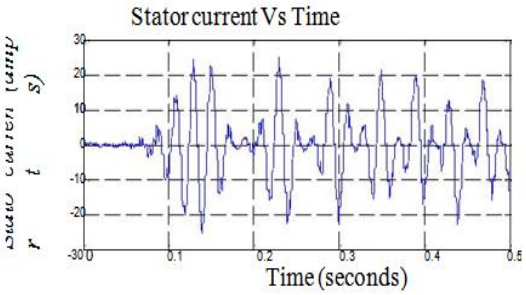

Figure 7. Stator current

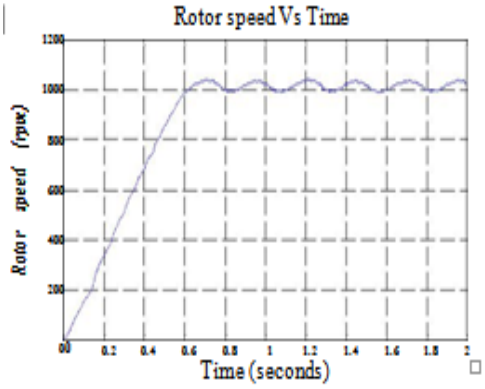

Figure 8. Rotor speed

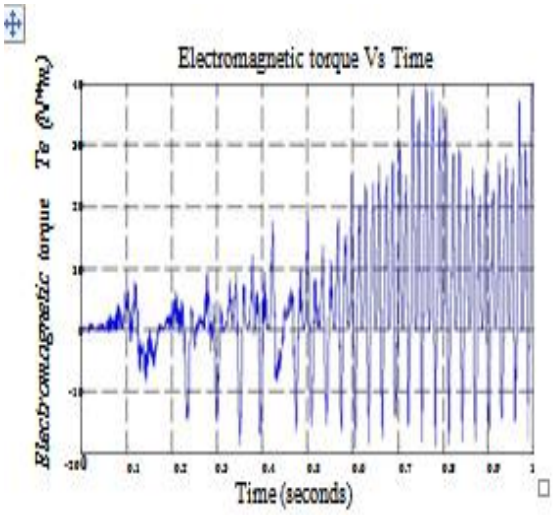

Figure 9. Electromagnetic torque

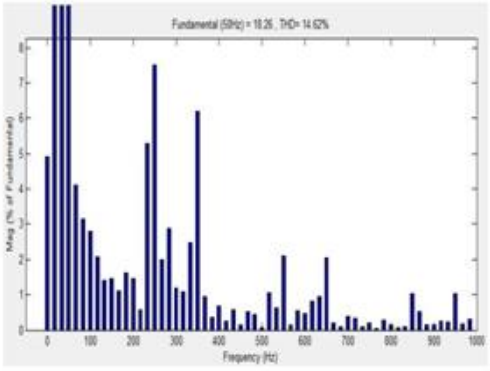

Figure 10. Harmonic spectrums of stator currents

B. Dual 5L inverter

Synchronous optimal control of the induction motor drive was verified using a five-level inverter, as shown in Fig.1 (b). The proposed SOP technique generates optimal switching angles for five-level dual inverter. Optimal switching angles are calculated and are e programmed for m = 0.65 and N=6. The input voltage for dual 5L inverter is maintained at 230 V, respectively. The output of inverters is directly connected to induction motor of 1.5KW. The load torque of 40 Nm is applied at 0.3 Seconds so that speed settles downs at 0.7 seconds. The stator current, rotor speed and electromagnetic torque are shown in Fig. 5(b)-(d), respectively. The phase voltage of 5L waveforms and stator currents are sinusoidal. The FFT analysis is analysed for a frequency of 50Hz where THD of stator currents is equal to 5.34%.

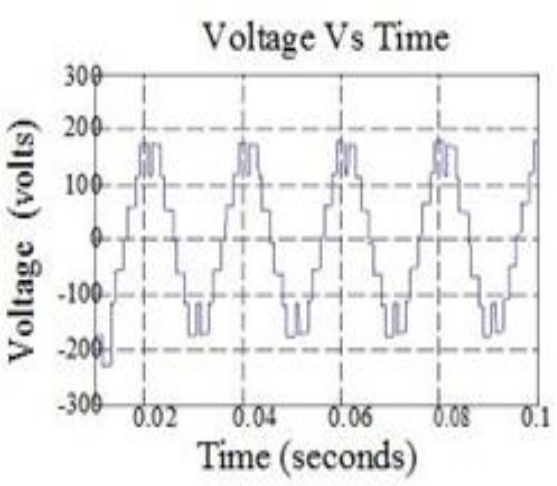

Figure 11. Voltage Waveform

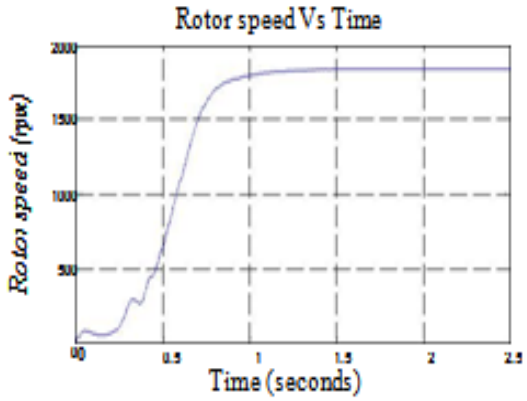

Figure 12. Rotor Speed

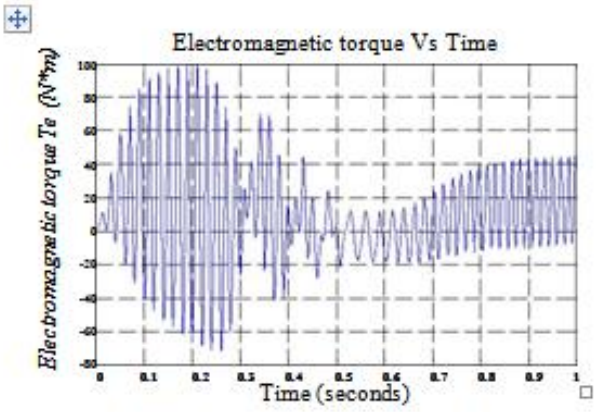

Figure 13. Electromagnetic torque

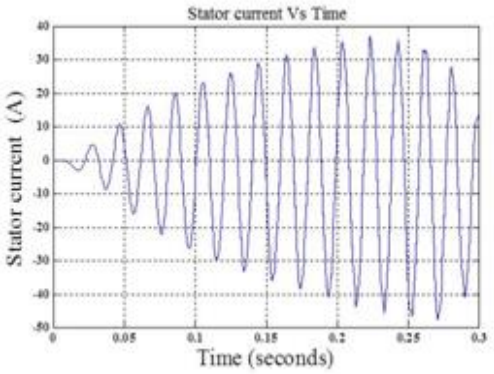

Figure 14. Stator current

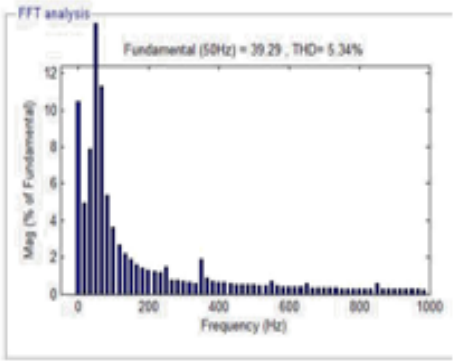

Figure 15. Harmonic spectrum of stator currents

V. CONCLUSION

machine stator currents. It enables operation at very low switching frequency and also reduces the switching frequency. This reduces the switching losses that contribute a major portion of the total losses of medium-voltage power semiconductor devices. Reducing the switching losses permits one to increase the output power of a given inverter. Dual-inverter Synchronous optimal PWM for the control of medium-voltage inverters reduces the harmonic content of the configurations for open-end winding induction motor drives require common-mode inductor. Also, MV high-power drives require low device switching frequency with high quality of machine stator currents. Therefore, SOP has been proposed to achieve minimal harmonic distortion of machine stator currents while operating semiconductor devices at low switching frequency.

REFERENCES

[1] J. Rodriguez, S. Bernet, B.Wu, J. Pontt, and S.Kouro, "Multilevel voltagesource-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron. Mag.,vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron.,vol. 49, no. 4, pp. 724–738, Aug. 2002.

[4] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 36– 44,Jan./Feb. 1999.

[5] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[6] Barry Venugopal Reddy and Veeramraju Tirumala Somasekar, "A dual inverter fed four- level open-end winding inducto motor drive with a nested rectifier-inverter," IEEE Trans. Ind.Electron., vol. 9, no.2, May 2013.

[7] K.Ramachandra Sekhar and S. Srinivas,"Discontinuous decoupled pwms for reduced current ripple in a dual two-level inverter fed open-end winding induction motor drive," IEEE Trans. Ind. Electron., vol. 28, no.5, May 2013.

[8] P.N. Tekwani, R. S. Kanchan and K.Gopukumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimination and dc-link capacitor voltage balancing using only the switching-state redundancy—Part I," IEEE Trans. Ind. Electron., vol. 54, no. 5, Oct 2007.

[9] Amarendra Edupuganti, Akshay Kumar Rathore, " New optimal pulsewidth modulation for single dc-link dual-inverter fed open-end stator winding induction motor drive," IEEE Trans. Ind. Electron., vol. 30, no.8, Aug 2015.

[10] M. R. Baiju, K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," IEEE Trans. Power Electron., vol. 19, no. 3,pp. 794–805, May 2004.

[11] V. T. Somasekhar, K. Gopakumar, E. Sivakumar, and S. Sinha, "A space vector modulation scheme for a dual two level inverter fed open-end winding induction motor drive for the elimination of zero sequence currents," EPE J., vol. 12, no. 2, pp. 26–36, 2002.

[12] J. Holtz andN.Oikonomou, "Synchronous optimal pulsewidthmodulation and stator flux trajectory control for medium-voltage drives," IEEE Trans.Ind. Appl., vol. 43, no. 2, pp. 600–608, Mar./Apr. 2007.

[13] N. Oikonomou and J. Holtz, "Closed-loop control of medium-voltage drives operated with synchronous optimal pulsewidth modulation," IEEETrans. Ind. Appl., vol. 44, no. 1, pp. 115 –123, Jan./Feb. 2008.

[14] A. Rathore, J. Holtz, and T. Boller, "Synchronous optimal pulsewidth modulation for low-switching-frequency control of medium-voltage multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2374–2381, Jul. 2010.

[15] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives,"IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 6– 44,Jan./Feb. 1999.