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Dual-Rail Domino Logic Circuits with PVT Variations in VDSM Technology

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Abstract: *This paper presents dual-rail domino logic circuits with less power consumption and high speed performance. Advances in dynamic circuits are driven by the need to meet high performance targets in deep- sub- micron designs. Speed critical paths often deploy dynamic logic to meet speed requirements. Performance gain over static logic becomes even larger as the number of inputs to the logic grows. Wide fan-in dynamic logic such as domino is often used in performance critical paths, to achieve high speeds where static CMOS fails to meet performance objectives. However, domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS gates. The low power and error free operation of domino logic circuits is a major challenge in the current CMOS technologies. Keeping in view of the above stated problems in previous existing designs, novel energy-efficient domino circuit techniques are proposed. The proposed circuit techniques reduced the dynamic switching power consumption, short-circuit current overhead, idle mode leakage power consumption and enhanced evaluation speed in domino logic circuits. Also regarding performance, these techniques minimized the power-delay product (PDP) as compared to the standard circuits in very deep sub micron CMOS technology.*

I.INTRODUCTION

Dynamic domino logic circuits are widely used in modern VLSI circuits. The dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. This work discusses several domino circuit design techniques to reduce the power dissipation of domino logic. In this paper novel energy-efficient domino circuit techniques are proposed.

This paper is organized as follows. In section II, Dual-rail domino circuit with self- timed precharge scheme is proposed. Section III describes the effect of PVT variations on domino logic presented in section II. Then conclusions are presented in section IV.

II.DUAL-RAIL DOMINO FOOTLESS CIRCUIT WITH SELF-TIMED PRECHARGE SCHEME (DRDFSTP):

Conventional domino circuits: In this section, several conventional domino circuits with their own clocking schemes are briefly reviewed.

A. Dynamic DCVSL Footed Circuit (DDCVSLF):

Fig.1 shows AND/NAND dynamic DCVSL Footed circuit. The operation of this circuit is divided into two major phases, namely precharge and evaluation phase, with the mode of operation is determined by the precharge signal P. When P goes low, all gates are precharged simultaneously. The precharge transistors Mp and the foot transistor Mn are turned on and off, respectively, and the outputs of the n-type dynamic gates are charged to V_{dd}, and the outputs of the inverters are set to zero. When P goes high, Mp and Mn are turned off and on, respectively, and the circuit enters the evaluation phase. The incoming data inputs may conditionally conduct the pull-down network (PDN) to discharge the dynamic gate, and the output of the inverter makes a low-to-high transition accordingly. One of the disadvantages of this kind of domino circuit is that the existence foot transistor slows the gates somewhat, as it presents an extra series resistance

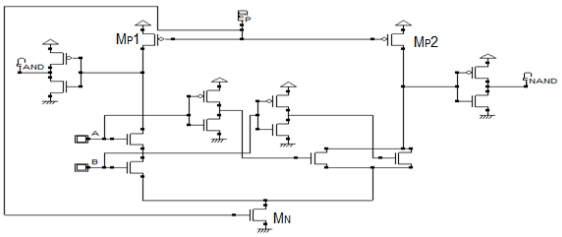

Fig 1: Dynamic DCVSL AND/NAND Footed gate

B. Dynamic DCVSL Footless Circuit (DDCVSLFL):

Fig. 2 shows AND/NAND dynamic DCVSL Footless circuit. Two benefits come from the usage of footless domino gates: improved pull-down speed and reduced precharge signal load. Elimination of the foot transistor does not affect the operation of the evaluation phase. Main disadvantage is simultaneous precharge will cause short-circuit current.

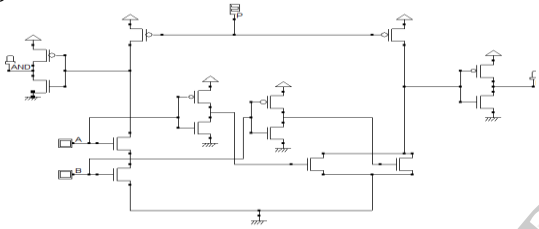

Fig 2: Dynamic DCVSL AND/NAND Footless gate

C. Delayed-Reset Domino Circuit (DRD):

Fig. 3 illustrates the delayed-reset domino AND/NAND circuit . All domino gates are footless, except those gates connected to the primary inputs. The benefits that come from the usage of footless domino gates are improved pull-down speed and reduced precharge signal load. However, simultaneous precharge will cause short-circuit current. To ensure a correct operation, the precharge signal's falling edge of a gate should be delayed until all its inputs going low. This is why consecutive logic stages are driven by a series of delayed precharge signals. One side benefit of such a delayed-reset scheme is that the peak of precharge current is reduced. However, the use of delay elements, together with the need of both footed and footless cell libraries tends to increase design complexity.

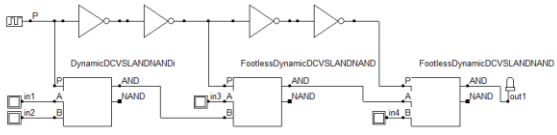

Figure 3: The delayed-reset domino AND/NAND circuit

D. Dual-Rail Data-Driven Dynamic Logic (D^4L):

D^4L circuit uses input signals instead of precharge signal for correct precharge and evaluation sequencing. Correspondingly, clock-buffering and clock-distribution problems can be eliminated. Furthermore, the foot transistor can be eliminated without causing a short-circuit problem. A D^4L two-input AND/NAND gate is shown in Fig. 4. In this structure, a signal pair (B, B') is used for precharging corresponding gate, instead of a precharge signal. When the precharging wave reaches the input of D^4L gate, set them to low and precharge the outputs to high. In the evaluation phase, one of the rails in (B, B') and (A, A') is set to high and prevent short-circuit between V_{dd} and ground in this phase. However, due to the extra load added to input signals, the speed performance of the circuit is somewhat degraded.

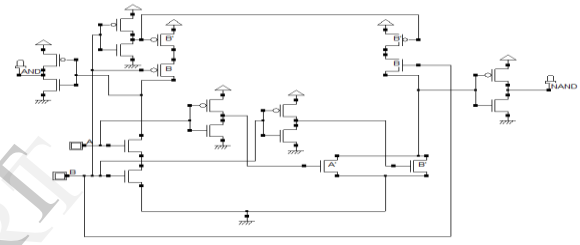

Figure 4: Dual-Rail Data-Driven Dynamic AND/NAND Logic

E. FOOTLESS DUAL-RAIL DOMINO CIRCUIT WITH SELF- TIMED PRECHARGE SCHEME (FDRDCWSTPS):

The presence of the foot transistor in the conventional dynamic DCVSL circuit presents an extra series resistance. To safely remove the transistor, two constraints must be met: (1) gate changes to evaluation phase before valid input come; (2) gate changes to precharge phase only after inputs change to zero. We propose a footless dual-rail domino circuit with self-timed precharge scheme to realize a high performance footless domino circuit while meeting the constraints mentioned above. Fig 5 shows the AND/NAND gate of the proposed footless dual-rail domino circuit with self-timed precharge scheme. The self-timed precharge control logic consists of static CMOS inverts whose source of NMOS transistors are tied to input signals, which generate sub- precharge signals (PC1-PC4) from precharge signal P in cases of the corresponding input signals are zero. The PMOS precharge tree above the pull down network (PDN) is used for

precharging the corresponding gate.

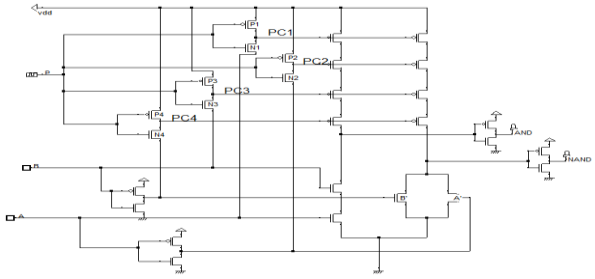

Figure 5: Footless dual-rail domino AND-NAND gate with self timed precharge scheme

III. Simulation results:

In this work, we have implemented a Dynamic DCVSL circuit, Dual-Rail Data-Driven Dynamic Logic and a proposed circuit Dual-Rail Domino Footless Circuit with Self-Timed Precharge Scheme. The results of simulation are shown in the below TABLES1-3

Table1: AND/NAND GATE

S. No:	Technique	Power	Critical Delay	PDP(10^{-15}sec)	Area
1	DDCVSLF	7.6	0.088	0.6688	69.62
2	DDCVSLFL	152	0.025	3.8	65.41
3	DRD	205	0.137	28.085	252.9
4	D4L	72.55	0.111	8.053606	93.3
5	FDRDCWSTPS	7.676	0.042	0.322392	177.6

Table2: OR/NOR GATE

S. No:	Technique	Power	Critical Delay	PDP(10^{-15}sec)	Area
1	DDCVSLF	7.58	0.087	0.65946	74.82
2	DDCVSLFL	145	0.090	13.05	66.59
3	DRD	220	0.403	88.66	290
4	D4L	10.16	0.112	1.138256	78.48
5	FDRDCWSTPS	7.583	0.042	0.318486	130.18

Table3: XOR/XNOR GATE

S.No:	Technique	Power	Critical Delay	PDP(10^{-15}sec)	Area
1	DDCVSLF	11.7	0.032	0.3744	99.2
2	DDCVSLFL	99.02	0.032	3.1687	92.17
3	DRD	231	0.091	21.021	391.9
4	D4L	16.8	0.029	0.48725	100.5
5	FDRDCWSTPS	11.64	0.04	0.46568	200.13

IV. PROCESS, VOLTAGE AND TEMPERATURE VARIATIONS (PVT) ON THE PERFORMANCE OF DOMINO LOGIC:

The effect of PVT variations on the domino logic circuit techniques which are explained in section II are studied and analysed in this section. The process variations considered are VTHO(Threshold voltage at zero bias), TOXE (Oxide layer thickness) and UO

(Carrier Mobility). The PVT variances on the domino logic in section II are given below in Tables4-6.

Table 4.PROCESS VARIATIONS (V AND T CONSTANT)

BENCHMARKCIRCUITS		AND/NAND		OR/NOR		XOR/XNOR	
		VTHO=0.3 TOXE=0.7 UO=0.030	VTHO=0.4 TOXE=1.6 U0=0.8	VTHO=0.3 TOXE=0.7 UO=0.030	VTHO=0.4 TOXE=1.6 U0=0.8	VTHO=0.3 TOXE=0.7 UO=0.030	VTHO=0.4 TOXE=1.6 U0=0.8
DDCVSLF	POWER DISSIPATION(µW)	7.520	7.623	7.565	7.746	11.330	11.84
	ION(ma)	0.120	0.358	0.120	0.358	0.120	0.358
	IOFF(na)	2	0	1	0	2	0
DDCVSLFL	POWER DISSIPATION(µW)	11.958	17.044	11.325	15.834	15.910	22.471
	ION(ma)	0.051	0.139	0.120	0.358	0.51	0.153
	IOFF(na)	1	0	2	0	1	0
DRD	POWER DISSIPATION(µW)	7.90	3.604	0.004	0.004	29.521	4.719
	ION(ma)	0.449	0.438	0.304	0.280	2.794	0.438
	IOFF(na)	6	1	2	0	37	1
D^4L	POWER DISSIPATION(µW)	8.109	13.437	0.234	0.227	7.254	12.033
	ION(ma)	0.120	0.358	0.120	0.358	0.12	0.358
	IOFF(na)	2	0	2	0	2	0
FDRDCWSTPS	POWER DISSIPATION(µW)	8.109	13.437	0.234	0.227	7.254	12.033
	ION(ma)	0.120	0.358	0.120	0.358	0.12	0.358
	IOFF(na)	2	0	2	0	2	0

Table 5.VOLTAGE VARIATIONS (P AND T CONSTANT)

BENCHMARK CIRCUITS		AND/NAND			OR/NOR			XOR/XNOR		
		Vdd=0.7	Vdd=0.8	Vdd=1	Vdd=0.7	Vdd=0.8	Vdd=1	Vdd=0.7	Vdd=0.8	Vdd=1
DDCVSLF	POWER DISSIPATION(µW)	7.152	7.153	7.6	7.141	7.524	7.58	9.345	11.809	11.7
	ION(ma)	0.131	0.171	0.250	0.131	0.171	0.250	0.131	0.171	0.250
	IOFF(na)	0	0	0	0	0	0	0	0	0
DDCVSLFL	POWER DISSIPATION(µW)	100.714	101.621	152	102.185	145.317	145	98.264	99.821	99.023
	ION(ma)	0.131	0.171	0.250	0.131	0.171	0.250	0.131	0.171	0.250
	IOFF(na)	0	0	0	0	0	0	0	0	0
DRD	POWER DISSIPATION(µW)	67.053	102	205	94.217	94.712	220	220.013	230.983	231
	ION(ma)	0.131	0.171	0.107	0.131	0.171	0.107	0.131	0.171	0.107
	IOFF(na)	0	0	0	0	0	0	0	0	0
D^4L	POWER DISSIPATION(µW)	54.187	72.868	72.555	9.127	9.217	10.163	14.717	16.504	16.802
	ION(ma)	0.131	0.171	0.250	0.131	0.171	0.250	0.131	0.171	0.250
	IOFF(na)	0	0	0	0	0	0	0	0	0
FDRDCWSTPS	POWER DISSIPATION(µW)	7.885	7.278	7.676	7.317	7.155	7.583	11.521	11.504	11.642
	ION(ma)	0.131	0.171	0.250	0.131	0.171	0.250	0.131	0.171	0.250
	IOFF(na)	0	0	0	0	0	0	0	0	0

Table 6.TEMPERATURE VARIATIONS (P AND V CONSTANT)

BENCHMARK CIRCUITS		AND/NAND			OR/NOR			XOR/XNOR		
		T= -73	T= 27	T= 127	T= -73	T= 27	T=127	T= -73	T= 27	T= 127
DDCVSLF	POWER DISSIPATION(µW)	7.503	7.6	7.768	7.425	7.58	8.025	11.369	11.7	11.691
	ION(ma)	0.445	0.250	0.163	0.445	0.250	0.163	0.445	0.250	0.163
	IOFF(na)	0	0	27	0	0	27	0	0	27
DDCVSLFL	POWER DISSIPATION(µW)	246	152	108	247	145	112	169	99.023	77.078
	ION(ma)	0.445	0.250	0.163	0.445	0.250	0.163	0.445	0.250	0.163
	IOFF(na)	0	0	27	0	0	27	0	0	27
DRD	POWER DISSIPATION(µW)	208.507	205	217.451	162	220	72.266	116	231	248.937
	ION(ma)	0.190	0.107	0.069	0.190	0.107	0.069	0.107	0.107	0.069
	IOFF(na)	0	0	11	0	0	11	0	0	11
D^4L	POWER DISSIPATION(µW)	94.835	72.555	59.951	4.072	10.163	11.788	5.767	16.802	22.507
	ION(ma)	0.445	0.250	0.163	0.445	0.250	0.163	0.445	0.250	0.163
	IOFF(na)	0	0	27	0	0	27	0	0	27
FDRDCWSTPS	POWER DISSIPATION(µW)	7.555	7.676	8.355	7.408	7.583	8.358	9.024	11.642	13.708
	ION(ma)	0.445	0.250	0.163	0.445	0.250	0.163	0.445	0.250	0.163
	IOFF(na)	0	0	27	0	0	27	0	0	27

VI. CONCLUSIONS

This work consists of two parts. In section II, the existing circuits Dynamic DCVSL (Differential Cascode Voltage Switch Logic) footed circuit (DDCVSLF), dynamic DCVSL footless circuit (DDCVSLFL), delayed-reset domino circuit (DRD), dual-rail data-driven dynamic logic (D^4L)are compared with the proposed novel dual-rail domino footless circuit with self-timed precharge scheme (FDRDCWSTPS). From the results, the proposed circuit FDRDCWSTPS offers an improved performance in power dissipation, speed when compared with standard circuits. Hence, it is concluded that the proposed designs will provide a platform for designing high performance and low power digital circuits such as, processors and multipliers.

In section III, the effect of PVT variations on the performance (I_{on}, I_{off}, Power consumption) of the proposed energy-efficient domino logic circuit techniques are studied and analyzed. The process variations considered are VTHO (Threshold voltage at zero bias), TOXE (Oxide layer thickness) and UO (carrier mobility). The voltage variations considered are 0.7v, 0.8v. The temperature variations considered are +127℃ and-73℃. The technology considered is 65 nm. From the results, it can be observed that when

process variations increase then power dissipation decreases and vice versa. When the temperature variations decrease power dissipation decreases and vice versa. When voltage variations increase, power dissipation decreases.

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