# EBL Based Biquad Infinite Impulse Response Filter Using High Efficiency Charge Recovery Logic

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***ABSTRACT****- Charge recovering circuit has the potential to reduce dynamic power consumption in digital systems with significant switching activity. The overall energy-efficiency of charge recovery circuit depends on the rate at which transitions occur. A charge recovery logic family named Enhanced Boost Logic has been presented. EBL is an enhanced version of Boost Logic that achieves shorter pipeline latencies while retaining its energy advantages over static CMOS. EBL is capable of operation at high clock frequencies by developing a near-threshold voltage before the onset of the power clock. The EBL based Biquad IIR filter is designed. The design yields lower latency while maintaining good energy efficiency.*

*Index terms; Digital Signal Processing (DSP), low power VLSI, Infinite Impulse Response(IIR),finite impulse response(FIR).*



## "1. INTRODUCTION".

Demands for low power electronics have motivated designers to explore new approaches to VLSI circuits. The classical approaches of reducing energy dissipation in conventional CMOS circuits included reducing the supply voltages, node capacitance, and Switching frequencies Energy-recovery circuitry, on the other hand, is a new promising approach to the design of VLSI circuits with very low energy dissipation.

Charge-recovery circuitry has potential reduce dynamic power consumption in digital systems with Significant switching activity. To keep energy consumption to a minimum, charge-recovery circuitry is typically designed so that it maintains low voltage drops across device channels, while recovering the charge supplied to it every clock cycle [1].

It introduces the Enhanced Boost Logic (EBL), an improved version of the basic Boost Logic that achieves shorter pipeline latencies while retaining its energy advantages over static CMOS. Similar to Boost Logic, EBL is capable of operation at high clock frequencies by developing a near-threshold voltage before the onset of the power clock. Evaluation devices in EBL have twice the gate overdrive compared to first-generation Boost Logic [2], [3].

The biquad has a necessary coefficient scaling factor when one or more of the coefficients are greater than 1.0. This filter has a 16-bit input, 16 bit output, and 16 bit coefficients. This code lets the ADSP-2100 Family DSP perform a Nth-order IIR filter by performing N/2 biquads. The execution time is [8*(N/2) + 10] instruction cycles. The DSP can perform a tenth-order IIR filter on a signal sampled at more than 300 k Sa/s.

The latency of this EBL-based IIR is only 1.5 cycles longer than that of a similar-performance static CMOS design that has been implemented separately. Fabricated in a 0.13-µ m CMOS process, the test-chip includes a fully-integrated 3 nH inductor.

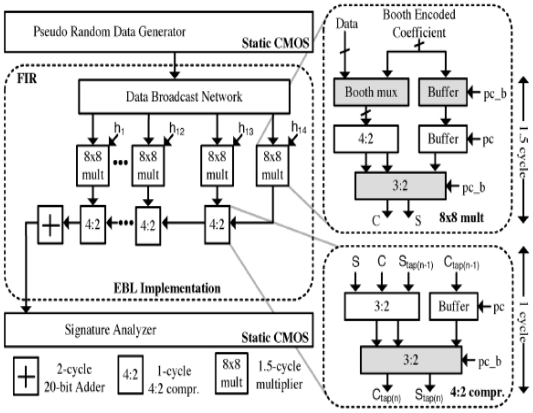
The Chapter II describes about enhanced boost logic with FIR filter. The Chapter III describes the test chip overview. The chapter IV is describes the EBL design methodology. The chapter V describes simulation result and discussion. The Chapter VI describes the conclusion. The chapter VII describes the references.

## "2. ENHANCED BOOST LOGIC".

Powered by the aggressively-scaled voltage, the Logic stage drives the dual-rail outputs conventionally with sub threshold-level energy consumption the first half of each clock cycle. Subsequently, during the second half of each cycle, the Boost stage amplifies the near-threshold voltage between the two outputs to full rail using the two complementary clock phases pc and pc_ b. These clock phases are generated using an H-bridge topology. The energy-efficient and multi-MHz operation of SBL with a single sub threshold supply has been demonstrated in silicon [4], [5].

Another departure from Boost Logic is that the same sub threshold supply is used to power a "blip" clock generator, producing two partially-overlapping clock waveforms and with peak values significantly greater than VCC. The bulk of all NMOS transistors are connected to ground, and the bulk of PMOS transistors in the cross-coupled inverters are connected to the corresponding power-clock phases.

Since the Evaluation stage inputs follow clock phase pc to full VDD, the performance of the NMOS precharge device is relatively immune to the Vth drop thanks to the increased gate overdrive.




**"Fig 1. FIR block diagram and clock generator".**

Per-cycle energy consumption of an EBL gate is given by the equation

$$E_{EBL}=E_{Evaluation}+E_{Boost}+E_{crowbar}$$

## "3.FIR TEST-CHIP OVERVIEW".

EBL gate has a built-in transparent latch, the state intensive nature of a transpose-type FIR filter coupled with the relatively simple combinational logic between its state elements. The FIR filter is pipelined to take advantage of EBL's potential for low latency overhead. Input data are broadcast to each tap within 1 cycle. Each 8x 8 multiplier takes 1.5 cycles to merge the partial products from the Booth mux to the sum and carry.

4:2 compressor array is formed by a series of 4:2 compressors cascaded together it together, is used to

perform column-wise compression of the partial produce. By taking the NOT of Carry.

| Cell name | Power dissip a-tion | Average delay | Worst case delay | Average PDP | Worst case PDP | Operation frequency |
|---|---|---|---|---|---|---|
| FA_ con | 100% | 100% | 100% | 100% | 100% | 100% |
| FA_ new | 67% | 104% | 124% | 70% | 84% | 87% |
| FA_s D | 74% | 79% | 95% | 58% | 71% | 113% |

"**Table 1: Comparison of Different Full Adders".**

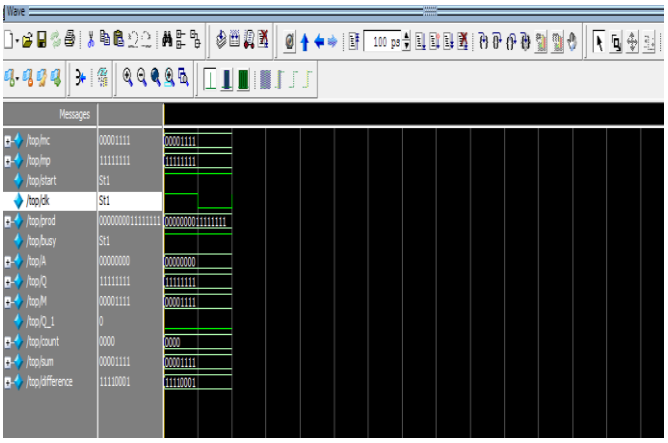
The Sum function has an evaluation stack height of six, and the Carry function has an evaluation stack height of five. The 121.6 m layout implementation of the 4-to-2 compressor in EBL, which has only 7.6% area overhead when compared to a static CMOS implementation.

## "4. EBL DESIGN METHODOLOGY".

Charge-Recovery logic has been designed using transistor- level simulation to verify functionality and electrical properties. The number of simulation cycles it takes to excite all possible input combinations and all possible timing arcs is at least exponential with the number of inputs. Even with the use of fast Spice programs such as Synopsys HSIM or Cadence.

## "5. SIMULATION RESULTS AND DISCUSSION".

This output is combined code for EBL, biquad, 20bit adder, boost logic and the compressor. The compressor is used for full adder. The 20 bit adder is widely used for carry save adder and ripple carry adder.



The result is finally got the power consumption is reduced 50% and delay also reduced in this paper.

## "6.CONCLUSION".

The performance and energy advantages of EBL, we have designed a biquad IIR filter in a 0.13µ m CMOS process. The proposed results were designed to support frequency-scaled operation and the clock generator.

"**Table.2 comparisons of different filters".**

| Design type | Biquad | 14 tap 8 bit | 8tap 6 bit | 14 tap 8 bit |
|---|---|---|---|---|
| Technology | 0.13µ m | 0.13µ m | 0.18µ m | 0.13µm |
| Normal supply | 1.0 | 1.2 | 1.8 | 1.2 |
| Operating frequency | 450 | 466 | 225 | 1010 |
| Sample rate(M/samples) | 450 | 466 | 550 | 1010 |
| Power dissipation(mW) | 40.0 | 39.1 | 36 | 122.5 |
| Area(mm2) | 0.3 | 0.34 | 0.3 | 0.85 |
| Power/MHz/Tap/In bits/Coeff bits | 90.6n W | 93.6n W | 230nW | 133nW |

Latency is typically an order of magnitude higher than static CMOS design. At its resonant frequency of 450 MHz, the test-chip dissipates 40.1 mW with a 90.6 nW /MHz/Tap/InBit/CoeffBit.

# “7.REFERENCES”.

[1] .W. Athas, L. Svensson, J. Koller, N. Tzartzanis, and E. Ying-Chin Chou, “Low-power digital systems based on adiabatic-switching principles,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 2, no. 4, pp. 398–407, Dec. 1994.

[2] S. Kim, C. Ziesler, and M. Papaefthymiou, “A true single-phase 8-bit adiabatic multiplier,” in *Proc. Des. Autom. Conf.*, 2001, pp. 758–763.

[3] V. Sathe, J.-Y. Chueh, and M. Papaefthymiou, 1.1 GHz charge recovery logic,” in *Dig. Techn. Papers IEEE Int. Solid- State Circuits Conf. (ISSCC)*, 2006, pp. 1540–1549.

[4] W.-H. Ma, J. C. Kao, V. S. Sathe, and M. Papaefthymiou, “A 187 MHz sub threshold-supply robust FIR filter with charge-recovery logic,” in *Proc. Symp. VLSI Circuits*, 2009, pp. 202–203.

[5] W.-H. Ma, J. Kao, V. Sathe, and M. Papaefthymiou, “187 MHz sub threshold- supply charge-recovery FIR,” *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 793–803, Apr. 2010.