Embedded Transition Inversion Coding with Low Switching Activity for Serial Links

N. Suresh
M.Tech, Assistant Professor
Department of ECE
ASIST, Paritala, A.P

Shaik Saidulu
B.Tech, Student
Department of ECE
ASIST, Paritala, A.P

N. Vishnu priya
B.Tech, Student
Department of ECE
ASIST, Paritala, A.P

M. Siva Reddy
B.Tech, Student
Department of ECE
ASIST, Paritala, A.P

M. Venkata Sudha
B.Tech, Student
Department of ECE
ASIST, Paritala, A.P

K.Vamsi Krishna
B.Tech, Student
Department of ECE
ASIST, Paritala, A.P

***Abstract*— Serial link interconnection has been proposed for its advantages of reducing crosstalk and area. However, serializing parallel buses tends to increase bit transition and power dissipation. Several coding schemes, such as serial followed by encoding (SE) and transition inversion coding (TIC), have been proposed to reduce bit transition. TIC is capable of decreasing transitions by 15% compared to the SE scheme, but an extra indication bit is added in every data word to represent inversion occurrence. The extra bit increases the transmission overhead and the bit transitions. This paper proposes an embedded transition inversion (ETI) coding scheme that uses the phase difference between the clock and data in the transmitted serial data to tackle the problem of the extra indication bit. The ETI coding scheme reduces the transition by up to 31% compared to SE scheme. The analysis and simulation results indicate that the proposed coding scheme produces a low bit transition for different kinds of data patterns. Using the optimum degree of multiplexing, width, and spacing, the ETI coding scheme achieves 30%–60% energy reduction compared with the parallel bus without overhead. Taking circuit overhead into consideration, the power saving is up to 31.71% and 26.46% at a clock cycle of 250 ps for the 90- and 130-nm CMOS technology for m = 2 where m is the number of parallel wires multiplexed into a serial link.**

Keywords*— Coding techniques, low switching activity, phase detector, serial link.

I. INTRODUCTION

Low power design, in a system perspective, happens at all levels of the digital electronic system stack. It is being done from the lowermost device level design to the topmost software design. And there are the intermediate levels where a lot of effort is being expended to make systems run at low power, keeping the compromise in performance to be minimum. The increasing density of the integrated circuits as postulated by Moore's law makes it even more important to have low power systems since the power supply for such a density integrated circuit may not keep track in size with the miniaturization of the electronic components. Hence research is being made at all levels of a system stack. A system can consist of multiple components.

Advanced silicon technology offers the possibility of integrating hundreds of millions of transistors into a single chip, which makes system-on-chip (SOC) design possible with the continuous scaling of silicon technology, area and power dissipation of interconnects are one of the main bottlenecks for both on-chip and off-chip buses. Multiplexing parallel buses into a serial link enables an improvement in terms of reducing interconnect area, coupling capacitance, and crosstalk [1], but it may increase the overall switching activity factor (AF) and energy dissipation. Therefore, an efficient coding method that reduces the switching AF is an important issue in serial interconnect design.

Serial link interconnection has been proposed for its advantages of reducing crosstalk and area. However, serializing parallel buses tends to increase bit transition and power dissipation. Embedded transition inversion (ETI) coding scheme is used here that uses the phase difference between the clock and data in the transmitted serial data which reduces the problem of the extra indication bit.

The ETI coding scheme reduces the transition by up to 31% compared to SE scheme. The analysis and simulation results indicate that the proposed coding scheme produces a low bit transition for different kinds of data patterns. Using the optimum degree of multiplexing, width, and spacing, the ETI coding scheme achieves 30%–60% energy reduction compared with the parallel bus without overhead.

II. LITERATURE SURVEY

Serial link interconnection has been proposed for its advantages of reducing crosstalk and area. However, serializing parallel buses tends to increase bit transition and power dissipation. Several coding schemes, such as serial followed by encoding (SE) and transition inversion coding (TIC), have been proposed to reduce bit transition. TIC is capable of decreasing transitions by 15% compared to the SE scheme, but an extra indication bit is added in every data

word to represent inversion occurrence. The extra bit increases the transmission overhead and the bit transitions. Embedded transition inversion (ETI) coding scheme that uses the phase difference between the clock and data in the transmitted serial data to tackle the problem of the extra indication bit. The ETI coding scheme reduces the transition by up to 31% compared to SE scheme. The analysis and simulation results indicate that the proposed coding scheme produces a low bit transition for different kinds of data patterns. Using the optimum degree of multiplexing, width, and spacing, the ETI coding scheme achieves 30%–60% energy reduction compared with the parallel bus without overhead. Taking circuit overhead into consideration ,the power saving is up to 31.71% and 26.46% at a clock cycle of 250 ps for the 90- and 130-nm CMOS technology for $m = 2$ where m is the number of parallel wires multiplexed into a serial link.

III. IMPLEMENTATION

This project focuses on power optimization in a serial communication link. This optimization of power can be achieved by using a technique called embedded transition inversion (ETI) coding which reduces the number of transitions such that the power consumption can be optimized. If the number of transitions increases the switching activity increases and hence power increases. ETI scheme uses the phase difference between the clock and the transmitted serial data which reduces the problem of extra indication bit. ETI uses the bus invert mechanism in order to count the no of transitions.

a. Bus Invert

Bus invert works by counting the number of transitions, which involves XOR of the present and previous data. If the number of transitions is more than half the bus width, the inverted data is transmitted, else the original data is transmitted. A separate line is also added to the bus which will carry the decision. This is an overhead to the design of the system which requires extra circuitry as well as traces. The decision bit will signify whether the data that is on the bus is the original data or its complement. The bus invert logic has to be added to an existing bus interface just where the external interface is happening. It can be just before the level converter, which converts the chip internal voltage levels to external voltage levels. The logic will take its input from what the bus core systems is feeding it and processes it to feed to the level converter. The bus invert algorithm is explained below.

b. Algorithm 1: Bus Invert

1. Count the transitions between the data on the bus and the next data that is to be put on bus
2. **if** transitions count < half of the bus width
3. Assign next data to bus
4. **else**
5. Invert the next data and assign the complement to bus

A block diagram of the Bus Invert system is shown in Figure 2.2. A sample coding process for a sample data is shown in Table 2.1.

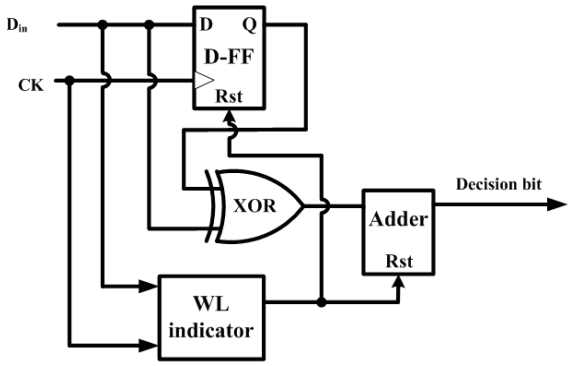


Figure 2.1 Bus Invert Decision Circuit

Table 2.1 Bus Invert Decision Circuit

Bit No.	1	2	3	4	5	6	7	8
Current Data on bus	1	0	1	0	1	0	1	1
Next Data to be put on Bus	0	1	1	1	0	1	0	1
XOR of present and next data (Transition Vector)	1	1	0	1	1	1	1	0

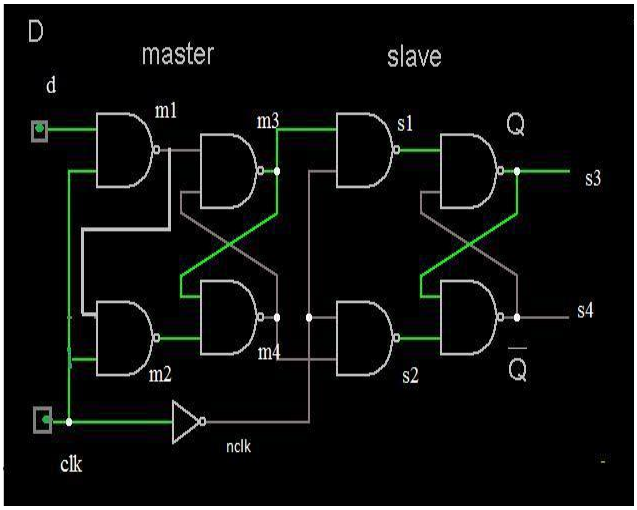
In the given example the number of transitions is 6 which is more than half the bus width, 4. So the data is inverted and then sent. The decision is sent on a separate line. An XOR between the current data and the next data that is put on the bus shows that the transitions are reduced to 2 which is also given by (N-t) where N is the bus width and t is the original number of transitions

The whole operation involves a chain of full adders to count the transitions and then perform another XOR on the data that has to be sent. All these operations have to be done before the next data is to be put on the bus. The chain of full adders operating the output of the array of XOR gates contribute to the delay in taking a decision. This delay is the parameter which limits the maximum bandwidth of the system. Beyond this the encoder delay also has to be taken into account which involves a parallel XOR to perform controlled inversion. This entire set of operations has to be over by the time the next data arrives leading to a restriction on bandwidth.

The no of transitions are calculated and the decision bit is generated and depending on the decision bit transition inversion coding will be done and the no of transitions will be reduced after encoding and hence the power will be optimized.

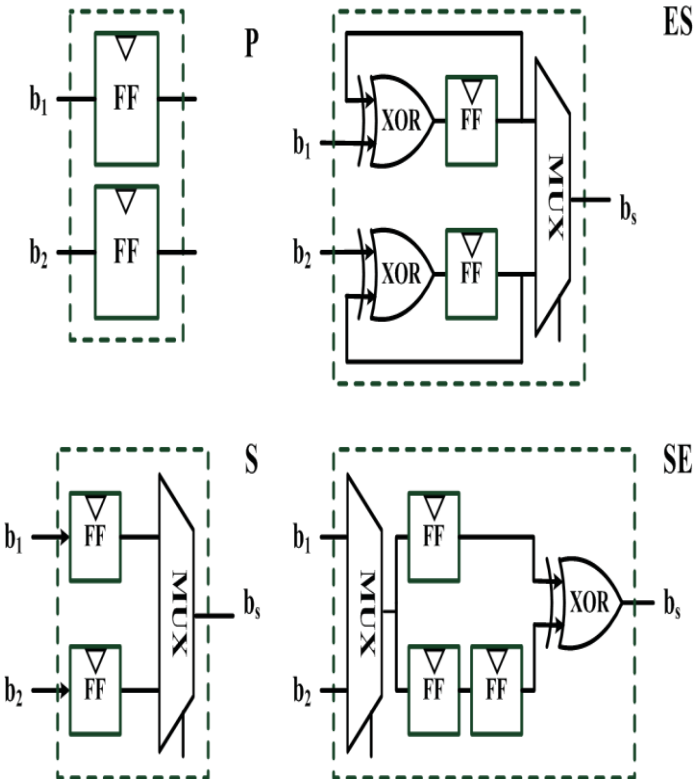
Here in this project along with power time is also optimized by taking the DFF architecture into consideration. Instead of designing another inverter to invert the data the DFF architecture is considered which is capable inverting the data such that the time can be optimized.

The equations are an exception to the prescribed specifications of this template. You will need to determine



c.BUS SCHEMES

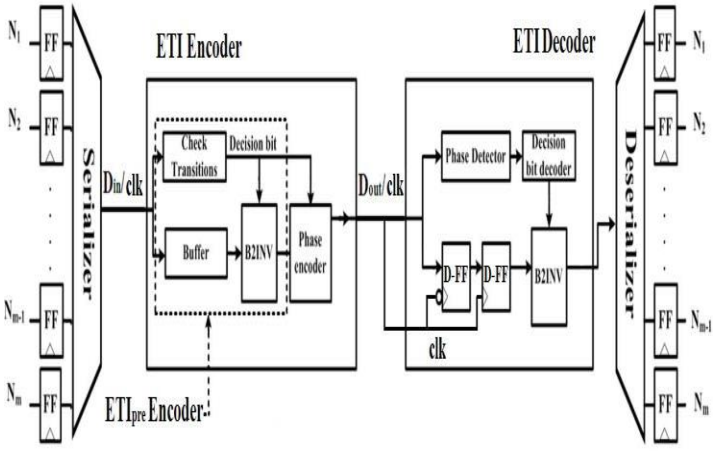
There are four types of bus schemes, including parallel (P), serial (S), encoding followed by serial (ES), and serial followed by encoding (SE) as shown in Fig. Their average AFs are AFP, AFS, AFES, and AFSE, respectively. The bit stream in this paper refers to the transmitted data in each wire of the input parallel bus. The AF analysis results of serializing two bit streams into a single output



IV. EXISTING TECHNIQUE TO DESIGN BUS

(TIC) technique to reduce switching activity for random data and to detect errors. Their technique counts the transitions in the data word, and inverts the transition states if the number of transitions in a data word is more than half of the word length. The scheme sets the current bit in the serial stream to be the same as the previous encoded bit when there is a transition .Otherwise, it is set to the inversion of the previous encoded bit. A transition indication bit is added in every data word. This extra bit not only increases the number of transmitted bits, but also increases the transitions and latency. A serial link on-chip bus architecture is proposed to lower interconnect power. Serialization reduces the number of wires and leads to a larger interconnect width and spacing. A large interconnect spacing reduces the coupling capacitance, while the wider interconnects reduce the resistivity. A significant improvement in the interconnect energy dissipation is achieved by applying different coding schemes and their proposed multiplexing techniques. However, the power reduction decreases when the degree of multiplexing increases. The embedded transition inversion (ETI) coding scheme to solve the issue of the extra indication bit. This scheme eliminates the need of sending an extra bit by embedding the inversion information in the phase difference between the clock and the encoded data. When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains unchanged and there is no phase difference between the clock and the data. This ETI coding scheme reduces transition by 31% compared with the SE scheme. The improvement of transition reduction is 19% compared with that of the TIC.

V. ETI ARCHITECTURE:



VI. EMBEDDED TRANSITION INVERSION CODING:

Word exceeds the threshold Nth, the bits in the data word should be encoded. Otherwise, the data word remains the same. When an encoding is needed in a data word, this method checks every two-bit in the data word, as Fig. shows. Every two bit in the serial stream is combined as a base to be encoded. In this case, the b11b21 is a base and the b31b41 is

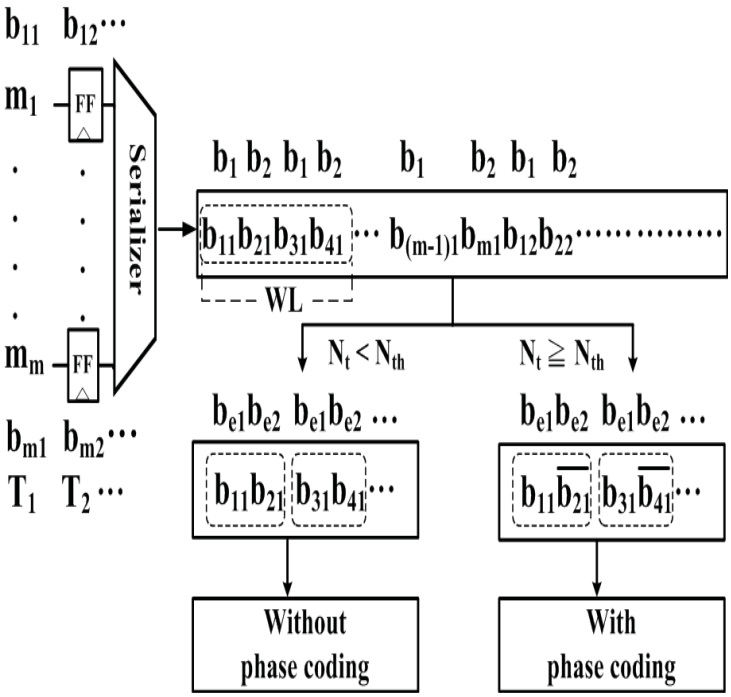
another base. The 2-bit in a base is denoted as b1b2 and the encoded output is denoted as be1be2. When the Nt in a data word is less than Nth, b1b2 remains unchanged. Otherwise, we perform the inversion coding and the phase coding. For the inversion coding, the bit streams "01" and "10" are mapped to "00" and "11," respectively. The bit streams "00" and "11" are mapped to "01" and "10," respectively. For the phase coding, we embed the inversion information in the phase difference between the clock and the encoded data.

Parallel Streams		Serial Stream	Serial Stream	Serial Stream
Stream1	Stream2	(TIC)	(ETI_{pre})	(ETI)
$b_{11}b_{12}$	$b_{21}b_{22}$	$b_{11}b_{21}b_{12}b_{22}\mathbf{b}_{ex}$	$b_{11}b_{21}b_{12}b_{22}$	$b_{11}b_{21}b_{12}b_{22}$
00	00	0000 **0**	0000	0000
00	01	0001 **0**	0001	0001
00	10	0001 **1**	0001	0001
00	11	0000 **1**	0000	**1**000
01	00	0111 **1**	0111	0111
01	01	0011 **0**	0011	0011
01	10	0011 **1**	0011	0011
01	11	0111 **0**	0111	0111
10	00	1000 **0**	1000	1000
10	01	1100 **1**	1100	1100
10	10	1100 **0**	1100	1100
10	11	1000 **1**	1000	1000
11	00	1111 **1**	1111	**0**111
11	01	1110 **1**	1110	1110
11	10	1110 **0**	1110	1110
11	11	1111 **0**	1111	1111

$$b_{e1} = b_1$$

$$b_{e2} = \begin{cases} b_2, & \text{with} \quad N_t < N_{\text{th}} \\ !b_2, & \text{with} \quad N_t \geq N_{\text{th}}. \end{cases}$$

Since this operation is on a two-bit basis and only the second bit is inverted, it is called bit-two inversion (B2INV).



ETI coding scheme for one serial link, word length = WL*N*th = *WL/2*, and number of transition = *Nt* .

BIBLOGRAPHY

[1] Abinesh, Bharghava R., Suresh Purini, Govindarajulu Regeti, "Transition Inversion based Low Power data coding scheme for Buffered Data Transfer", Accepted for publication in special issue of Journal of Low Power Electronics, October 2010.

[2] Abinesh R., Bharghava R., Suresh Purini, Govindarajulu Regeti, "Transition Inversion based Low Power data coding scheme for Buffered Data Transfer", 23rd International Conference on VLSI Design, January 2010

[3] Joint Winner of Intel Research Challenge (also known as Intel Scholar Program) 2008-2009 http://www.intel.com/cd/corporate/education/APAC/ENG/in/news/news43/419015.htm

[4] Abinesh R., Bharghava R., M.B. Srinivas, "Transition Inversion Based Low Power Data Coding Scheme for Synchronous Serial Communication", is vlsi, pp.103-108, 2009 IEEE Computer Society Annual Symposium on VLSI, 2009

[5] The New York Times Technology section April 1, 2008. Light and Cheap, Netbooks Are Poised to Reshape PC Industry.

[6] http://lesswatts.org/ Intel sponsored community project for software based low power development.

[7] http://www.intel.com/consumer/products/style/netbook.htm Netbook vs. Laptop and Entry Level Desktops.