International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 3, March - 2014

Energy Efficiency - FIR Implementation Via Voltage Overscaling -Based Residue Number System

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Abstract— **In Low power design based circuits, power consumption gets reduced with the decrease in supply voltage. There are several techniques to reduce Vdd including multiple supply voltages, variable voltage scaling & retiming. The drawback involved is timing violation in the critical path. The proposed technique to scale down the supply voltage below the critical supply voltage (CSV) is referred as Voltage Over Scaling (VOS). The residue number system (RNS), which performs the parallel carry-free arithmetic algorithm, has a shorter critical path and lower hardware complexity than the two's complement system under the same computation precise and can achieve higher energy efficiency.The improvement over those techniques lead to design of Joint Residue Number System & Residue Precision redundancy (JRR).The voltage over scaling (VOS) technique in Residue-Number-System (RNS)-based digital signal processing system for achieving high energy efficiency. JRR can save 54% more energy compared to the traditional FIR filter.**

Keywords— Energy efficiency, joint RNS-RPR (JRR),reduced precision redundancy (RPR), residue number system (RNS).

I. INTRODUCTION

Residue Number Systems have gained significant importance in the field of high speed digital signal processing due to their carry-free nature and speed-up provided by parallelism. The critical aspect in the application of RNS is the selection of the moduli set and the design of the conversion units. There have been several RNS (Residue Number Systems) moduli sets proposed for the implementation of digital filters. However, some are unbalanced and some do not provide the required dynamic range. This addresses the drawbacks of existing RNS moduli sets and proposes a new moduli set for efficient implementation of FIR filters. An efficient VLSI implementation model has been derived for the design of a reverse converter from RNS to the conventional two's complement representation. This model facilitates the realization of a reverse converter for better performance with less hardware complexity when compared with the reverse converter designs of the existing balanced 4-moduli sets. Comparing multiply and accumulate units using RNS that are implemented using the proposed four-moduli set with the state-of-the-art balanced four-modulus sets, show large improvements in area and power reduction for various dynamic ranges.

To mitigate the soft errors caused by VOS (voltage over scaling), method is proposed called Joint RNS (Residue Number System)-RPR (Reduced Precision Redundancy) JRR, which is the combination of RNS and the Reduced Precision Redundancy (RPR) technique. The JRR technology inherits the properties of RNS, including shorter critical path, low complexity, and low power. Moreover, JRR can achieve higher power reduction than RNS for VOS applications. Since the soft errors caused by VOS lead to significant performance degradation of RNS, the information from RNS and RPR to achieve a high recovering probability of the soft errors with low hardware complexity. JRR has lower complexity and better performance than the traditional soft error mitigation method. The improvement over those techniques leads to design of Joint Residue Number System & Residue Precision Redundancy (JRR).To achieve a high recovering probability of the soft errors with low hardware complexity using Joint Residue Number System(JRR) Design a FIR filter based on JRR technique.

In Low power design based circuits, power consumption gets reduced with the decrease in supply voltage. There are several techniques to reduce multiple supply voltages, variable voltage scaling & retiming. The drawback involved is timing violation in the critical path. The proposed technique to scale down the supply voltage below the critical supply voltage (CSV) is referred as Voltage Over Scaling (VOS). The residue number system (RNS), which performs the parallel carry-free arithmetic algorithm, has a shorter critical path and lower hardware complexity than the two's complement system under the same computation precise and can achieve higher energy efficiency.

II. PROPOSED SYSTEM

Residue Number System is Integer System performs addition, subtraction and Multiplication. RNS is a multiple data path independently perform arithmetic operation. The RNS which performs the parallel Carry-free arithmetic algorithm, has a shorter critical path and lower hardware complexity than the two's complement system (TCS) under the same computation precise. Hence the RNS based FIR

system can achieve higher energy efficiency. The multi voltage technique is used in RNS to achieve higher power reduction in RNS parallel independent channels. Convert Arithmetic on Large Numbers to Arithmetic on Small Numbers. Each channel is characterized by a small dynamic range. Big advantages if the dynamic range is high (32, 64,128 bit) when a lot of small moduli can be used in RNS.A specific RNS is defined with respect to a relatively prime moduli set {m1,m2,m3,. ,mn},where mi is a positive integer and satisfies greatest common divisor (mi ,m j) = 1, i ≠ j, i, j = 1, 2, . . . , n(n > 1). An integer X can be represented in RNS as a set {x1, x2, . . . , xn}, in which xi is the residue of X mod mi

xi = X mod mi = (X)mi i = 1, 2, . n (1)

RNS has multiple data paths, which independently perform the arithmetic operation in parallel. The mod *mi* processors in RNS are operated in the VOS regime to achieve high energy efficiency.R2B and B2R converters are supplied with the CSV to guarantee the conversion is error free.

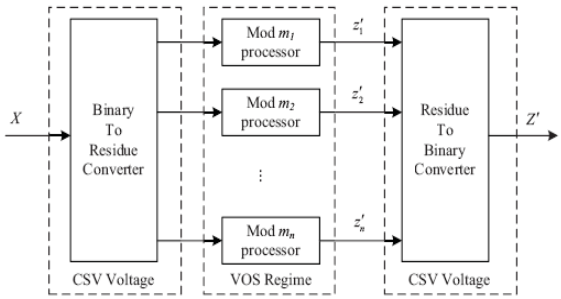

Figure 1.Block diagram for proposed Rns Scheme In Vos

BINARY TO RNS (RESIDUE NUMBE SYSTEM)

Two-level four moduli set (2n, 2n+1–1, 2n –1, 2n +1) is introduced and an efficient residue to binary converter is proposed for it. This moduli set contains (2n, 2n –1, 2n +1) in its first-level and the moduli set {2n,2n+1 –1} in its second-level for the modulo 2n.The RNS is defined in terms of a set of relatively prime moduli. For unsigned integer in the range of (0, m) can be represent in RNS.

IMPLEMENTATION OF FIR FILTERS in RNS

The most popular use of RNS in the design of digital Finite Impulse Response (FIR) filters. FIR filters are highly stable architectures and are less sensitive to quantization errors than filters of recursive architectures like Infinite Impulse Response (IIR) filters. A digital FIR filter response of N-taps is mathematically represented, two's complement system (TCS) representation is widely chosen for the binary representation of the input and co-efficient of a digital filter. FIR filters can be implemented in hardware either in the direct form. For high speed implementations of Direct form FIR filters, the result of the multiplier is represented in carry-save format and the accumulator is implemented as carry save adder. The final stage of the implementation of transpose form FIR filter is a conventional adder to add the carry save vectors of the last stage. The direct form FIR filter need pipeline register between the adders to reduce the delay of the adder tree and to achieve high throughput

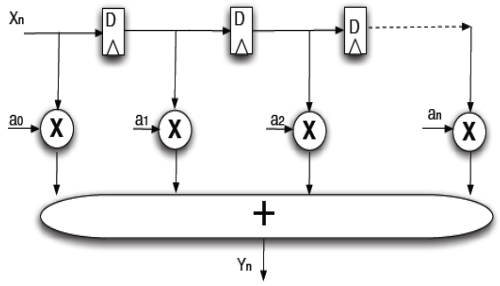

Figure 2.Transposed Form Of Fir Filter

RNS FILTER ARCHITECTURES

Reduction in the peak current Compared to conventional implementation of FIR Filters, RNS architectures uses smaller arithmetic units and less complex designs. Hence, the peak current in each arithmetic unit decreases. Reduction in the switching activity.The reason mentioned above is applied for Smaller switching activities in RNS arithmetic units. As RNS systems operate on smaller input widths, the switching activities are also relatively smaller. The reduction in peak current as well as switching activity results in smaller dynamic Power. Several other circuit level power reduction techniques like voltage scaling in noncritical paths using high threshold transistors can be applied very easily in RNS circuits. In conventional binary systems, there are only specific Paths where high threshold transistors can be used. RNS FIR filters are the conversion units from binary to RNS and the reverse converter to convert the individual filter responses to binary response.

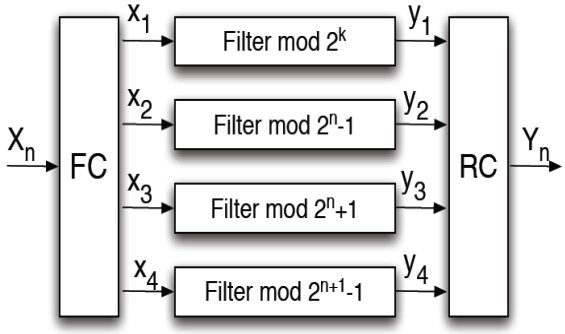

Figure 3.Rns Filter Architectures

There are three basic steps in the implementation of RNS FIR filter using the moduli.

1. Forward Convertor
2. Reverse Convertor
3. RNS Fir Filter Implementation

FORWARD CONVERTOR

The forward converter encodes a binary number into a residue represented number, with regard to the moduli set. Each arithmetic channel requires modular multiplication and accumulation for each modulo of set.

REVERSE CONVERTOR

Implementation of RNS FIR filters is the conversion units from binary to RNS and the reverse converter to convert

the individual filter responses to binary response. The arithmetic channels are working in a completely parallel architecture without any dependency, and this result in considerable speed enhancement. Several small residues, on which modular arithmetic operations are performed. Due to the carry free properties of these residues, the arithmetic operations can be performed in parallel and hence RNS presents a promising alternative to the binary number representation in high speed digital signal processing (DSP) applications. RNS helps in reducing hardware complexity and the associated power consumption.

RNS FIR FILTER IMPLEMENTATION

MODULI 2N

If X is the input of n bits wide, then X mod 2n is simply calculated by discarding the most significant bits to the k th bit position. For example if X is represented as

X mod 2n = X0 …….. Xn-1 (2)

MODULI 2(N-1) AND (MODULI 2(N-1)-1)

There are popular algorithms to calculate residues of the moduli of kind 2(n-1).First step in the process of moduli calculation is to represent input X in slices of n (n+1) bits. These operands generated are added using a Multi-Operand Moduli Adder (MOMA).Carry Save Adders (CSA) with end-around-carry to reduce multiple operands to two vectors (carry vector and save vector) of n bits wide. This high speed implementation of the moduli adder is used in the current design.

MODULI 2(N+1)

The input bits are arranged using the periodicity property of the moduli 2n+1 as operands of n bits. The operands generated and the correction factors are added using carry save adders modulo 2n +1.The moduli 2n +1 carry save addition is as explained.

RESIDUE TO BINARY

The advantages of using the residue number system (RNS) over the conventional binary number system are well documented. Early researchers considered using mutually prime integers as moduli in the chosen RNS and the solutions for realizing all arithmetic operations were based on ROMs in order to speed up execution. However, it was later realized that by using powers-of-two related moduli sets, the need for ROMs to build RNS-based processors can generally be eliminated, and the basic building blocks needed such as adders, multipliers, binary- to-RNS converters and RNS-to-binary converters can be easily realized using logic gates.

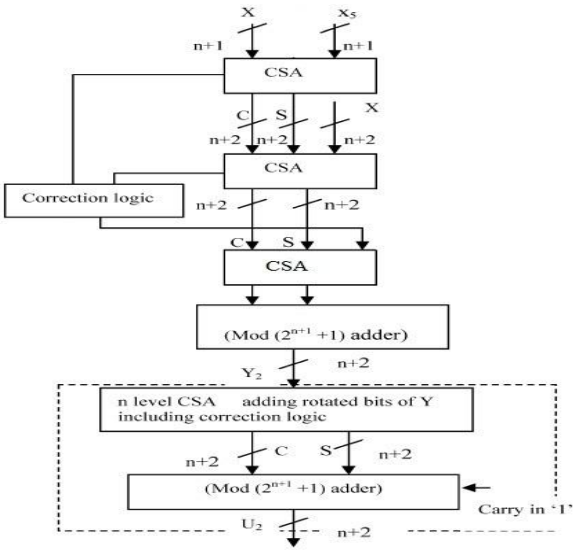

Figure 4.RNS to Binary

JRR METHOD IN RNS SCHEME.

JRR METHOD

The JRR-based RNS DSP system applies the joint information from RPR and RNS to correct the soft errors. We first give a brief introduction of the RPR method.

RPR Algorithm

The RPR requires an RPR whose output can be employed as the corrected output if the original system computes erroneously Since RPR has shorter critical path than the original system, the timing violation will not happen in the RPR module. The output signal of RPR can be represented as

$$Zrpr = F(X + \delta r) \quad (3)$$

where Zrpr is the output of the RPR module, δr is the rounding noise, and F is the system function. The correct output Z and Zrpr satisfy.

$$Z = Zrpr + f(\delta r, X) \in [-Nr, Nr] \quad (4)$$

where Nr is the bound of the rounding noise, which is inversely proportional to the bit width of RPR and f (δr , X) is the output of the rounding noise. The probability density function of the rounding noise for a 4-tap FIR filter.If Mi is large enough, Uδ will be much smaller than Rδ by division. Hence, the quotient Urpr is more precise than the remainder Rrpr . We can utilize this property to recover the information corrupted by the soft errors.

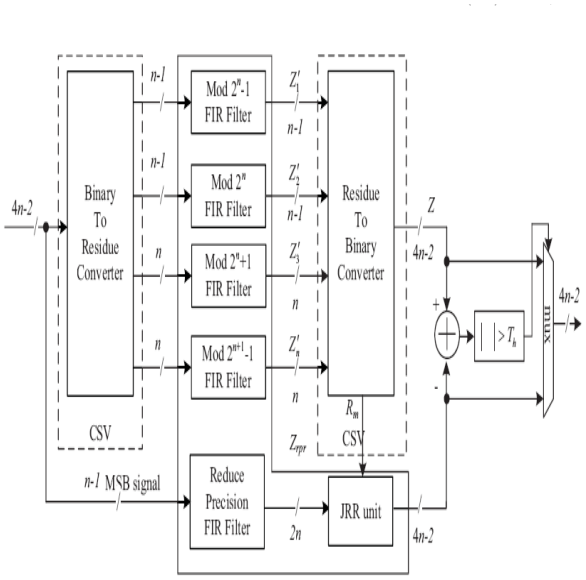

Figure 5.JRR Method In RNS Scheme

III. SIMULATION RESULTS

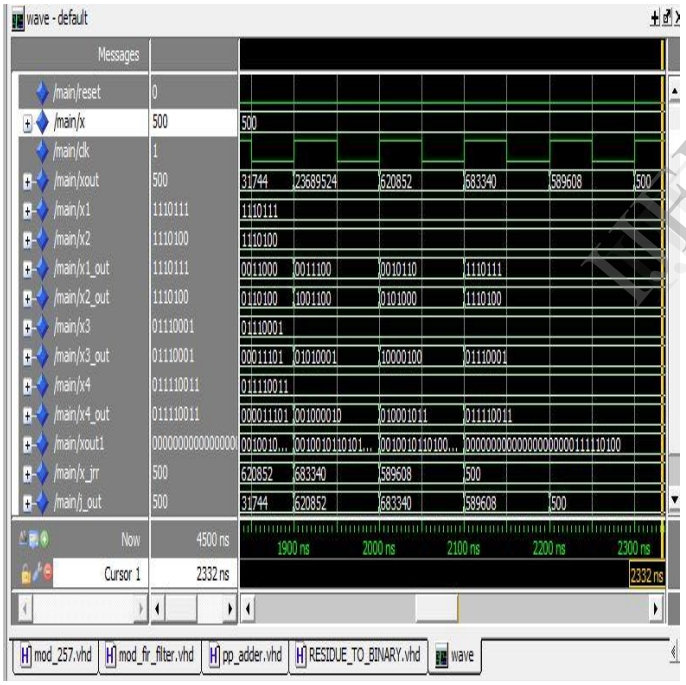

Figure 6.VLSI Output Waveform

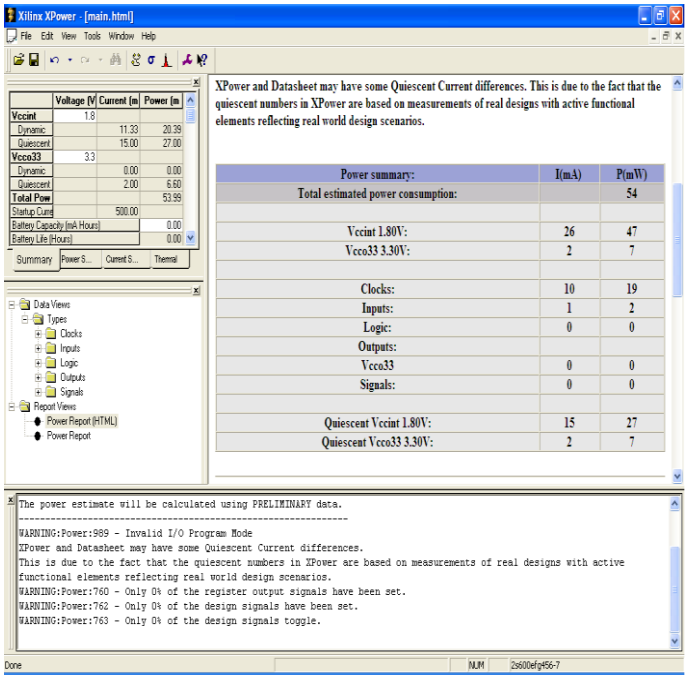

Figure 7.Power Analysis

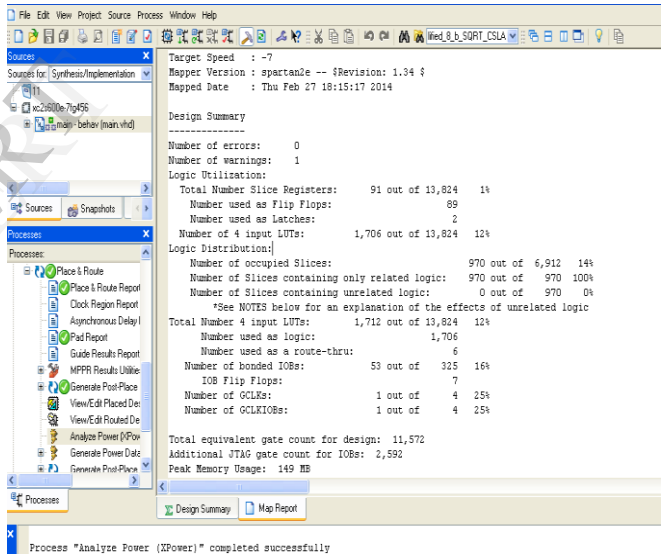

Figure 8.Area Analysis

IV. CONCLUSION

The VOS (Voltage over Scaling) technology method in RNS energy efficiency.R2B and B2R converters are supplied with the CSV to the conversion of error free. By implementing RNS in Fir filter to reduced noise and low power. An efficient RNS architecture for low power, high-throughput, and low area implementation of Fir filter is presented. Compared to the best of other existing designs our proposed design is better for area and power consumption. The energy-efficient method via RNS had a shorter critical path than the traditional system. by using the VOS technology, the EC(Error Control) method in RNS achieves higher energy efficiency.

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