Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 13 Issue 8, August 2024

Engineering TFETS for Terahertz Applications: Critical Design Insights

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***Abstract*—This research paper explores the impact of a novel approach to drain doping engineering on the behavior of Tunneling Field-Effect Transistors (TFETs) through TCAD simulations. The central concept involves the construction of a TFET structure that utilizes dual doping levels in the drain region: a high-doped region situated above a low-doped one. Investigating indicates a significant alteration in the tunneling phenomenon at the interface between the channel and drain due to this dual drain doping configuration. Specifically, the introduction of two distinct drain regions leads to an expansion in the tunneling width at the channel-drain junction. This expansion plays a key role in significantly reducing ambipolar current in the TFET, an essential aspect for improved device performance.**

***Keywords*— TFET, Ambipolar, BTBT, cutoff frequency, tunneling width.**

I. INTRODUCTION

Tunnel Field-Effect Transistors (TFETs) with high-frequency Tunnel have been established as transformative technology within the past few years; they form the basic architecture of today's electronics. These special transistors have an inherent feature to perform very well on high frequency operations which has become a necessity in today's technologically advanced world [1-5]. Above all, high-frequency TFETs have pushed the development of communication systems, changing the world from 4G to 5G, and increasing the complicated network directly related to our daily lifelessness. Some of these qualities include high switching speed, low power consumption which have significantly enhanced efficiency and speeds of wireless communications. Furthermore, these TFETs have organically fit into the areas of low power and high speed data processing especially in emerging areas such as artificial intelligence and edge computing [6-8]. Equally, their ability to operate efficiently at low supply voltage also places them at the heart of energy related products such as IoT sensors; they are instrumental at extending the battery life of devices. On this note, high frequency TFETs have the prospects of being significant tools for enhancing the advancement of the faster, efficient and environmentally friendly electronic systems as the technology expands.

In the conventional MOSFET, carrier transport that occurs on the channel depends on the thermionic emission across the energy barrier. On the other hand, Tunneling Field-Effect Transistors (TFETs) are based on a concept called band-to-band tunnelling, whereby the carriers switch from one band to another. The reason is that this specific type of BTBT mechanism deployed in TFETs eliminates the need for a conventional minimum subthreshold slope requirement. Surprisingly, many TFETs with subthreshold slope (SS) lower than 60 mV/decade were reported in many research articles [9-11]. Low ON current is one of the distinguishing features of the Tunneling Field-Effect Transistor (TFET) and it is possible to exceed the OFF current of conventional MOSFETs by several orders [12]. Several possible ideas have been proposed to make a higher ON current flow; Among them, several of them is the following have been found to work effectively. Such approaches involve the use of a double gate structure that employs a high-k gate dielectric or low k spacer [13-14]. Further, other methods require the use of a p-n-p-n configuration with different source pocket and the impact of strained silicon [15-18].

To counter the problem of ambipolar conduction in TFETs the following innovative approaches can be used though it makes things feel more relatable and connected to people [19]. Of these, one approach is the use of a mixed high-k and low-k gate dielectric material in which a high-k gate dielectric material is incorporated on the source side of the gate while a low-k dielectric material is incorporated on the drain side of the gate [20]. Nevertheless, it is crucial to focus on the fact that the recent studies indicate that this strategy is not very effective [21-22]. Another approach includes gate–drain underlap while

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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these methods do help in fighting ambipolar conduction, most of them have demerits like low ON current, poor high frequency response and complexity in the processing [23-25]. However, besides these non-stationary methods, consequences of these methods have been researched and analyzed, but the effects of these methods on high frequency behavior have not been looked in details in most of the earlier studies, hence making the high frequency performances ambiguous. Despite these studies, modest focus has been assigned to analyzing the high-frequency behavior of TFETs [26-27]. In other words, the following paper is mainly focused on evaluating the impact of the proposed technique on ambipolarity, as well as the high-frequency performance analysis at the same time. which significantly curtails ambipolar conduction but does have the downside of lower current gain [28]. Another solution that has been proposed involves using Gaussian doping in the drain region; nevertheless, friendly readers should note that physically implementing Gaussian doping can often be a challenge [29-30]. As far as the work function of gates is concerned, a pattern of using a dual metal gate has been towards. But it is noteworthy to define that this method results in an increase in the gate-to-drain capacitance and may be a problem in terms of high frequency [31]. Another technique, which is a gate-on-drain overlap technique, has been found to alleviate effects of ambipolar conduction [32]. However, it is also crucial to point out that the method of raising the length of the overlap region comes with the downside of raising the gate-to-drain capacitance; this decreases the device's high-frequency responsiveness [33-37].

In this paper, based on the help of the 2-D device simulations illustrating a method to suppress the ambipolar conduction by incorporating a highly doped layer above a low doped layer in the drain side of an n-channel TFET. The presented approach can be used to reduce ambipolar current while maintaining high frequency switching characteristics. Elaboratively, I calculated all the significant figures of merit for TFETs with high operating frequency such as gm, Csgs, Cdgs, and fT by changing the high-doped drain region thickness, spacer lengths, and various drain doping levels. The subsequent sections of this paper are structured as follows: Section II discusses simulation approach and calibration in general. In the subsequent Section III, the authors address the proposed device structure and the corresponding design specifications. The effects of major device design parameters are discussed in Section IV.

II. PROPOSED DEVICE ARXHITECTURE

TCAD simulations are very popular for the investigation of new device structure. Since the closed form expressions are difficult to obtain, numerical simulations have turned out to be a powerful technique for characterizing the behavior of the TFET and analyzing how its properties are affected by various design variables. In this study, all simulations were simulated using Silvaco Atlas version 5. 20. 2. R. For allowing the lateral tunneling to occur, the nonlocal Band-to-Band Tunneling (BBT. NONLOCAL) model was used. By incorporating mobility issues, the Lombardi mobility model (CVT) was initiated to address issues like the transverse field effects, the effect of doping and the effects of temperature. Specifically for high doping levels, which appear due to a combination of highly doped source and drain regions with a bandgap narrowing model, Fermi–Dirac statistics were also applied, and the Shockley–Read–Hall as well as the Auger recombination models were considered. Carrier transport was simulated by drift-diffusion and gate leakage current contribution was not considered. In addition, for establishing high-frequent performance parameters, small-signal AC analysis at a frequency of 1 MHz was also done within the design we prepared, which made it possible to obtain high-frequent figures of merit. Shown in Figure 1 is the cross-sectional view of the silicon n-channel type TFET used in this research. The major distinction between this proposed structure and the regular one is the position of the drain additional structure. Here, we have introduced two different drain regions: one is the n + drain having a high doping concentration while the other is the n – drain having a comparatively lower doping concentration, instead of having a continuously varying doping concentration as it is in the frequently used conventional drain.

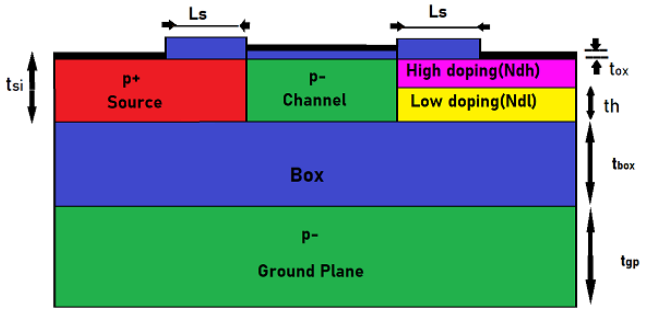

Fig. 1. Cross-sectional view of the proposed TFET

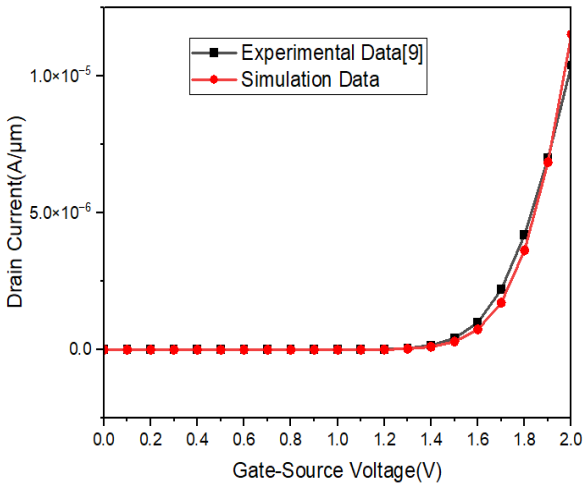

Fig. 2 Comparison of Calibrated Experimental Data and Simulated data.

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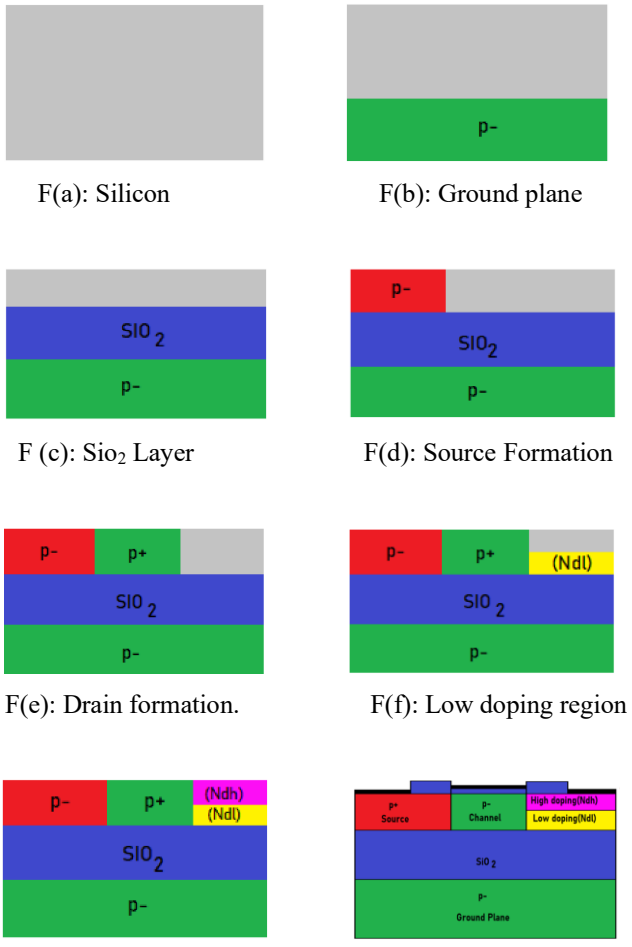
Variables	Values
Spacer length (Ls)	28nm
Thickness of silicon (tsi)	10nm
BOX Thickness	20nm
Thickness of Ground plane	20nm
Thickness of oxide (tox)	1nm
Thickness of doping region at drain (th)	2nm
Gate work function	4.3ev

Table 1: The dimensions and parameters are used in simulation of the proposed device.



F(a): Silicon F(b): Ground plane

F (c): Sio_2 Layer F(d): Source Formation

F(e): Drain formation. F(f): Low doping region

F(g): High Doping Regions f(h): Metallization

Fig 3: Tentative fabrication flowchart of the proposed device

The BTBT model used in the simulations within this paper has been calibrated following the arguments put forward by Boucart and Ionescu. It included calibration based on experimental data, so producers were constructed of fabricated IBM tunnel diodes. The calibration is shown in Figure 2 alongside Boucart's results. For achieving the best-fit electron and hole tunneling masses were assigned for electrons (me) and holes (mh) were set at 0. 11 and 0. 71, respectively. In our simulations, two distinct cases were considered: the first case was tunneling meshing only at the source/channel region (Simulation case I) while the second case involved meshing at both the source/channel and the drain/channel regions (Simulation case II). However, it is crucial to underline that the numeric results cannot be used for quantitative comparison of the proposed drain doping engineering with the conventional structure, as this paper aims to show only the relative shifts in the device characteristics due to the discussed modification.

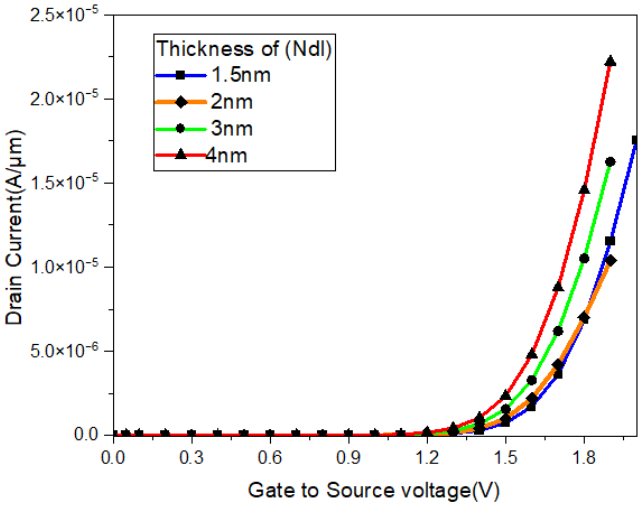


Fig. 4 Transfer characteristics of the proposed TFET with different high-doped drain region thicknesses at VDS = 1. V

In all simulations the doping level was kept constant; the source region was doped at 1×10^20 cm^{-3} and the intrinsic region at 1×10^17 cm^{-3}. For better Ohmic contact with the drain electrode the upper drain region was doped at 5×10^18 cm^{-3}. However, the lower drain region maintained the default doping concentration of 1×10^17 cm-3. The gate dielectric material used was SiO2 with tox of 1 nm and dielectric constant of 3.9 were employed. The work function of the metal gate was estimated to be 4.3 eV. Furthermore, it was defined that the gate length of the device should be 40nm while drain and source lengths should be 80nm. Depending on the device requirements, the thickness of the silicon film was set as 10nm, and the spacer length (Ls) followed the general standard of 28 nm. This study also included the high-doped region thickness as a varying parameter: However, it was maintained to be rather thin.

III. RESULTS AND DISCUSSIONS

The research paper examines the TFET intensively using an efficient tool known as the SILVACO TCAD ATLAS tool. Figure 4 itself shows a comparative study between the transfer characteristics of a conventional TFET structure and the proposed structure when the thickness is varied. As has been

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ISSN: 2278-0181
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observed, the ambipolar current varies strongly with the thickness of the high-doped drain region compared to the ON current. To clarify it is worth mentioning that the ambipolar current is indeed suppressed down to at least -0. 5 V, when 2 nm of the thickness is used, and at VGS = -0. At 8 V, the ambipolar current is remarkably low, even below that of the substrate. In addition, recent efforts in the GSM field do not adversely affect the suggested structure, as shown in Figure 5. This figure shows that especially for th = 2. Even at 5 nm, it is observed that there is minuscule difference between the proposed structure and the conventional structure in the output characteristics. To considerable note, all the mentioned simulations do not consider tunneling in the vertical direction, namely from the upper high-doped drain region to the lower one. Fig. 5. Output characteristics of the proposed structure with different values of VGS

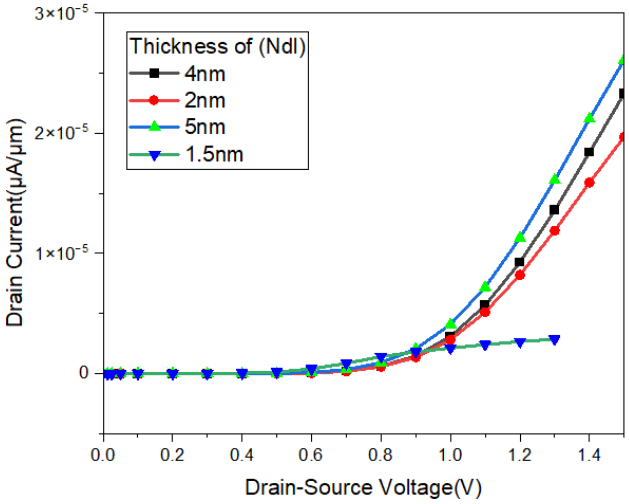

Fig. 5. Output characteristics of the proposed structure with different values of VGS

This is shown in Figure 6, which displays the conduction and valence bands for both the ON state (VGS = 1.2 V and VDS = 1.5 V) and the ambipolar state (VGS = -0.8 V and VDS = 1.5 V) for a thickness of th = 2.5 nm. As shown in figure 6, the conduction band closely aligns with the valence band primarily in the lateral direction. This alignment signifies that the Band-to-Band tunneling (BTBT) rates are nearly negligible in the vertical direction.

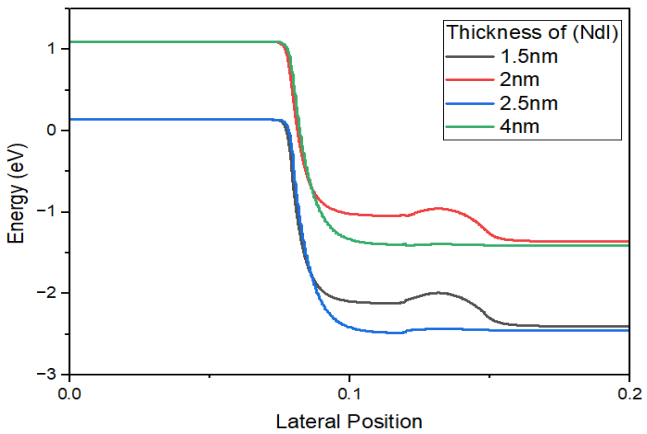

Fig. 6. Energy band profiles of the proposed TFET

However, we would like to note that the simulations do not include tunneling in the vertical direction from the upper high doped drain region to the lower region. Figure 6 helps in this regard as it offers understanding the conduction and valence bands of ON state (VGS = 1. 2 V and VDS = 1. 5 V) and ambipolar state (VGS = -0. 8 V and VDS = 1 V) if th = 2. 5 nm. If one examines this diagrammatically, it will easily be seen that the conduction band and the valence band change mostly in the lateral direction, as shown in the figure above. This critical observation means that the Band-to-Band (BTBT) tunneling rates are vanishingly small in the vertical direction. Omitting vertical tunneling becomes relevant to evaluate how far the proposed structure does allow ambipolar conduction. As a result of these improvements, lateral tunneling is the only tunneling that is observed, and this proposition makes a significant contribution to the reduction in ambipolar currents. To achieve a more accurate insight of the effect that the proposed method will have, the emphasis is made on the analysis of the nonlocal BTBT tunneling rates of both holes and electrons. Furthermore, plotting the energy band diagram besides the nonlocal BTB tunneling rates by tracing a cut line through both structures, located 1 nm below the Si–SiO2 interface. As illustrated in figure 6, the maximum observed was the enhancement of the minimum tunneling width using the proposed structure. This change in the tunneling width has a very important function of controlling the ambipolar current. Admittedly, ambipolar current itself is tunneling process, and the wider barrier width stated here enhances greatly its suppression. More precisely, this reduction in the thickness of the tunneling barrier decreases the number of ambipolar tunneling events that can occur, and thus consequently serves to decrease the overall ambipolar current.

This gives further confirmation of the effectiveness of the proposed approach and a clear physical position of how ambipolar conduction in TFETs is suppressed. To understand effects of thickness influence in a better way, performing an analytical work focusing on the minimum tunneling width at both the source and channel and drain part. Additionally, examining the corresponding currents, ION and Iamb, under two distinct operating conditions: the ON state, with VGS equal to 1. 2 V and VDS equal to 1 V and the ambipolar state, with VGS equal to -0. 8 V and VDS equal to 1 V. The effect of Wmin is more pronounced in the ON-state with a slight degradation of tunneling width and significant increase in thickness. Thus, ION does not vary with the thickness and the variations are observed only when the thickness is less than 2. 5 nm. Nonetheless, the influence of thickness on Wmin is larger for the system of ambipolar transport. The decrease of thickness will take a larger Wmin, which means that the ambipolar current will be suppressed. To further investigate the physical behavior especially in terms of the Band-to-Band (BTB) tunneling rates and Wmin the author considered it necessary to perform a detailed analysis on how the low-doped region influences the electric potential within the active Si region. Examining the 2D cross-sectional diagrams that depict potential distributions in the ambipolar state for both the conventional TFET and the presented structure – for the case when thickness has been set at 2.5 nm.

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Although, in the case of the conventional TFET the observed potential change seems to be slightly less than in the other two cases. Concretely, in the conventional TFET, the value of the potential rise is higher near the channel/drain interface, which corresponds to a narrower tunnel barrier width and a smaller Wmin. This compression is related to increased ambipolar current (Iamb). On the other hand, when thickness was set to 4 nm, the recording of a more extensive potential gradient was a sign of a steeper tunnel barrier. However, decreasing the thickness to 2. By applying 5 nm, there is a concomitant of a larger potential gradient meaning a wider tunnel barrier. Overall, these results underscore the importance of having two drain regions. The low-doped region also helps in effectively depleting the drain region at the channel-drain junction and thus enabling reduced tunneling barrier width and ambipolar current control.

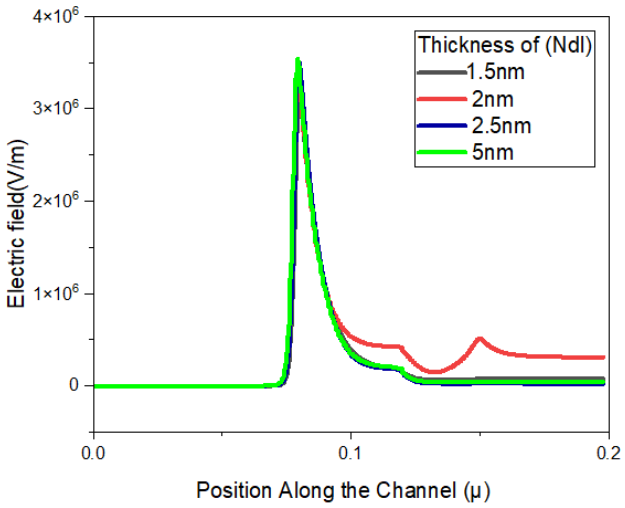

Fig. 7. Electric field of the proposed TFET for different drain doping thickness

Additional electric field analysis was carried out at the varying drain doping thickness, at 1. 5 nm, 2 nm, 2. 5 nm, and 4 nm, as indicated in Figure 7 above. These electric fields are especially useful in high frequency, and their usage cannot be further emphasized. First, there is the high-frequency performance which is most affected by the electric field since it influences the motion of charge carriers. In conditions of high electric field strength, it is easy to make fast and effective transport of these charge carriers. This phenomenon is of much significance in high frequency in the context of radio frequency (RF) as well as microwave communication system. A higher electric field gives the ability to charge carriers to move more rapidly, giving signals a boost. This is a key step in making high data rates and signal frequencies in the RF and microwave communication systems possible. Consequently, electric field intensity determines the span of frequencies that is usable in such applications. Hence, mastering and the proper positioning of electric field strength is a critical aspect of increasing operating frequencies and rates of high-frequency systems, which is one of the overarching goals in modern applications.

1)>Ft=(gm/2)(Cgs+Cgd)

A thorough analysis is carried out on high-frequency operating parameters of FETs, namely transconductance, drain-to-gate capacitance, source-to-gate capacitance, and the most important unit gain cut-off frequency. The results of this analysis are presented in the form of figure 8 which depicts cutoff frequency versus drain doping thickness. When comparing between the source-to-gate and drain-to-gate capacitances capacitance Csg remains invariant at all gate voltage values in both conventional and proposed TFETs. However, it reacts drastically different from the behavior of Cdg. As for the gate voltage below VGS ≈ 1.05 V, in the Cdg of the proposed structure, the upper region thicknesses are observed to be reduced. It is important to note that beyond VGS > 1.05 V, if the upper region thickness is less, then Cdg is slightly less for the thinner thickness regions. The transconductance (gm) has been evaluated in detail based on the thickness of the material at various thicknesses. Evaluating the change of the cutoff frequency with respect to the gate-to-source voltage, contrasting different cases of the proposed method with the conventional TFET. Analyzing the maximum cutoff frequency (fT max) in relation to the values varying from 1 to 10 nm. The understanding from the analysis is clear as crystal based on figure 8. The maximum cutoff frequency (fTmax), which starts with 60 GHz for the conventional structure is improved by a considerable extent when employing two layers of drain doping, beginning the upper layer thickness at 2 nm. The fT max is greatest when th is set at 2; this is an indication that the fT max has reached its optimal frequency. undefined Incredibly, if th is decreased to a dimension of less than 2 nm, fT max suffers a sharp decline. Hence, the choice of th seems to be highly sensitive, and it locates in the vicinity of 2. 5 nm or in its proximity.

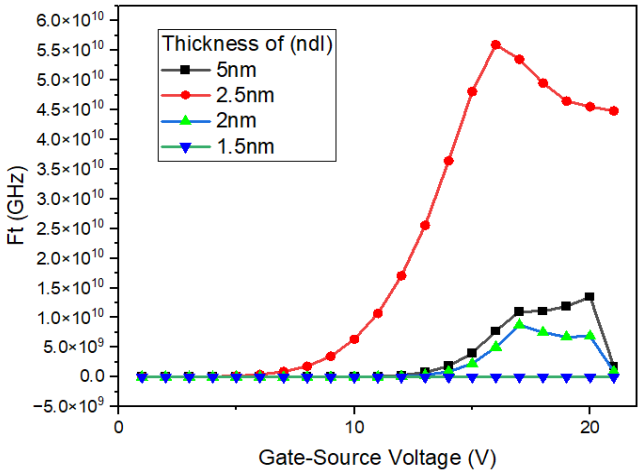

Fig. 8 Frequency of the proposed TFET for different drain doping thickness

In the next step directing focus to the spacer length (Ls) effect on ambipolar current measured at VGS = – 0.8 V and VDS = 1.5 V as well as the maximum cutoff frequency (Ft max). The purpose of this investigation has been performed for two different thickness of upper drain region which is th = 2 nm and th = 3nm. Strikingly, both trends are similar in these two cases. Integrating both the structural engineering with the doping engineering approaches into the device, including attaining a high frequency response greater than prior findings. Engaged in an investigation of important design parameters which substantially affect the performance of the device. From the decreasing ambipolar current (Iamb) at higher spacer length

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(Ls), it is evident that the length of the spacer cannot be increased to freely produce high speed output. This can be accounted for in the fact that the physical separation between the drain contact and the channel–drain interface is considerably longer than in MOSFETs. This results in a well-defined depletion region at the interface and increased distance from the junction. Whenever the spacer length is at 35 nm and above, there is virtually no occurrence of Iamb. But it is crucial to look at the fact that with these increased values of Ls the value of fT max, the maximum cutoff frequency decreases. Hence, it deserves careful thought concerning the selection of the proper value for the "Ls" with the aim of limiting ambipolar current while minimizing the influence used on the HF performance.

Variables	Conventional device	Proposed device
Spacer length (ls)	30nm	28nm
Source Length	80nm	100nm
Drain	80nm	100nm
Channel length	40nm	50nm
Doping thickness	5nm	2.5nm
Frequency	109	10^{10}
Gate work function	4.3ev	4.3ev
Electric field	------	4 x 10^{10}

Table 2: Comparing the Dimensions and Parameters in Simulation: Proposed with Conventional Devices

The effect of heavy doping (Ndh) as well as light doping (Ndl) on both Iamb and fT max must be compared. Figure 5 shows that ambipolar current increases with Ndl. Such behavior is typical for numerous doping of the higher drain region. What makes it much more interesting is that the variation of fT max is also varying as well at the same time. For Ndh of 6×10^18 cm−3 × 7×10^17 cm-3 the fT max shows almost linear dependence on Ndl, but for Ndl above 1×10^18 cm-3, there is a steep fall in the fT max value. For Ndh equal to 5 × 10^18 cm-3 fT max depends on Ndl and with its increase from 0 to 1 × 10^18 cm-3 the value increases and then sharply decreases with addition increase of Ndl. Such results show that there is an optimal method of drain doping that can lead to high frequency performance together with moderate ambipolar current. Sustaining such operation is central to high-frequency operation and thus underlines the precision required for set parameters in a device design.

IV. CONCLUSIONS

In this paper and for further evaluation of the cutoff frequency (fT), we used 2D TCAD simulations coupled with a comprehensive analysis of the structure of the device and drain doping concentrations. We examined four different drain doping thicknesses for the drain doping layers, namely 1. 5nm, 2 nm, 2. The optical band gaps of Composites 1, 2 and 3 were found to be 5 nm, 4 nm respectively. Among them, thickness of 2. Compared with other mob versions, 5 nm displayed the maximum cutoff frequency of response, standing at a record of high-frequency operation. These parameters consisted of the thickness of high doped drain region, spacer length and the dopant concentrations in both the low doped and high doped drain regions. This coverage gave us a better understanding of the influence of these factors on different performance characteristics including ON current, ambipolar current and cutoff frequency among others. Notably, we also observed that the ON-current levels are relatively stagnant irrespective of the design configurations. Furthermore, it was established that capacitance values were significantly boosted, especially up to an initial gate voltage of about 1V. 5 V. More importantly, these results are aligned with the capability to improve high-frequency characteristics based on a rational design strategy, particularly in terms of the changes to the thickness of the upper layer as well as doping levels. Not only does this pitched investigation make high-frequency devices demonstrate their merits, but it also provides us with explicit insights into these merits.

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