Enhancing ARM core capability using PSoC5 Bhargav C. Goradiya¹, Dr. H.N. Pandya²

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Abstract

ARM core is being utilized by the different manufacturers for the different applications. Here we are suggesting Cypress make PSoC5 consisting ARM core for enhancing the power of mixed signal processing. In this paper we are presenting the effective signal conditioning using Programmable System on Chip PSoC5. PSoC5 is highly enhanced ARM core architecture which consists of various analog and digital blocks. As the trend is to conserve the power in any application PSoC5 provides custom on and off of the block or the modules which are in use & thus offer better power saving feature. In this paper we are showing real time temperature monitoring and data logging application based on programmable system on chip with ARM core. The design can be used for the patient monitoring and history analysis. Even it can be used for data acquisition system for multiple sensors for industry.

1. Introduction

ARM core is being enhanced by different vendors; Cypress has come up with the CY8CKIT001 development kit which consists of PSoC CY8C55 (PSoC5) family processor module as one of the option. PSoC5 comprises 32-bit ARM Cortex M3 core running at 80MHz with integrated USB device support, analog and digital blocks, and in-system debugging capabilities.

Real time monitoring of various parameters are really essential for bio-medical analysis and to avoid catastrophic action in industry. Parameters can be Temperature, Pressure, Speed, Flow etc; which needs to track for the smooth conduction and at times for taking corrective measures. Mainly design involves selection of the sensors, signal conditioning, A to D conversion and display and monitoring of the data on the central computer.

We propose a design of real time temperature monitoring and data logging based on PSoC5 with ARM cortex-M3 core. Design usually required interfacing different analog and digital block which requires multiple chips and their power, speed issues. PSoC5 gives a single chip solution with selectable modules controls the on/off of the module and thereby power efficient. Apart from that system is more reliable and gives flexibility of design. The same design can be duplicated for other parameters like pressure, flow, speed etc; even for multiple sensors and data acquisition systems.

2. Hardware design of the system

The temperature measurement system requires a transducer to convert temperature into an electrical signal. There are different kinds of

temperature sensors available we are using LM35 it can be easily replaced by the different sensor as per the need of the application. The sensor module is connected with prototyping breadboard of the development kit.

The block diagram of the system is shown in figure 1. It is consisting of sensor module, the output of the sensor module is directly connected to (PSoC5 selectable) signal conditioning, the amplified signal is then converted to digital format with help of ADC



Figure 1 System block diagram

(sigma delta) then the converted digital data is processed by the ARM cortex M3 core. The processed output equivalent to the temperature is given to display and also made available to central computer through USB-UART converter. The hardware setup is shown in figure 2.



Figure 2. Snap shot of hardware setup

The tool which is used to work with PSoC5 is PSoC Creator which provides IDE for the Cypress make PSoC. The actual hardware is to select from the available modules and top diagram schematic is to develop. System schematic is shown in figure 3. For individual block like PGA, ADC etc; parameter setting is to be done as per the requirement. Once the parameters set the module behaves as per the properties set in the module. Here for the design pin 1 is connected with the output of the temperature sensor and pin 2 is connected with the ground for the reference of inverting amplified.



Figure 3. Hardware diagram Schematic

After the schematic is prepared pin assignment is to be done, this pin assignment will actually map the input output of the system with the pins of ARM core. The pin view is shown in figure 4.



Figure 4. Pin view

3. Firmware

The firmware for the system is implemented on PSoC5 using ARM Cortex-M3 controller programming instruction set. The system component required in the system must be configured first by the software initialization by the various parameters passing and calling appropriate routine. The selected block of the PSoC chip must be turn on by activating power source which is controlled through instructions. The flowchart of the system firmware is shown in figure 5.

The firmware starts with initializations of the PSoC5 digital and analog block. After initialization of the block the individual component is required to make powered, which is done through PSoC API functions. The algorithm continuously checked whether data available from ADC output. If data are available from the ADC data are displayed on the LCD display.

The acquired data is transmitted through a USB to UART converter module interface to PC. The data received on pc can be captured on GUI based terminal software which is available as open source. The baud rate for UART module in the PSoC is set to 9600 bps and one stop bit. However the baud rate can be change for other setting requirement in the PSoC UART module. The received data on pc can be stored in a file in data recording. The snap shot of the terminal software is shown in figure 6.



Figure 5 Flow chart

COM Port	Baud rate		Data bits	Parity	Stop Bits	Handshaking
	C 600 C 14	400 C 57600	C 5	none	@ 1	none
Disconnect COM3	C 1200 C 19	200 C 115200	C 6	Codd	1.000	C RTS/CTS
About. 2 CRM4	C 2400 C 28	800 C 128000	C 7	C even	C 1.5	C XON/XOFF
	C 4800 C 38 © 9600 C 56	400 C 256000 000 C custom	• 8	C mark C space	C 2	C RTS/CTS + XON/XOFI C RTS on TX
E Stau on T	DD CB-LE	9600	27 🔺	ADDIRADIE		
Beceive Stay on T	op 🔽 CR=LF	9600 7384 C HE G Striv	27 🚖	tLog StopLog		
CELAR Reset Counte	op CR=LF	9600 7384 CHE Striv	27 🚖	tLog StopLog		
CLEAR Reset Counter 05Dh 05Dh	op 🔽 CR=LF	9600 7384 CHE) Striv	27 🚖	tLog StopLog		
Stay on T Receive CLEAR Reset Counter 05Dh 05Dh 05Dh	op CR=LF	9600 - 7384 C HE2 © Strin	27 🚖	ntLog StopLog		
Stay on T Receive CLEAR IOSDh IOSDh IOSDh IOSDh	op CR=LF	9600 • 7384 C HE2 • Strin	27 🚖	tLog StopLog		
Stay on T Receive CLEAR Reset Counter 105Dh 105Dh 105Dh 105Dh	op ☐ CR=LF	9600 7384 C HE Strin	27 🚖	tLog StopLog		

Figure 6 Terminal software snap

The received data recorded in a log file can be used for history analysis and to take corrective measures. Figure 7 shows the log file for terminal which indicates the data recorded for a period of time.

📄 terminal - Notepad															
File	e E	dit	Form	nat	Vie	w	Help								
Terminal		log file													
35 68 30 68 50 50 50 50 50 50 50 50 50 50 50 50 50	41 0D 39 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 41 41 41 41 41 41 41 41 41 41 41 41	68 30 68 35 68 5 68	0D 30 0D 41 30 00 00 00 41 30 00 00 00 00 00 00 000 000 000000000	30 35 30 68 35 68 35 68 35 68 35 68 35 68 35 68 30 68 35 68 30 68 35 30 50 50 50 50 50 50 50 50 50 50 50 50 50	30 41 30 0D 41 30 00 0 0 00 00 00 00 00 00 00 00 00 00	35 68 30 80 50 80 80 80 80 80 80 80 80 80 80 80 80 80	41 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 41 30 0D 41 41 30 0D 41 41 30 0D 41 30 000 41 30 00 0 0 1 30 00 1 30 0 0 1 30 0 0 1 30 0 0 1 30 0 0 1 30 0 0 1 30 0 1 30 0 0 1 30 0 0 1 30 0 0 1 30 0 0 1 30 0 0 1 30 0 0 0	30 68 35 68 30 80 68 30 68 30 80 80 80 80 80 80 80 80 80 80 80 80 80	30 0D 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 3000 41 30 00 00 41 30 00 410 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 40 00 00 00 00 00 00 00 00 00 00 00	35 30 68 35 30 50 50 50 50 50 50 50 50 50 50 50 50 50	39 30 0D 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 30 00 41 30 00 30 30 30 30 30 30 30 30 30 30 30	68 35 30 68 35 30 68 35 35 68 35 35 68 35 30 68 35 5 8 5 8 5 5 8 5 8 5 5 8 5 8 5 8 5 8	0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 41 30 0D 41 41 30 0D 41 41 30 0D 41 41 30 0D 41 41 30 0D 41 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 0D 41 30 00 41 3000 4000 4	30 68 35 68 30 80 80 80 80 80 80 80 80 80 80 80 80 80	30 0D 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 3000 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 41 30 00 0 00
68	0D	30	30	35	41	68	0D	30	30	35	41	68	0D	30	30

Figure 7 Terminal Log file Snap

4. Scope & Future work

The design proposed with PSoC5 having ARM Cortex m3 core can be easily used for industrial and bio-medical applications. There is enormous scope of such kind of design which consumes less power, cost effective and faster. As the block which are available in PSoC are having custom on/off facility it is really power efficient.

The data received on the computer through terminal software can be analysed further for various off-line processing like plotting & storing of data.

The design based on ARM can be easily extended for multiple sensors as PSoC5 supports multiple inputs sensing capability. Data Acquisition System can be implemented for multiple inputs by utilising the needed block of PSoC5.

5. Conclusion

The design based on PSoC5 ARM core is more reliable and consuming less power compared to other ARM core because of its reconfigurable analog & digital blocks, ARM core with System on Chip is the need of the time. Unlike the other ARM core PSoC5 ARM core offers best flexibility in terms of Speed, Power and Cost.

6. References

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