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EUV: A New Adventure in Lithography

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Abstract— **Broadband topics like history, tool, source, resist, mask and even projection optics are included and reviewed in Extreme Ultraviolet Lithography (EUVL). EUVL has become the leading lithography technique in semiconductor manufacturing thanks to its short wavelength and therefore the ability to realize high-resolution patterns. EUVL has begun to use for top-volume manufacturing (HVM) of 7nm and 5nm logic nodes, and therefore the main benefits are enabling faster time to plug and better interconnects performance compared to other multiple patterning solutions by chip manufacturers. Over time, there are parallel developments in optics, exposure tools, resist metrology, and mask technology, many of which are been related to changes within the wavelength of light used for leading-edge lithography. During this review, various aspects sort of a mask, resist, and light source are discuss alongside the benefits, drawbacks, and future scope.**

***Index Terms*— EUVL, HVM, Lithography, wavelength.**

I. INTRODUCTION

The need for smaller and smaller structure has involved new pattering solutions, a number of them involving the extension optical principles, parallel patterning, and step and repeat by step and repeat by covering the surface of silicon wafers with consecutive exposure of identical patterns, projection of demagnified patterns from a mask onto the wafer rather than proximity printing. In 1986, Hiroo Kinoshita proposed the utilization of extreme UV (EUV) because the consequent continuation of photolithography with smaller wavelengths, which suggests 13.5 nm rather than 193 nm from deep ultraviolet (DUV) [1]. However, rather than transmission lenses, mirrors need to be used; also, the mask has got to be operated in reflective mode. EUV projection lithography (EUVL) will enable us to travel back to single mask exposure rather than double or quadruple exposure, a minimum of for the approaching node N7 and later N5.

Lithography is like photography therein it uses light to transfer the image onto a substrate, the term lithography springs from the words ‘lithos’ meaning stone and ‘graphy’ meaning write. Our stone may be a silicon wafer and writing is completed employing a photosensitive polymer. Extreme ultraviolet lithography is a sophisticated technology for creating microprocessors 100 times more powerful than those made today make, this lithographic technique utilized within the high-volume manufacture of integrated circuits. Over time, there has been an evolution within the sorts of problems that are the main target of lithography (Fig. 1) [2]. An example of the increase of activity on a selected topic in lithography over a period is illustrated in Fig. 2. a number of papers on resolution enhancement techniques (RETs) were presented at the SPIE Advanced Lithography Symposium in 1989 and 1990, and this was followed by several years of a way higher level of activity. Early lithographers worked on solutions for practical problems. Theoretical modeling was introduced and developed over time to greater levels of sophistication, eventually leading to the resolution enhancement techniques (RETs) and optical proximity corrections (OPC) that are in common use today. During the time period during which these methods were being developed, numerous research and development engineers at multiple companies worked on them.

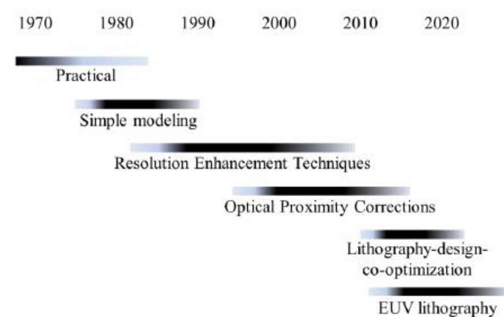

Fig 1. Periods of intense activity of lithography R&D.[2]

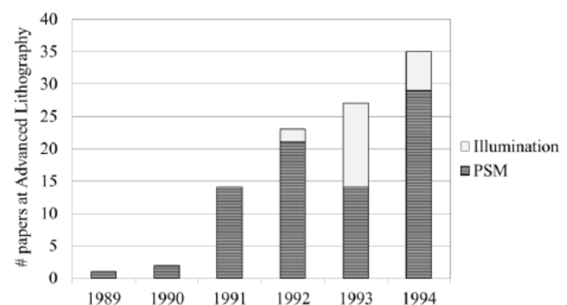

Fig 2. The amount of papers presented at the SPIE Advanced Lithography Symposium on the subject of resolution enhancement techniques.[2]

During the transition between 45-nm and 32-nm logic nodes, there wasn't a concurrent significant increase within the resolution of optical exposure tools [2]. As a consequence, to realize the specified pitches, at values of k1= 0.35 and lower, patterning is required. Even with well-stocked RET and OPC toolboxes, at such values for k1, it became impossible to pattern logic layouts that were direct shrinks of prior designs or ones with only minor modifications. This necessitated substantial changes in design styles and close interactions and cooperation became required between lithographers and designers. for instance, unidirectional lines and spaces are more easily patterned at low values of k1 than complex 2-dimensional shapes. However, significant layout effort was required to avoid enlarged logic cells with this new design style

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[4]. Sometimes it had been necessary to feature levels to the method to realize desired cell sizes, but this is able to increase overall wafer costs.

The need for greater collaboration between lithographers and designers took another quantum jump with the introduction of multiple patterning.[5] additionally to the standard design-rule restrictions supported feature size and shape, specific layouts that would not be composed into two patterning steps became prohibited. For applications involving interconnects which is made with multiple patterning, are requiring the designers inputs from lithography which is provided by the older version of EDA tool.

Defining new technology nodes has become increasingly complicated. Due to design restrictions, shrinks are not any longer proportional to changes in pitches. Rather, the size of actual logic and memory cells must be determined, after which routing efficiency must be calculated together with estimations of wafer costs, the worth proposition of a replacement technology node, in terms of cost per transistor, are often determined. (Fig. 3)

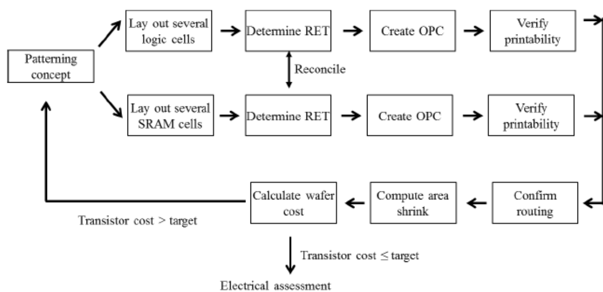

Fig 3. Work process flow for deciding on new patterning concepts.[2]

II. COMPARISON BETWEEN DIFFERENT LITHOGRAPHY TECHNIQUES

There is much work being done on various lithography technologies. However, optical systems are still dominant within the industrial environment. the appliance for electron beam systems is steadily developing. Ion beam systems are beginning to be used as a special too1 for direct patterning instead of for lithography applications.

X-ray lithography remains only under investigation [6]. There are too many problems with it that has to be solved before applying it to practical use. Conventional optical lithography technology seems to be the main candidate for half-micron technology. However, for beyond half micron technology.

There are not any clear solutions. Excimer laser lithography still has many problems not only in hardware but also in resist materials and resist process technologies. The most important problem in beam lithography is low throughput. Without solving this problem.

There is no possibility for the utilization of beam lithography within the mass production process line. A decrease within the number of process steps is extremely important for all lithography technologies. From now of view, x-ray features a great advantage over other technologies [6]. An entire lithography system should be developed for x-ray lithography first. Otherwise, it will have not any chance for industrial application.

Since the event, the speed of ULSI is quicker than that of x-ray technology. Ion beam lithography has distinct features. Utilizing these features, several special applications are going to be developed. Although optical lithography is most typical, there exist other lithographic techniques, as depicted in Figure 4.

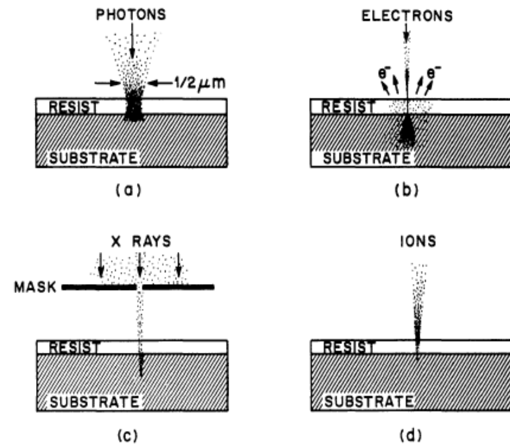

Fig 4: Types of lithographic methods. (a) Optical lithography. (b) Electron lithography. (c) X-ray lithography. (d) Ion lithography.

Optical lithography is the mainstream technology and a few commercially available resists can resolve all the way down to 0.1 µm or lower. Figure 5 shows the estimated resolution offered by the varied lithographic techniques. The borderline of every technology is somewhat fuzzy. Optical lithography is taken into account difficult to use for a design rule of much but 0.1 µm because of its resolution limit. Electron beam direct writing or x-ray lithography are the only two remaining options for deep sub-micrometer structures.

However, perfect x-ray masks are difficult to form and therefore the throughput of electron lithography is slow. For mass production, the price and footprint (required floor area) of the machine must even be minimized which might be done using Optical lithography i.e. EUVL.

III. WHY EUVL?

It is required for continuity of Moore's law, the number of transistor that can be placed inexpensively on an IC doubles approximately every year.[11]

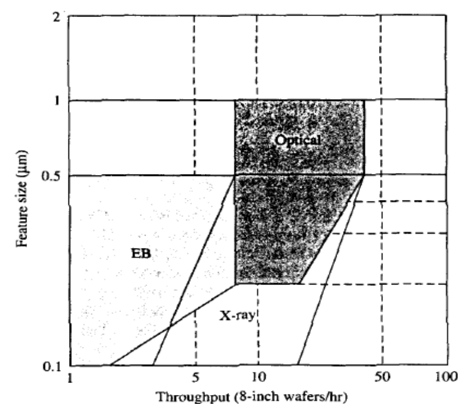

Fig 5. Resolution and throughput of sub-micrometer region for optical lithography, x-ray lithography and electron-beam (EB) lithography.

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EUV (extreme ultraviolet lithography) lithography is a lithography technique, which uses EUV light having an extremely short wavelength of 13.5 nm. It allows exposure of fine circuit patterns with a half-pitch below 20 nm that can't be exposed by the standard optical lithography techniques. With the event of EUV lithography, Moore's law still holds true.
This lithography technique is predicted to revolutionize state-of-the-art semiconductor manufacturing. The semiconductor industry as an entire is innovating within the EUV space because it transitions high-end technology production from 193 nm to EUV. EUVL is a next-generation technique. There are variety of next-generation lithography techniques like X-ray Lithography, beam lithography, and Nano-imprint lithography that are in a race with EUV Lithography. [8]
However, the EUV Lithography technique prevails over its contemporaries because it caters to the upcoming scaling demand for printing of smaller features. Lithography tool manufacturers have gradually reduced the wavelength of light i.e., Extreme Ultraviolet used for designing imaging system using this technique. EUV (Extreme Ultraviolet) lithography uses a EUV light of the extremely short wavelength of 13.5 nm. Using ArF excimer laser, older version of optical lithography cannot be exposed but with a half-pitch below 20nm of fine circuit, patterns will be allowed.

IV. EXTREME ULTRAVIOLET LITHOGRAPHY (EUVL)

The recent advance lithography technology, which is utilized in high volume manufacturing (HVM), is ArF Immersion lithography with double patterning. In addition, triple pattering is required if SrF immersion lithography is used in 7nm, along with that for 5nm quadruple patterning is used [19]. Nevertheless, when it comes to pattern shaping and cost this multiple-exposure patterning lithography techniques are having more advantages rather than any single layer resist process using EVU lithography [1]. For this reason, instead of ArF immersion lithography for multiple exposure, EUV lithography is used for single layer process.
In current scenario, some chip suppliers in the world are planning to apply EUVL to mass production for some mask pattern from 2018 to 2020 [13]. EUVL is planned to be used in the semiconductor electronics devices insertion to HVM for the patterning in 7nm node around 2018. EUV Light source power of 250W with the occupancy rate of 75% is required for the HVM EUV light source, and for the EUV power for 100W, EUV light source based on the free electron laser source is planned based on the accelerator technology [14]. For EUV resist development, the similar achievement of the high resolution, sensitivity, low LER, and low out gassing is required. For the mask development, the defect inspection of the actinite blank and patterned mask, and the pellicle to protect the mask from the particle originated from the mask loading and unloading in the exposure too are required [14].
The industry is rapidly approaching the 22 nm half pitch (hp) node for MPU and DRAM as outlined in the International Technology Roadmap for Semiconductors (ITRS) [15]. By now, leading edge device manufacturers have made their decisions on which lithography technology to use for this node; all of them are pursuing multiple patterning 193 nm immersion (MP 1931) lithography as the primary choice [18]. If EUVL should meet productivity and yield requirements, companies can be expected to be opportunistic in inserting EUV at 22 nm hp for select layers to realize cost savings vs the more expensive MP 193i option. However, if EUV does not meet those requirements, its HVM introduction could yet be delayed one further node to 16 nm hp [18].
An additional set of lithography activities has focused on changes in the wavelength used for leading-edge lithography, and there have been several such transitions since the first use of wafer steppers as exposure tools [2]. With a significant amount of research and development in lithography witrh a new wavelength is accompanied for resists, masks, exposure tools, metrology and process control which are the new capabilities required. Shown in Fig. 6 is the trend in the number of papers on DUV lithography in the SPIE Advanced Lithography Symposium proceedings. As shown in Figure 2, the increasing number of papers was more gradual than RETs, for DUVL. In addition, it became a consequence for significant number of problems, which DUVL will encounter daily, such as resist t-topping and poor laser reliability [2]. Eventually number of papers involving DUVL is growing very fast, but the aspect of wavelength is it taken into consideration nor even references; since DUV wavelengths are standards for leading-edge lithography for several years, the focus was often to other aspects of those papers like, overlay of lithography or design-for-manufacturability.

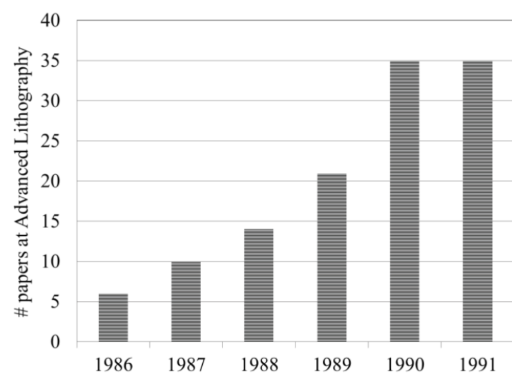

Fig 6. Number of papers on OPC in the proceedings of the SPIE Advanced Lithography Symposium [2].

From ArF lithography to EUV lithography, the transistion is most recent variation in terms of wavelength which is under consideration.Increasing level of research and development has a subject of EUVL and by 2010, SPIE Advanced Lithography Symposium noted that there were sufficiet subbmission that is seperating EUV Lithography Conference.
Moreover, in 2016 Symposium, there are multiple join session on the EUV resist materials between EUVL and Advances in Patterning Materials and even Processes Conferences. At the time of DUVL, similar situation arises. [2]. The magnitude of the challenges associated with EUV lithography has resulted in a state where the number of papers on EUV lithography has remained high and is not expected to taper rapidly, which was the case for several of the other topics that were the focus of interest over short periods but then became part of background knowledge [20].

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V. ASPECTS OF EUVL

There are various aspects for EUVL that is taken into consideration like EVU light source, EUV Resist, EUV mask and many more.

A. *EUV Light Source*

The EUV light source remains the most difficult challenge for EUV. Without sufficiently high source power and a mature source technology that provides for high source reliability and uptime, EUV will not be used in HVM. The target the iindustry has set itself to support a 22 nm hp EUV HVM introduction is to deliver 125 W at the intermediate focus (IF) in 2014 and 250 W in 2015.

To achieve this, the power of the CO2 laser that is used to produce EUV radiation by generating a highly ionized Sn plasma has to roughly double the 15kW used in beta tools, and the conversion efficiency from the 1064 nm CO2 wavelength to the 13.5 nm EUV wavelength has to double to ~3% [21]. The pre-pulse technique used to condition the Sn droplet target for the main CO2 laser pulse is critical to optimizing conversion efficiency. The pre-pulse wavelength can be the same as the main pulse (i.e. CO2 wavelength) [21] or a different wavelength can be used [22]. Depending on the set-up, up to 6% is the maximum conversion efficiency which is predicted. The highest power values reported so far with the pre-pulse system are in the 50W range with a recent value of 70 W reported for a short duration of six minutes [21].

Laser plasma (LPP) X-ray source, which in which Sn droplet is used as a target in the main stream of EUV light source. Sn droplets excited with YAG laser, and then during a 25kW CO_2 laser irradiation, EUV light wavelength of 13.5 nm is generated. At the focal point 250W power is requires of EUV light source. In today's scenario, the EUV light source installed in the exposure apparatus of ASML NXE-3350B achieved a power of 250W, and it is possible to expose 12-inch silicon wafer at the throughput of 125 wafers per hour. Fig.7 shows the transition of the EUV light source power so far.

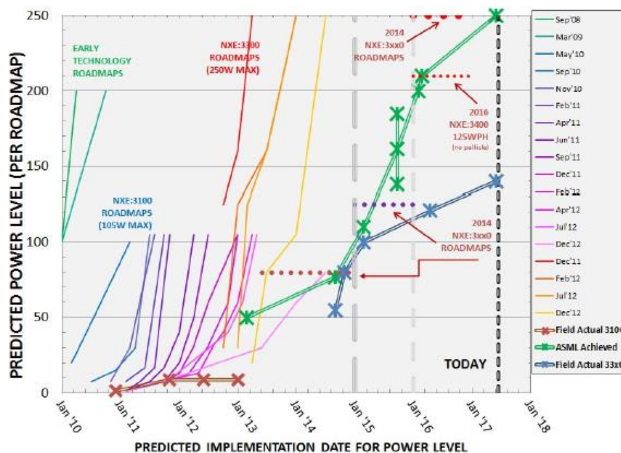

Fig 7. Transition of EUV light source power
(Provided by INTEL)[13]

B. *EUV Resist*

EUV resist materials have seen a significant improvement in resolution over the past two years with chemically amplified resists (CAR) now demonstrating modulation down to 16 nm half-pitch and below. This has been very much help by a set of consortia supported; small-field EUV exposure tools that enable materials supplier's rapid cycle learning. Resist sensitivity varies between 10-20 mJ/cm2 for line and space resists and 30-70 mJ/cm2 for contact hole resists [18]. All resist materials still produce a line width roughness (LWR) significantly higher than the ITRS specification. LWR reduction in post-exposure processing is seen as the key element to meet the post-etch "transferred LWR requirements". This applies to line/space resists as well as contact whole resists. For the latter, mask biasing is required to reduce the exposure dose and to meet contact hole uniformity and contact edge roughness metrics [18].

To meet HVM requirements certain improvements are required for resist material, to support HVM at 22/16 nm hp there is a gap for resist material, which is much smaller than the gap that source and mask technologies still face. To overcome the limitations of CAR materials with respect to resolution and LWR, novel non-CAR materials platforms are been developed: prominently among those are nanoparticle resists and organometallic materials [25, 26].

Specification of EUV resist required for 5nm node are resolution of 10nm or less, exposure 15 mJ/cm^2, LER of 0.1nm, and low outgassing. Among them, the exposure sensitivity is related to throughput, and LER greatly affects the electrical characteristics of the devices. For this reason, it is necessary for the EUV resist to satisfy high sensitivity and low LER. Resist is categorized as chemically amplified resist [27-29] and non-chemically amplified resist. Furthermore, each resist can be classified into a polymer type and a low molecular resist.

C. *EUV Mask*

Using CAD systems the patterns are been generated for VLSI and ULSI. The digital CAD output drives a pattern generator that transfers the patterns directly to the photosensitive masks [31]. Using chromium or iron oxide mask are generated from glass covered with hard surface material. On the final IC yield, number of mask defects has an effect, which is defined as the ratio of good chips per wafer to the total number of chips per wafer.

Defect-free EUV mask blanks are the other big challenge that needs to met before EUV can be successfully used in manufacturing. This starts with the surface quality improvement of the glass substrates on which the Mo/Si Bragg reflectors are been deposited. After Mo/Si deposition, the defects of Pit and bump type of the glass surface should be small that it would not result in printable defects. Achieving this will require improvements in existing fine polishing techniques, the introduction of new methods such as Dressed Photon Nano-Polishing (DPNP), and improvements in substrate cleaning [18].

The next step where defects need to be reduce is the reduction of handling induced defects that are deposit on the glass surface before deposition. Last, defects produced during the deposition process must be eliminate. The best mask blanks—40 bi-layers of Mo/Si with a Ru capping layer—have a handful of defects in the 50 nm size range and no defect larger than 100 nm (so called killer defects). These numbers need to improve to < 10 defects at 40 nm size and 0 defects > 80 nm achieved at a manufacturing yield of 30% or higher.

Defect generation during the absorber deposition is not seen as a significant problem. In addition, absorber deposition itself

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can be used to cover up a limited number of mask blank defects through patter shifting that otherwise would print. However, this requires blank inspection tools with sufficient defect sensitivity and coordinate accuracy to pinpoint defect locations. Such blank inspection tools are available in the optical range and a commercial actinic blank inspector with this capability is currently being built [30].

VI. WHAT'S NEXT?

Projection Lithography is possible by small featuring with aerial images, with the help of resolution provided by short EUV lithography. For example, with k1 of 0.35 20nm pitch can be resolved and a NA of 0.5. Still, with current 0.33 Numerical Aperture tool EUV's optical resolution is not been achieved. 28nm pitch resolution can be achieved with k1 of 0.35 and NA of 0.33, but pitches should be greater than 30nm are achieved, at least with good pattern fidelity. Line-edging roughness(LER) is one of the limiting factor for resolution. In large measure LER results are appreciated from Quantum effects, such as molecular inhomogeneity and photon shot noise. As dimensions shrink, such effects can only increase in significance [2].

VII. ADVANTAGES, DRAWBACKS & CHALLENGES AHEAD OF EUV LITHOGRAPHY

There are various advantages of EUVL, which includes:

1) Microprocessors made by EUVL are up to 100 times faster than today's most powerful chips
2) Decrement in size of chip but the speed of the chip increases.
3) EUVL technology attains good profundity of focus and linearity for both dense and isolated lines with low NA.
4) Increase in storage capacity.
5) The good image placement can achieved via low thermal expansion substrates.

Along with the advantages many drawback are even there which includes:

1) Positive charging, due to ejection of photoelectrons
2) Contamination deposition on the resist from out gassed hydrocarbons, which results from EUV- or electron-driven reactions.
3) No known method for repairing defects in a ML coating.
4) Entire process has to be carried out in vacuum.
5) Only 70% reflective mirrors are used.

Major challenges for EUV in near future are:

In EUVL, at 13.5nm wavelength, light is been converted from plasma via power source. Before hitting the wafer of printing small features on wafer, the light hits the mirrors several times and it bounces off. EUV faces several challenges of light source, equipment downtime among other, despite of having several advantages. Requirement of high-power light source in form of high-power light source to illuminate photoresist is the biggest drawback in the path of EUVL.

The failure to develop a light source with enough power has been one of the primary reasons behind delay in commercial use of EUV lithography [32]. Capability to generate 450W radiation with the radiation power of 250W is the current shipping equipment of ASML. Reliability of EUVL can be improves by the production of high power light source. In developing a photoresist for EUVL, a major challenge, which comes in a way of success, is the strong absorption of EUV radiation by all materials. The absorption depth in standard resists used today is less than 100 nm. At the surface of the resist, EUV resist will be structured so that printing occurs in a thin imaging layer at the surface of resist. Moreover, EUV resist materials will be evolve with upcoming evolution with respect to light source technology [32].

SUMMARY

EUVL will definitely open a new chapter in semiconductor industry. Successful implementation of EUVL will enable processors to operate very high speed with small size. EUV lithography is solidly on a path to HVM insertion, with timing determined by technology readiness and cost effective significant progress, as demonstrated by exposure source power meeting the projected power roadmap as well as the creation of printable-defect-free EUV masks and commercial pellicles, provide credibility in achieving the performance needed to support HVM. To take the full advantage of optical resolution of EUVL, manifestations of molecular-level effects is also becoming an evident.

With respect to resist, development progress is still expected, and development is being promoted mainly for metal resist to increase sensitivity with the help of Chemical Amplification PR, and decrease the swelling issue, which changes the thickness. Much work is to be done to overcome disadvantages, but in the end, our industry will optimize the technical trade-offs of lithography for the lowest cost of production of the chips that consumers want.

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