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Evolution of CMOS Technology

Past, Present and Future

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***Abstract*— This paper presents innovation of CMOS and CMOS technologies. The performance of integrated circuits has been improving exponentially. This can be achieved by minimizing size of CMOS. For faster processing demands in market CMOS technologies are upgraded. Minimizing size should reduce power consumption as well as boost speed. Today Graphene is the material which is used in industries for CMOS design. IBM engineers built a very fast chip, 10000 times faster using graphene. SiC (Silicon Carbide) wafer covered with graphene for designing a high performance transistor. As computational devices becomes more and more faster, the reason behind this is innovation of new CMOS technologies. Every company can't develop most advanced technologies. Also for designing a HCMOS, the material used are III-V/Ge and Graphene. Now CMOS devices designed using Non-Planar technology replaces conventional CMOS devices with planar technology. Three-dimensional technology have tendency to reduce power consumption, size of integrated circuits and increase speed than conventional two-dimensional technology. But it is very difficult to replace the Si-CMOS with new semiconductor material based CMOS.**

Keywords—Graphene; CMOS scaling; HCMOS; Wafer;

I. INTRODUCTION

CMOS technology was invented in 1963 by frank wanlass while he was working at Fairchild semiconductor. CMOS is a combination of N-type and P-type MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor). CMOS technology is used for constructing integrated circuits, microprocessors, microcontrollers, sensors, RAM (Random Access Memory) and many more digital circuits. Gordons Moore observed that number of transistor doubles after every 18 months in an integrated circuit [1]. This computerized electronics world demands more and more faster devices. This can be achievable by scaling CMOS technology from fraction of millimeters to few of nanometers in today technologies [2]. From past few years Non-Planar(3D) technology by industries. This make ease towards manufacturing high speed IC's, Processors and other electronic devices. Scientist make a very sharp reduction in size of CMOS to 7nm in future CMOS technologies [3]. Graphene is preferred to be used for future and today in 3D(three dimensional) technology. Latest material used for CMOS design is Graphene [4]. Graphene have very attractive properties: high electron and hole mobility, planar structure, high thermal conductance, high current carrying capacity and thin body [5]. All properties are sufficient for designing a high performance CMOS. Innovations of new technologies is very important for downsizing of CMOS integrated circuits [6]. As scaling down of CMOS size after every decade is difficult and we have to face some problems while downscaling of CMOS exceeds certain limit.

II. INNOVATION OF CMOS

After bipolar junction transistor MOSFET(Metal-Oxide-Semiconductor Field Effect Transistor) comes with very interesting feature like: low power consumption, low operating voltage, higher speed etc. which make MOSFET useful in electronics design. Two types of MOS transistor PMOS and NMOS are invented and used for designing integrated circuits. Both types have very high static power consumption. This problem is solved if and only a logic designed in such a way that it consumes no power in static state. After decades Frank Wanlass introduces a new logic designed using two complementary p-type and n-type MOSFETs. Two main advantages of CMOS technology is high noise immunity and very low static power consumption [7]. The last several decades have seen innovation of new CMOS technologies with excellent features. The trends of MOS integrated circuits downsizing

(1970) (2D technology) 10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm (2005) → 32nm (2007) → 28nm (2009) → 22nm (2012) (3D technology) → 15nm (2013) → 10nm (2015) → 7nm (2017)

Fig.1. Trend of downsizing for MOS, HCMOS integrated circuits [3-6]

The semiconductor material is subjected to various processes in which impurities and other material are added. Integrated circuits is electronic network which is fabricated on a single piece of semiconductor material. There are number of steps followed by designer such as: lithography, physical structure, CMOS fabrication sequence, design rules, advanced CMOS process and technical scaling to design a CMOS device. Lithography is the process used to transfer the electronics network patterns to every layer of IC. In next step we will do fabrication sequence. P-type silicon wafer is starting point of process. First step in CMOS fabrication is epitaxial growth. The epi layer is used as a base layer to design the digital devices. After that there is n-well formation. Active area is the planar area where CMOS transistors builds and a thin layer of SiO_2 is grown over and covered with silicon nitride. Number of steps as like : gate oxide growth, polysilicon deposition, PMOS formation, NMOS formation, annealing should be done to build an integrated circuit.

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As from the figure.1 it is clear the trend of downsizing of CMOS should not end. Early in 1970 CMOS is designed using Planar(2D) technology. But to follow the Gordons Moore's law downsizing and new technology are very important. Now Non-Planar technology is used to design CMOS integrated circuits. As well material are selected list of semiconductors. We cannot use all semiconductors, it depends upon the structure of the material that can we use it or not. Graphene and III-V/Ge are used at rich level in 3D technology. But III-V materials will not completely replace the Si-CMOS because of some feature of Switching from 2D technology to 3D technology increases performance and better speed with smaller area without scaling. The advantage of using three dimensional technique is not only to increase the CMOS density on a chip but also have other advantages, such as: mixed circuit technologies(e.g. digital and analog) , mixed process technologies(e.g. bipolar and CMOS) and combination of different semiconductor material [8]. In 3D integration packaging density varies from device to device, high or low. This chart shows range of 3D technology.

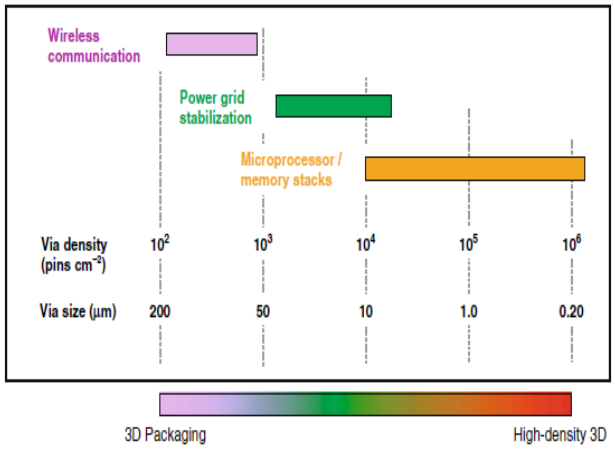

Fig.2. Chart showing range of 3D technology applications being implemented at IBM [2].

After CMOS the HCMOS(High-Speed CMOS or High Performance CMOS) was introduced. High-k CMOS are also a high performance CMOS. As the conventional CMOS face many challenges, such as: higher gate leakage current, source to drain leakage current, gate stack reliability and channel mobility degradation due to increasing electric field cause rising dynamic power dissipation(CV^2f) from non-scaled power supply voltage, band to band tunneling leakage at high body doping levels, device to device variation from random dopants fluctuations effects, and high source drain access resistance from source drain[3]. There are different advanced technologies used for annealing and surface cleaning. For advanced CMOS technologies the high-k dielectric material is used instead of using SiO_2.

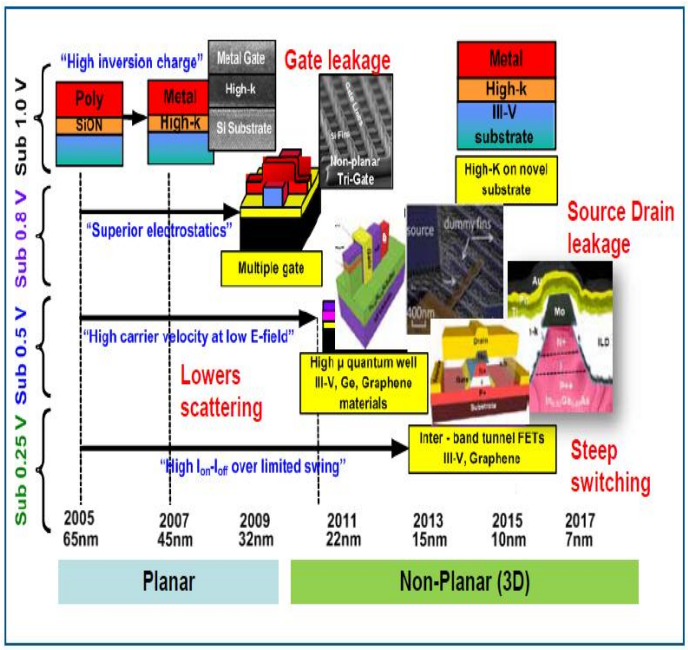

Fig.3. Trend in high performance (HP) CMOS transistor innovation. Different materials used (high-k dielectric, Ge, III-V) and the transistor (3D, tunnel FET) being implemented to improve rate of performance, density and power scaling [3].

Early researchers are researching for high-k dielectric material. They found out a material hafnium dioxide (HfO_2). HfO_2 due to .The advantage of using high-k material is to achieve same electrically oxide thickness with 5 times physically thicker hafnium oxide dielectric compared to silicon dioxide.

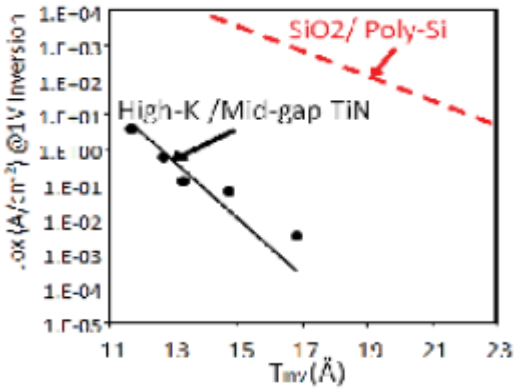

Fig.4. Significant reduction in gate leakage by replacing SiO_2 with high-k dielectric [3].

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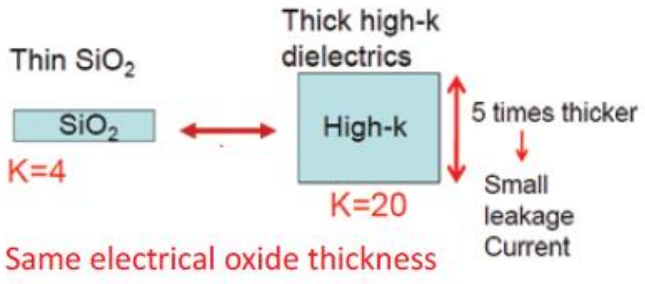


Fig.5. Same electrically oxide thickness is achieved with 5 times thicker physically thicker HfO_2(Hafnium dioxide) dielectric compared to SiO_2(Silicon dioxide) [3].

A. Power Density and Voltage scaling

As we knew the transistor density increased, almost doubles after every 18 months. The supply voltage has not decreased in that proportion. Question raise in our mind is, Why power increased. Reason behind this is increase in die size and fast frequency scaling. If V_{dd} has not scaled then energy scaled slowly. Different methods used to reduce energy are reducing waste and problem reformulation. Since transistor still leak when power is off. Leakage should minimized by using low leakage system on chip design techniques. Low leakage system contains following switches and cells: Power switch control signal, Embedded power switches and Row of standard cells[14].

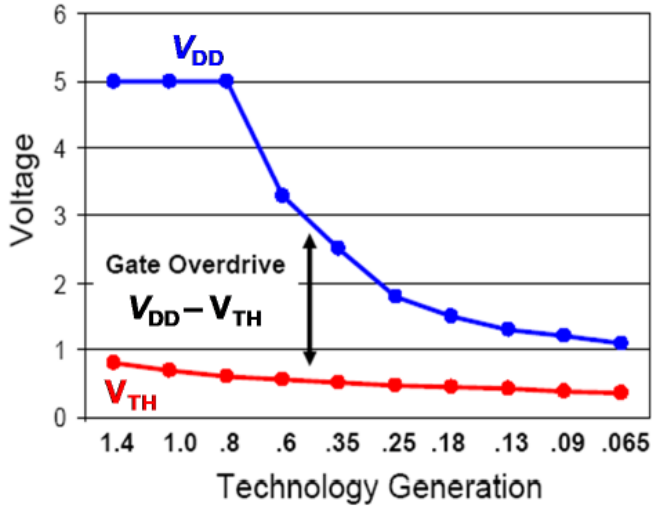


Fig.6. CMOS voltage scaling[9]

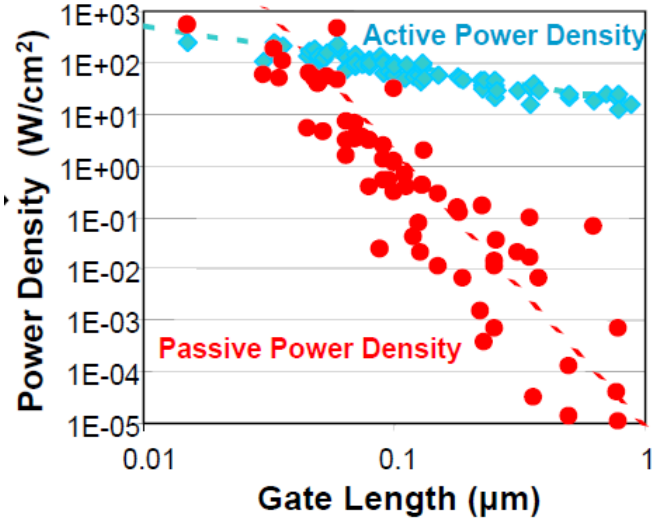
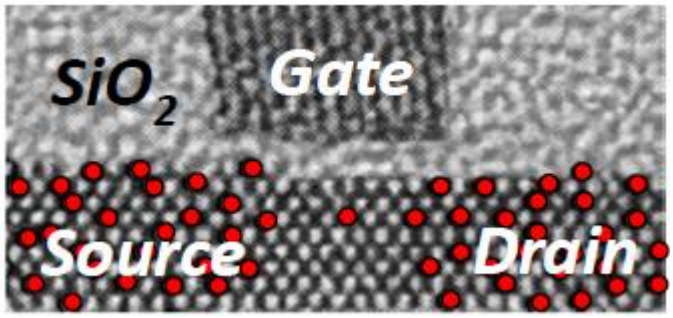


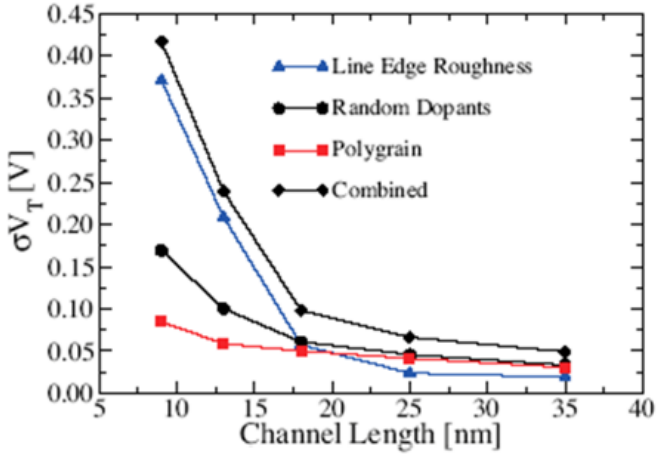
Fig.7. Power Density vs. Gate Length [10]

B. Random Dopant Flucuations

In nanoscale CMOS circuits the Random Dopant Fluctuation(RDF) cause variations in threshold voltage(V_t) in transistors[15]. Random variation in number and placement of dopant atoms cause random variations in transistor threshold voltage(V_{th}) is called random dopant effect[16]-[18].



(a)



(b)

Fig.8. (a)MOS transistor with dopant atoms[11] (b) Variations in threshold voltage with parameters[12]

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C. Segmented channel MOSFET

In segmented channel MOSFET channel region comprises stripes of equal width $\geq (L_g)$ isolated by Very Shallow Trench Isolation (VSTI). VSTI is much shallower than the STI between transistors. Deep Source/Drain regions and ground plane are not segmented. Gate control is enhanced by fringing the electric fields. The channel stripes can be elevated above the VSTI , or a High-k VSTI dielectric can be used , to further enhance the gate control. Segmented channel MOSFET has lower gate leakage due to reduced transverse electric field.

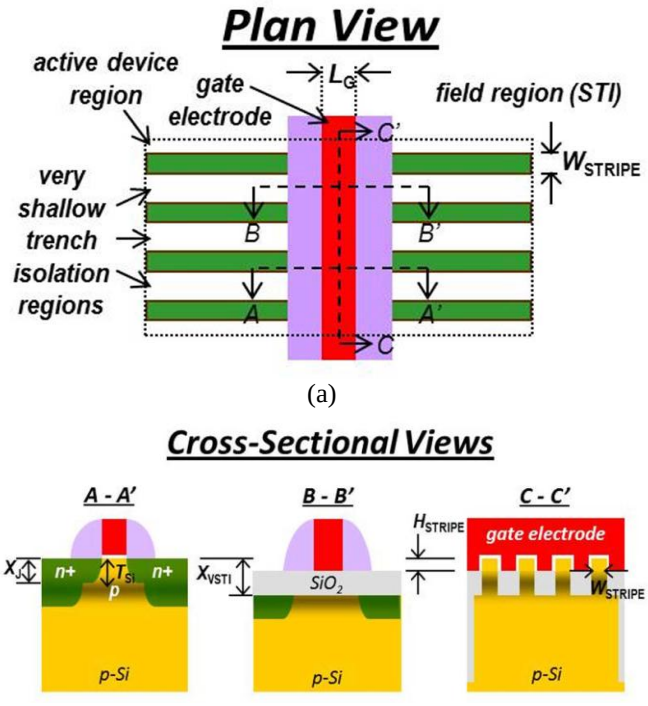

Fig.9. (a) Plain View [13] (b) Cross-Sectional View [13]

CONCLUSIONS

This paper examined the different CMOS technologies and their scaling. The scaling is priorities of industries because it reduces the size of computational devices. During 1970s the CMOS has very large in size as compared to today's technology. After few decades size is continuously scaled down. Since problems faced by designer to more and more narrowing the CMOS size using same technology, then new technology comes into market called 3D technology. Material researchers found new high-k dielectric material, which makes ease towards designing high performance CMOS.

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