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Fault Detection for ISCAS 89' S-27 Benchmark Circuit Using Low Power Lt-RTPG

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Abstract

In this project test patterns generated by the Low-transition random pattern generator (LT-RTPG) detect Easy-to-detect faults. This LT-RTPG's are normally used in Built In Self Tests (BIST). This project also presents a novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the Output sequence of a conventional LFSR. The proposed design, called Bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 Multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain Input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. The proposed LT-RTPG can significantly reduce switching activity during BIST. These techniques have a substantial effect on average and peak-power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS'89 S-27 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively.

Index Terms — Built-in self-test (BIST), linear feedback shift register (LFSR), low-power test, pseudorandom pattern generator

1. Introduction

The LT-RTPG reduces switching activity during BIST by reducing transitions at scan inputs during scan shift operations. An example LT-RTPG is shown in Fig. The LT-RTPG is comprised of an r-stage LFSR, a K-input AND gate, and a toggle flip-flop (T flip-flop). Hence, it can be implemented with very little hardware. Each of K inputs of the AND gate is connected to either a normal or an inverting output of the LFSR stages. If large K is used, large sets of neighbouring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in test sequence length. In this project, LT-RTPGs with only K=2 or 3 are used since a T- flip-flop holds previous values until the input of the T flip-flop is assigned a 1,the same value v, where v E{0,1} , is repeatedly scanned into the scan chain until the value at the output of the AND gate. Hence, adjacent scan flip-flops are assigned identical values in most test patterns and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations. The LT-RTPG can reduce heat dissipation during overall scan testing. This paper presents a new TPG, called the bit-swapping linear feedback shift register (BS-LFSR), that is based on a simple bit swapping technique applied to the output sequence of a conventional LFSR and designed using a conventional LFSR and a 2 × 1 multiplexer. The proposed BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT.

2. Proposed approach to Design the LT-RTPG:

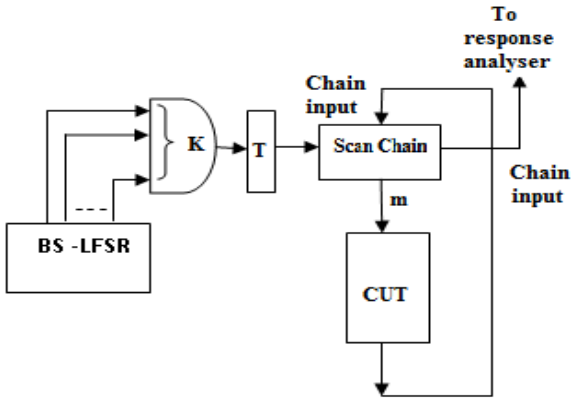

Fig: PROPOSED LT-RTPG

It has been observed that many faults that escape random patterns are highly correlated with each other and can be detected by continuously complementing values of a few inputs from a parent test vector. These observations are exploited and improve fault coverage for circuits that have large numbers of RPRFs. We have also observed that tests for faults that escape LT-RTPG test sequences share many common input assignments. This implies that RPRFs that escape LT-RTPG test sequences can be effectively detected by fixing selected inputs to binary values specified in deterministic test cubes for these RPRFs and applying random patterns to the rest of inputs. This technique is used in the 3-weight WRBIST to achieve high fault coverage for random pattern resistant circuits. The proposed LT-RTPG is as follows.

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3.Bit-swapping LFSR:

In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems. However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation.

Several techniques that have been developed to reduce the peak and average power dissipated during scan-based tests. A direct technique to reduce power consumption is by running the test at a slower frequency than that in normal mode. This technique of reducing power consumption, while easy to implement, significantly increases the test application time . Furthermore, it fails in reducing peak-power consumption since it is independent of clock frequency.

Another category of techniques used to reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scan chain- ordering techniques. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture).The design of low-transition test-pattern generators (TPGs) is one of the most common and efficient techniques for low-power tests. This project presents a new TPG, called the bit-swapping linear feedback shift register (BS-LFSR), that is based on a simple bit swapping technique applied to the output sequence of a conventional LFSR and designed using a conventional LFSR and a 2 × 1 multiplexer.

The introduced BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT.

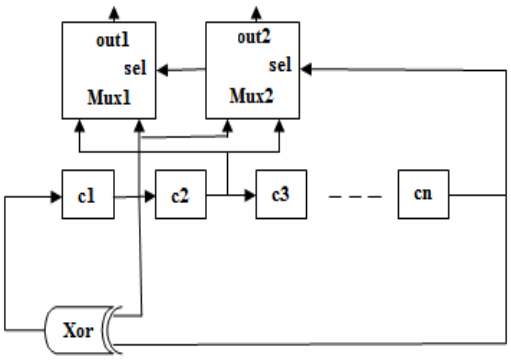


Fig : Bit-swapping LFSR

The introduced BS-LFSR for test-per-scan BISTs is based upon some new observations concerning the number of transitions produced at the output of an LFSR.

Definition: Two cells in an *n*-bit LFSR are considered to be adjacent if the output of one cell feeds the input of the second directly (i.e., without an intervening XOR gate).

Approach: Each cell in a maximal-length *n*-stage LFSR will produce a number of transitions equal to 2*n*-1 after going through a sequence of 2*n* clock cycles.

Proof: The sequence of 1s and 0s that is followed by one bit position of a maximal-length LFSR is commonly referred to as an *m*-sequence. Each bit within the LFSR will follow the same *m*-sequence with a one-time-step delay. The *m*-sequence generated by an LFSR of length *n* has a periodicity of 2^n - 1. It is a well-known standard property of an *m*-sequence of length *n* that the total number of runs of consecutive occurrences of the same binary digit. The beginning of each run is marked by a transition between 0 and 1; therefore, the total number of transitions for each stage of the LFSR is 2^n *-1*. This approach can be proved by using the toggle property of the XOR gates used in the feedback of the LFSR.

IMPORTANT PROPERTIES OF THE BS-LFSR:

There are some important features of the BS-LFSR that make it equivalent to a conventional LFSR. The most important properties of the BS-LFSR are the following.

1) The BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence,

the proposed design retains an important feature of any random TPG. Furthermore, the output of the multiplexer depends on three different cells of the LFSR, each of which contains a pseudorandom value. Hence, the expected value at the output can also be considered to be a pseudorandom value.

2) If the BS-LFSR is used to generate test patterns for either test per- clock BIST or for the primary inputs of a scan-based sequential circuit (assuming that they are directly accessible) as shown in Fig. 3, then consider the case that *c*1 will be swapped with *c*2 and *c*3 with *c*4, . . . , *cn*-2 with *cn*-1 according to the value of *cn* which is connected to the selection line of the multiplexers (see Fig. A). In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced by 25%.

4. S27 sequential circuit

Here S27 circuit is selected, which belongs to ISCAS 89' benchmark circuit family and It is a purely sequential circuit with four inputs. The circuit has been tested by using Built In-Self Test. Initially faults are inserted into the circuit, in the above circuit faults are inserted at a2,a9,a4 and a10 locations.

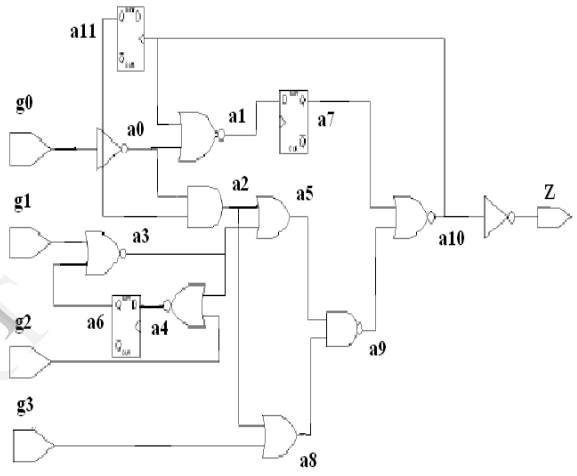
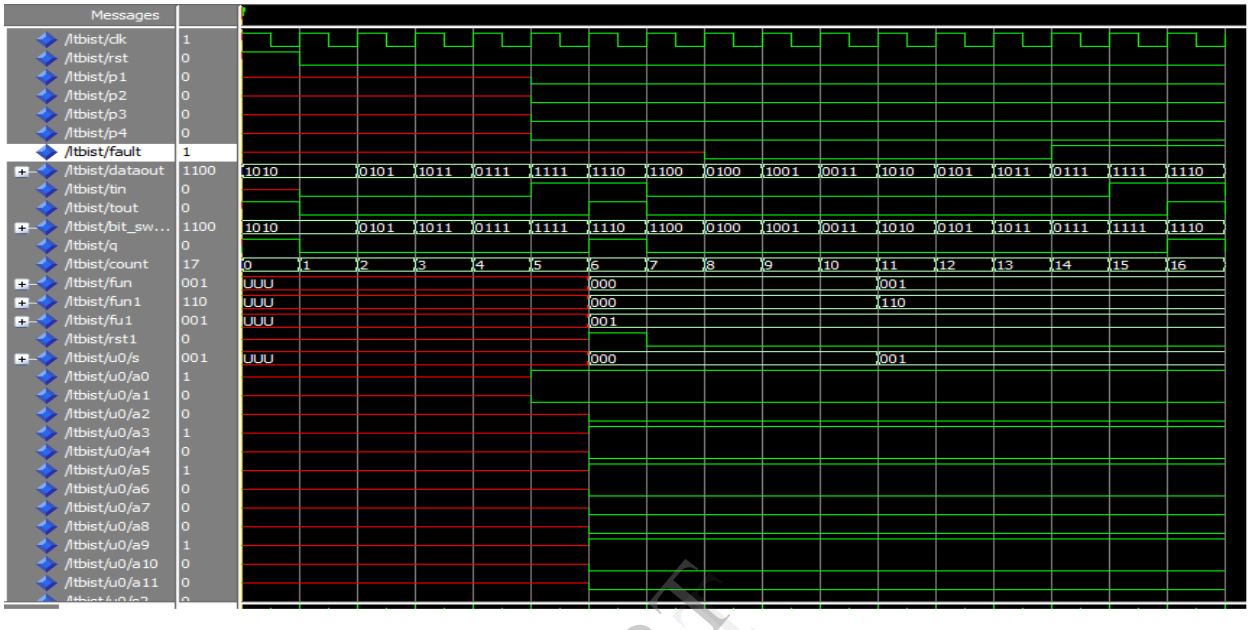


Fig : ISCAS 89'Benchmark S27 circuit

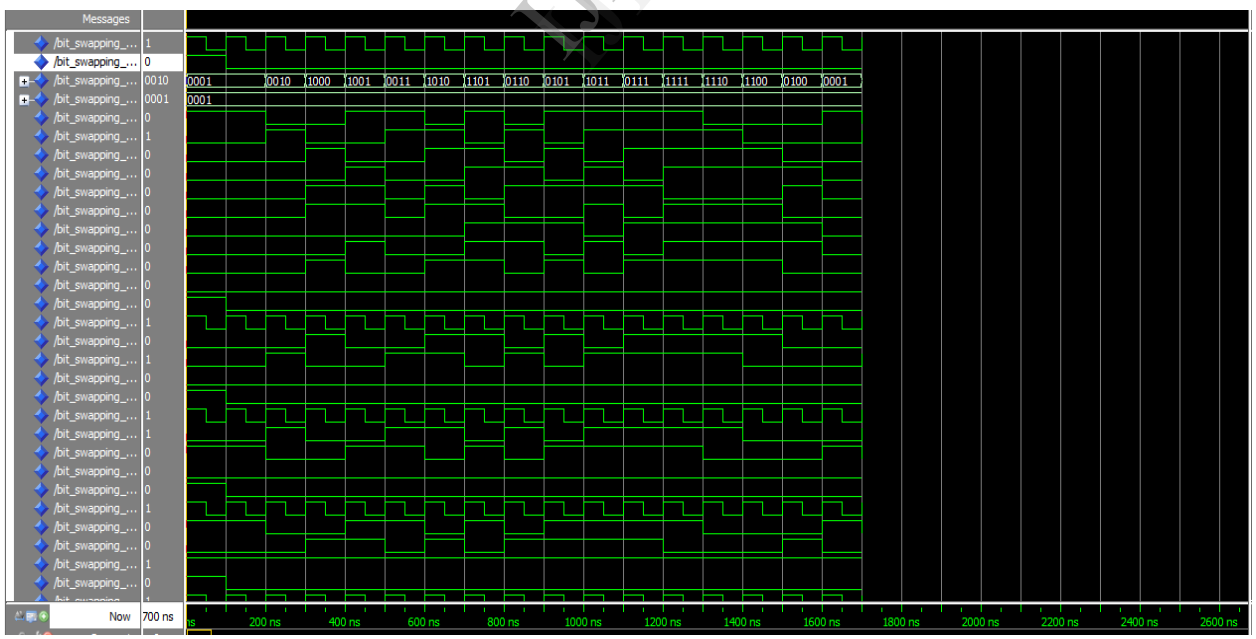
For each and every fault pseudorandom patterns are applied corresponding test vector will be taken for four faults four test vectors are taken. These vectors are divided into two sub groups for the reduction of transitions. As number of transitions are reduced the power consumption is reduced. if output value of faulty S27,and normal S27 circuits are different then fault has been covered.

5. Experimental results and comparison:

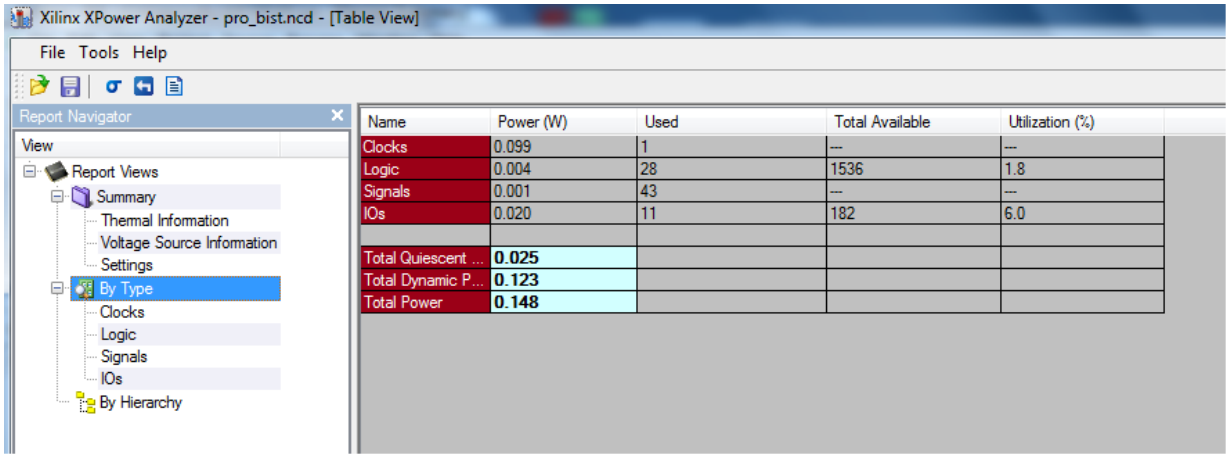
5.1 simulated waveform of fault coverage for S-27 circuit



5.2 simulated waveform of Bit-Swapping LFSR

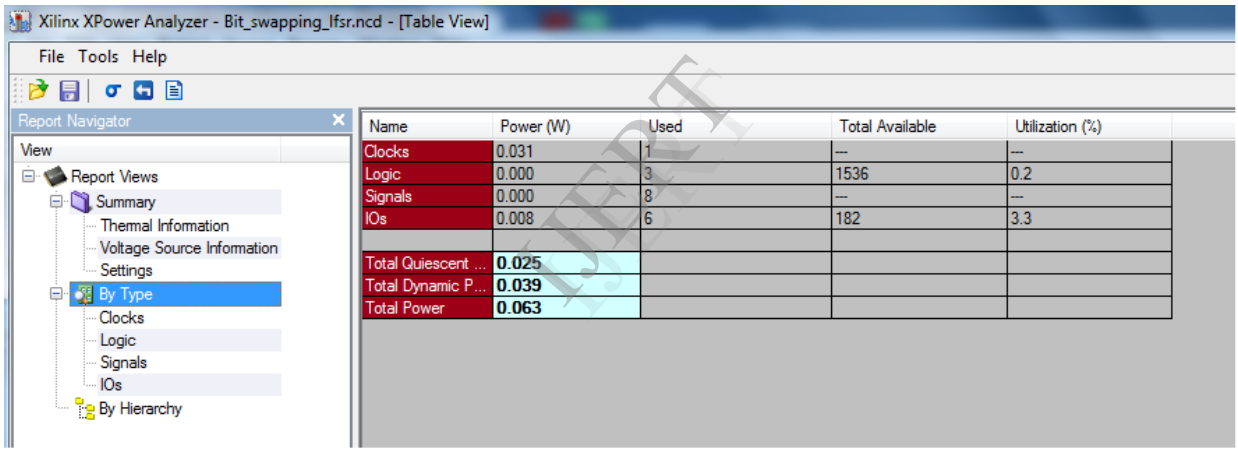


5.3 Power analysis report of LT-RTPG for S27 circuit:



Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.099	1	---	---
Logic	0.004	28	1536	1.8
Signals	0.001	43	---	---
IOs	0.020	11	182	6.0
Total Quiescent ...	**0.025**			
Total Dynamic P...	**0.123**			
Total Power	**0.148**			

5.4 Power analysis report for Bit-Swapping LFSR:



Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.031	1	---	---
Logic	0.000	3	1536	0.2
Signals	0.000	8	---	---
IOs	0.008	6	182	3.3
Total Quiescent ...	**0.025**			
Total Dynamic P...	**0.039**			
Total Power	**0.063**			

5.5 Synthesis report for LT-RTPG:

TT Project Status			
Project File:	tt.ise	**Current State:**	Placed and Routed
Module Name:	ltbist	**• Errors:**	No Errors
Target Device:	xc2s600e-7fg456	**• Warnings:**	16 Warnings
Product Version:	ISE, 8.1i	**• Updated:**	Sun Jan 6 11:21:47 2013

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	41	13,824	1%	
Number of 4 input LUTs	22	13,824	1%	
Logic Distribution				
Number of occupied Slices	32	6,912	1%	
Number of Slices containing only related logic	32	32	100%	
Number of Slices containing unrelated logic	0	32	0%	
Total Number 4 input LUTs	53	13,824	1%	
Number used as logic	22			
Number used as a route-thru	31			
Number of bonded IOBs	6	325	1%	
IOB Flip Flops	4			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	678			
Additional JTAG gate count for IOBs	336			

5. Conclusion:

A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most tested benchmark circuits.

Acknowledgment

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