Five Level Inverter Capable of Power Factor Correction with DC Link Switches

Ajin. K.V, K. Suryasen, K.V Devadas
Department of Electrical and Electronics Engineering
KVG College of Engineering, Sullia, D.K-574 327
Karnataka,India

***Abstract*--Multilevel inverters are widely used in electric high power application. They offer less harmonics and possibility of working at lower switching frequencies. The device voltage rating can be made much lower than that of a two-level inverter for the same output voltage. Therefore in case of multilevel inverters switching losses can be significantly reduced and system efficiency can be increased. This paper proposes a Five Level Inverter based on H Bridge with four DC Link switches .In this paper Phase Opposition Disposition (POD) modulation method which requires only single carrier signals is described. In order to increase the number of voltage level, the proposed topology requires minimum number of components. The Five Level Inverter is verified through the simulation and hardware.**

I .INTRODUCTION

Conventional two-level inverters, are mostly used today to generate an AC voltage from an DC voltage. The two-level inverter can only create two different output voltages for the load, Vdc/2 or –Vdc/2 (when the inverter is fed with Vdc). To build up an AC output voltage these two voltages are usually switched with PWM. Though this method is effective, it creates harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). This may not always be a problem but for some applications there may be a need for low distortion in the output voltage. The concepts of Multilevel Inverters (MLI) do not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

Industries have increased the use of multilevel inverters for high-voltage applications, such as static var compensators, active power filters, and adjustable-speed drives (ASDs) for medium-voltage induction motors. ASDs have been used in several industry sectors such as the petrochemical, mining, water/waste, pulp and paper, cement, chemical, power generation, metal, and marine sectors. They are employed in equipment such as pumps, fans, compressors, blowers, extruders, conveyors, crushers and mills, rolling mills, mixers, propulsion, test beds, synchronous condensers, gas turbine starts, hoists, and winders.

Several MLI topologies have been suggested so far and they can be mainly classified as three types. The Fig. 1.1 shows the three types, Neutral point clamped (NPC) Flying capacitor (FC), and
Cascaded type

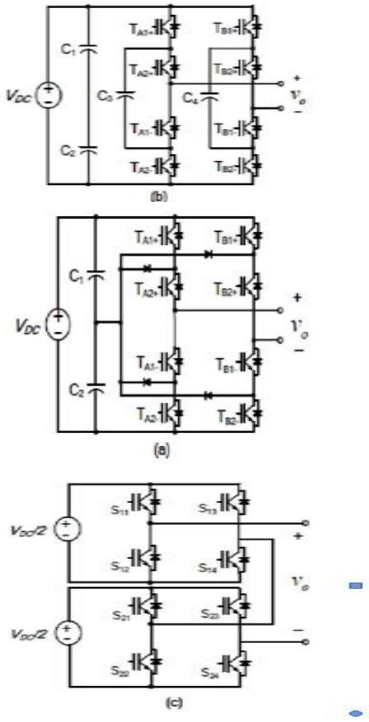

Fig. 1 : Topologies of multi-level inverters
(a) Neutral point clamped (NPC) type. (b) Flying capacitor (FC) type. (c) Cascade type.

The main advantages of the NPC inverter is its simplicity, the use of a small number of semiconductor devices, and the requirement of only one dc voltage source to supply the three legs of the inverter. However, the cost of the semiconductor devices increases exponentially with higher voltage ratings. The cost of cascaded topology is not necessarily higher than the NPC inverter, and cascaded topologies may present low distortion output voltage and

higher efficiency. In FC inverter the capacitor transfers the limited amount of voltage to electrical devices. Drawback of FC inverter is output is half of the input DC voltage.

II. PROPOSED FIVE LEVEL INVERTER

The proposed five level inverter system is more reliable and cost competitive than the conventional two level and multi level inverters. It is due to the fact that the number of devices of the proposed system is fewer than the two level and conventional multilevel inverters. The switches in the H Bridge are operating at a lower frequency. Therefore the switching losses are almost negligible. Only one carrier signal is used to generate eight PWM signals in the proposed PWM method. Thus it is quite simple. In addition, the switching sequence considering the voltage balance of dc-link was proposed.

A. Topology of Five-Level Inverter

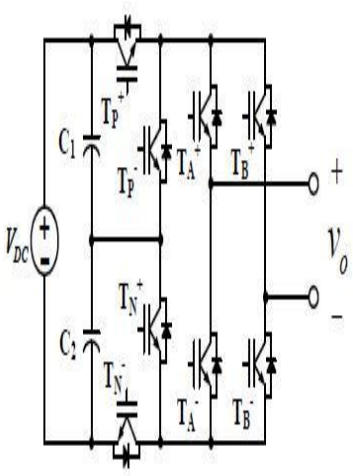

Fig. 2: Proposed single phase five-level inverter topology.

As shown in Fig. 2.12, the proposed MLI is composed of two dc-link capacitors (C1, C2) and four switching devices (TA+,TA-, TB+, TB-) comprising a H-bridge, and four active switches (TP+, TP-, TN+, TN -) located between dc-link and H-bridge. The voltage across the switching devices in the dc-link (TP+, TP-,TN+, TN-) is VDC/2 and operated at a switching frequency. Whereas, voltage across the switching devices in the H-bridge (TA+, TA-, TB+, TB-) is VDC and the switches (TA+, TA-, TB+, TB-) are switched at a frequency of the fundamental component of the output voltage (e.g. 50 or 60 Hz). Thus, the dc-link switches (TP+, TP-, TN+, TN-) and the H bridge switches (TA+, TA-, TB+, TB-) can be strategically selected based on the rated power of the inverter system in order to reduce system cost and increase efficiency. Table1 shows the output voltage according to the switching states.

Table 1: Output voltage of proposed five level inverter according to the switching states

Output voltage(Vo)	Switching condition					
	TP+	TP-	TN+	TN-	TA+,TB-	TA-,TB+
Vdc	ON	OFF	OFF	ON	ON	OFF
Vdc/2	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	ON	OFF
-Vdc/2	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
-Vdc	ON	OFF	OFF	ON	OFF	ON

The output voltage of the proposed MLI has five levels (VDC, VDC/2, 0, - VDC/2, -VDC) according to the switching states of the inverter. There are four operation modes depending on the instantaneous value of the reference voltage, Vref and the maximum value of the carrier signal, Vc.

B. Operating Modes and Proposed PWM Strategy

Table 2: Operating modes of the proposed Five Level Inverter

Operating mode	Reference voltage range	Output voltage
Mode 1	Vc≤Vref<2Vc	Vdc/2 or Vdc
Mode 2	0≤Vref<Vc	0 or Vdc
Mode 3	-Vc≤Vref<0	-Vdc/2 or 0
Mode 4	-2Vc≤Vref<-Vc	-Vdc or –Vdc/2

There are four operation modes depending on the instantaneous value of the reference voltage, Vref and the maximum value of the carrier signal, Vc. If the reference signal is positive, then the switch pair (TA+, TB-) are turned on, and if it is negative, then the switch pair (TA-, TB+) are turned on. Thus the switches composing the H bridge inverter turned on and turned off once during the period of the reference signal. The voltage across the switch at blocking state is VDC. The switches (TP -, TN +) are operated complementally to the switches (TP+, TN-). The generation of the PWM signal for dc-link switches (TP+, TN-) can be explained as follows.

· Mode 1: a signal subtracted from the reference signal by Vc is compared with the carrier signal. If *vref* -Vc> *vcarrier*, then all switches TP+ and TN- are turned on. If *vref* -Vc< *vcarrier*, then the switch TP+ or TN- is turned off alternately.

· Mode 2: the reference signal is directly compared with a carrier signal. If *vref* > *vcarrier*, then the switch TP+ or TN- is
turned on alternately. If *vref* < *vcarrier*, then all switches TP+ and TN- are turned off.

· Mode 3: *-vref* is directly compared with a carrier signal.If *-vref* > *vcarrier*, then the switch TP+ or TN- is turned on alternately. If *-vref* < *vcarrier*, then all switches TP+ and TN- are turned off.

Mode 4: a signal subtracted from *-vref* by Vc is compared with the carrier signal. If If *-vref* by Vc> *Vcarrier*, then all switches TP+ and TN - are turned on. If *-vref* -Vc< *vcarrier*, then the switch TP + or TN - is turned off alternately.

In case of the N-level NPC type multi-level inverter, N-1 triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range +VDC to -VDC. A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. Here Phase Opposition Disposition (POD) method is used. In this method the carriers above zero voltage are 180 degree out of phase with those below zero voltage. Only one carrier signal is used to generate eight PWM signals in the proposed PWM method. Thus it is quite simple.

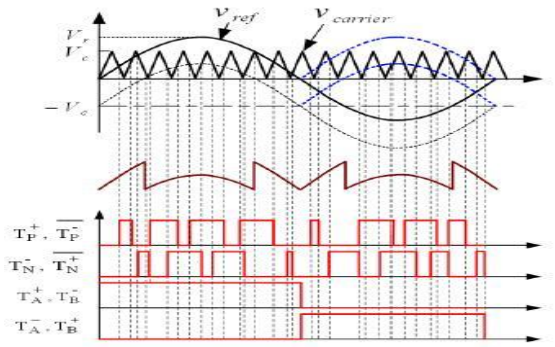

Fig. 3: PWM strategy based on POD with single carrier signal

III. SCOPE FOR FUTURE WORK

The Five level inverter can be extended to Seven or Nine Level inverter. In case of 9-level or 7-level inverter, the proposed inverter requires less active devices than 9-level or 7-level cascaded H bridge MLI. Therefore, number of switching devices in the higher Level Inverter can be reduced significantly as the number of voltage level increases.

IV. SIMULATION RESULTS

The proposed Five Level Inverter is verified through the simulation in MATLAB/SIMULINK .The H bridge switches are operates at a fundamental frequency of 50 Hz. The circuit was simulated with RL load. Figure shows the output waveform of the Five Level Inverter. The Figure shows the output waveforms with power factor correction.

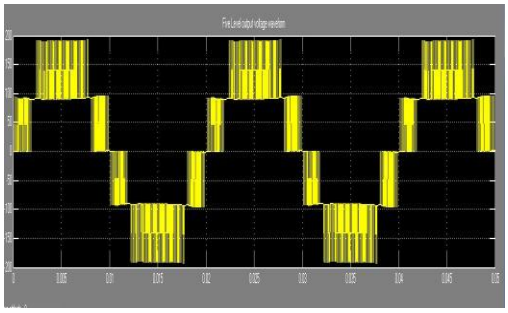

Fig .4: Output voltage of the Five Level Inverter

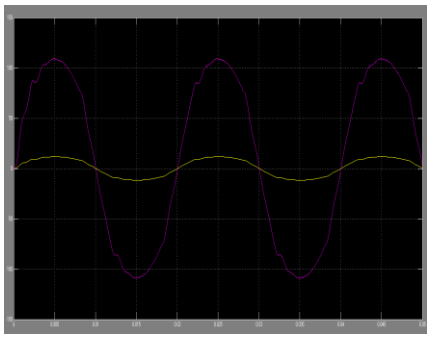

Fig .5 : Output voltage and current waveforms after power factor correction

V. CONCLUSIONS

Number of devices of the proposed five-level inverter is fewer than that of the conventional *multi-level inverters. Therefore, the proposed system is more reliable and cost effective* than the conventional two-level and multilevel inverters. The four switches in the H-bridge are switched at a low frequency. Therefore, switching loss of the four switches is almost negligible. Only one carrier signal is required to generate the PWM signals for four switching devices. Only one carrier signal is used to generate the PWM signals for four DC link switches. This made controller design implementation simple and cost effective.

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