Five Level Inverter Fed Induction Motor Drive Using CBSVPWM

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ABSTRACT:

Variable speed induction motor drives are widely spread in electromechanical systems for a large spectrum of industrial applications. When high dynamic performance and high precision control in a wide speed range are required, vector control based induction motor drive can be used with speed. On the other hand, for medium and low performance applications, sensor-less control of induction motor is becoming an industrial standard. The recent advancement in power electronics has been initiated to improve the level of inverter rather than increasing the filter size. Using multilevel inverters, it is better to reduce the harmonics. In this paper, space vector modulation technique that uses to reduce the harmonics. For redundant switching, a space vector modulation is required due to vector selection in dq stationary reference frame. The space vector modulation technique is used for multilevel inverter system. However, space vector modulation has more advantages due to low harmonic production

INTRODUCTION:

An induction motor being rugged, reliable, and relatively inexpensive makes it more preferable in most of the industrial drives. They are mainly used for constant speed applications because of unavailability of the variable-frequency supply voltage [1]. But many applications are in need of variable speed operations. In early times, mechanical gear systems were used to obtain variable speed. Recently, power electronics and control systems have matured to allow these components to be used for motor control in place of mechanical gears. These electronics not only control the motor's speed, but can improve the motor's dynamic and steady state characteristics. Adjustable speed ac machine system is equipped with an adjustable frequency drive that is a power electronic device for speed control of an electric machine. It controls the speed of the electric machine by converting the fixed voltage and frequency to adjustable values on the machine side. High power induction motor drives using classical three - phase converters have the disadvantages of poor voltage and current qualities. To improve these values, the switching frequency has to be raised which causes additional switching losses. Another

possibility is to put a motor input filter between the converter and motor, which causes additional weight. The diode clamp method can be applied to higher level converters. As the number of level increases, the synthesized output waveform adds more steps, producing a staircase waveform. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels. In this paper, a three-phase diode clamped multilevel inverter fed induction motor is described. The diode clamped inverter provides multiple voltage levels from a five level unidirectional voltage balancing method of diode clamped inverter [2]. The voltage across the switches has only half of the dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device [3]. The proposed inverter can reduce the harmonic contents by using carrier based SVPWM technique. It generates motor currents of high quality. V/f is an efficient method for speed control in open loop. In this scheme, the speed of induction machine is controlled by the adjustable magnitude of stator voltages and its frequency in such a way that the air gap flux is always maintained at the desired value at the steady state. Here the speed of an induction motor is precisely controlled by using five level diode clamped multilevel inverter

MULTILEVEL INVERTERS:

The concept of utilizing multiple small voltage levels to perform power conversion was patented by an MIT researcher over twenty years ago [1,2]. Advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability. The main disadvantages of this technique are that a larger number of switching semiconductors are required for lower-voltage systems and the small voltage steps must be supplied on the dc side either by a capacitor bank or isolated voltage sources. The first topology introduced was the series H-bridge design [1]. This was followed by the diodeclamped [2-4] converter which utilized a bank of series capacitors. A later invention [5] detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors

[6]. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged [7] some involving cascading the fundamental topologies [8-12]. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

Several different five-level multilevel carrier-based PWM techniques have been extended by previous authors as a means for controlling the active devices in a multilevel converter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. The three major carrier-based techniques used in a conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third harmonic injection PWM (THPWM), and space vector PWM (SVM). Carrier based SVPWM is a efficient and effective method in industrial applications.

CARRIER BASED SVPWM:

Carrier based SVPWM allow fast and efficient implementation of SVPWM without sector determination. The technique is based on the duty ratio profiles that SVPWM exhibits. By comparing the duty ratio profile with a higher frequency triangular carrier the pulses can be generated, based on the same arguments as the sinusoidal pulse width modulation [10].

The standard topology of a 3-phase VSI is shown in Fig.2 and consists of three phase legs with two switches per leg, arranged so that each phase output can be connected to either the upper or the lower DC bus as desired. In Fig. 1, the eight available different switching vectors of the inverter are depicted with the space vector concept. The switching state "1" means the firing for the upper device of one arm and the pole voltage (V_{ao}, V_{bo}, V_{co}) will have half of the DC-link voltage value[7].
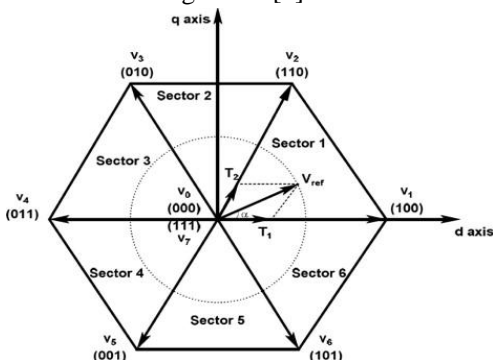

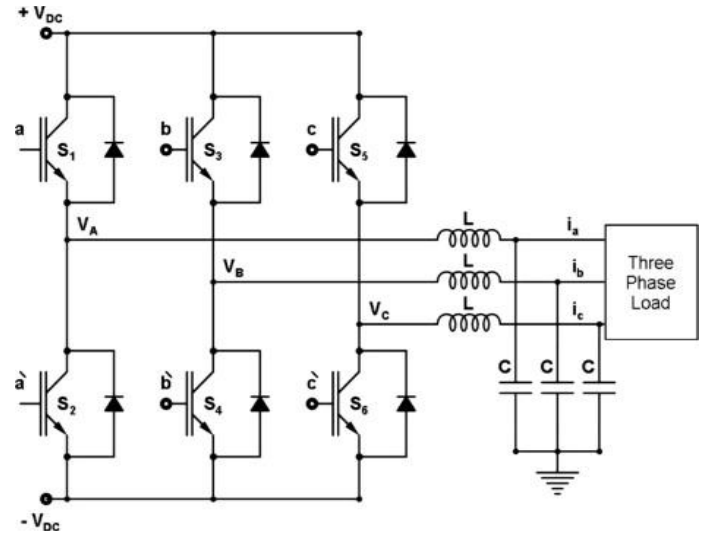Fig.1 Space vector diagram of the available switching vectors

Fig.2 Three-phase PWM inverter

Note that the switching states of each arm should be combined with each other to compose the required three-phase output voltage. Because each pole voltage has only two levels according to the related switching state, the time duration in which the different voltages are maintained is definitely related to the voltage modulation task. Therefore, the modulation task can be greatly simplified by considering the relation between the time duration and the output voltage[10]. We now focus on the effective voltage that makes an actual power flow between inverter and load. Fig.3 shows the switching states of sector 1 at different times during two sampling intervals. T_S denotes the sampling time and T_{eff} denotes the time duration in which the different voltage is maintained. T_{eff} is called the "effective time". For the purpose of explanation, an imaginary time value will be introduced as follows

$$Txs = \frac{Ts}{Vdc}Vxs* ,(x=a,b,c)$$

$V_{as}*$, $V_{bs}*$ and $V_{cs}*$ are the A-phase, B-phase, and C-phase reference voltages, respectively. This switching time could be negative in the case where negative phase voltage is commanded. Therefore, this time is called the "imaginary switching time".

Now, the effective time can be defined as the time duration between the minimum and the maximum value of three imaginary times, as given by

$T_{eff} = T_{max} - T_{min}$

Where $T_{min} = min(T_{as}, T_{bs}, T_{cs})$

$T_{max} = max (T_{as}, T_{bs}, T_{cs})$

When the actual gating signals for power devices are generated in the PWM algorithm, there is one degree of freedom by which the effective time can be relocated anywhere within the sampling interval.
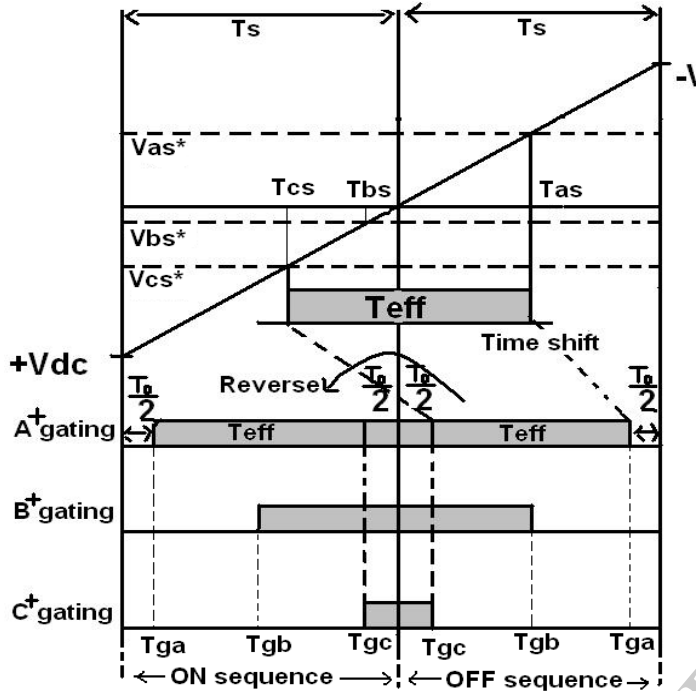

Fig.3 Actual gating time generation for continuous SVM

Therefore, a time-shifting operation will be applied to the imaginary switching times to generate the actual gating times (T_{ga},T_{gb},T_{gc}) for each inverter arm, as shown in Fig. 4. This task is accomplished by adding the same value to the imaginary times as follows:

$$T_{ga}=T_{as}+T_{offset}$$

$$T_{gb}=T_{bs}+T_{offset}$$

$$T_{gc}=T_{cs}+T_{offset}$$

Where T_{offset} is the 'offset time'

This gating time determination task is only performed for the sampling interval in which all of the switching states of each arm go to 0 from 1. This interval is called the "OFF sequence". In the other sequence, it is called the "ON sequence." In order to generate a symmetrical switching pulse pattern within two sampling intervals, the actual switching time will be replaced by the subtraction value, with sampling time as follows:
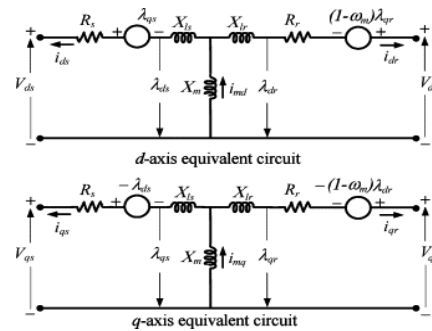
$$T_{ga}=T_s-T_{ga}$$

$$T_{gb}=T_s-T_{gb}$$

$$T_{gc}=T_s-T_{gc}$$

MODELLING OF INDUCTION MOTOR

In the control of any power electronics drive system(say a motor), to start with a mathematical model of the plant is required. This mathematical model is required further to design any type of controller to control the process of the plant. The induction motor model is established using a rotating (*d*, *q*) field reference (without saturation) concept. The power circuit of the 3-φ induction motor is shown in the Fig. 1. The equivalent circuit used for obtaining the mathematical model of the induction motor is shown in the Fig. 2. An induction motor model is then used to predict the voltage required to drive the flux and torque to the demanded values within a fixed time period[9]. This calculated voltage is then synthesized using the space vector modulation. The stator & rotor voltage equations are given by

$$u_d = R_1 i_d + \frac{d\psi_d}{dt} - \omega_1\psi_q$$

$$u_q = R_1 i_q + \frac{d\psi_q}{dt} - \omega_1\psi_d$$

$$u_{dr} = R_2 i_{dr} + \frac{d\psi_{dr}}{dt} - (\omega_1-\omega)\psi_{qr}$$

$$u_{qr} = R_2 i_{qr} + \frac{d\psi_{qr}}{dt} - (\omega_1-\omega)\psi_{dr}$$

Fig.4 Equivalent circuit of induction motor in *d* -*q* fram

where u_{sd} and u_{sq}, u_{rd} and u_{rq} are the direct axes & quadrature axes stator and rotor voltages. The squirrel-cage induction motor considered for the simulation study in this paper, has the *d* and *q*-axis components of the rotor voltage zero.

By superposition, i.e., adding the torques acting on the *d*-axis and the *q*-axis of the rotor windings, the instantaneous torque produced in the electromechanical interaction is given by

$$T_e = \frac{3}{2}\left(\frac{P}{2}\right)\frac{L_m}{L_r}\left(i_{qs}\lambda_{dr} - i_{ds}\lambda_{qr}\right).$$

SIMULATION RESULTS:

In this paper, five level CBSVPWM inverters employed to control the induction motor. The magnetizing flux linkage and the electromagnetic torque can be controlled by selecting optimum inverter switching modes. This selection is made to restrict the flux and torque errors within the corresponding flux and torque hysteresis bands and to achieve fast torque response, low inverter switching frequency, and low harmonic losses. MATLAB/SIMULINK model for five level inverter is shown in Fig 5.
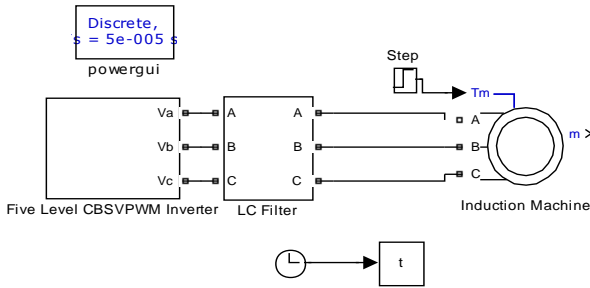

Fig.5.Simulink model for three phase five level inverter

Phase voltage, line current, Torque and speed responses of the two level inverter are shown in Figure.6-10.
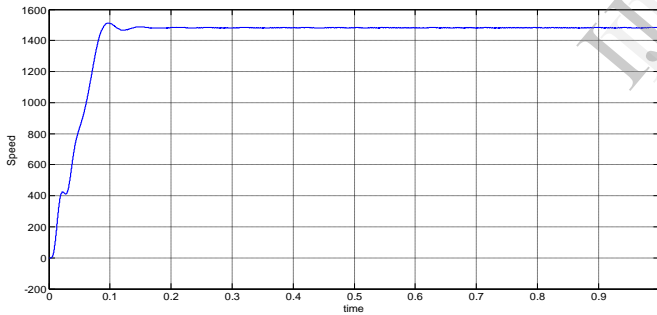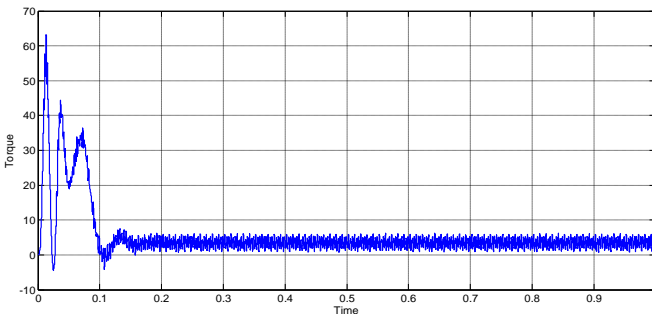

Fig.6.Output Speed of a five level inverter

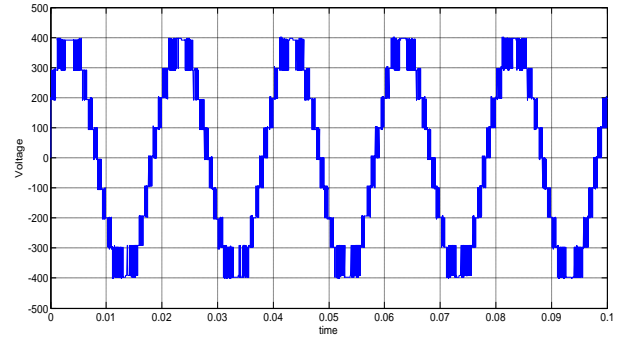Fig7. Output Torque of a five level inverter

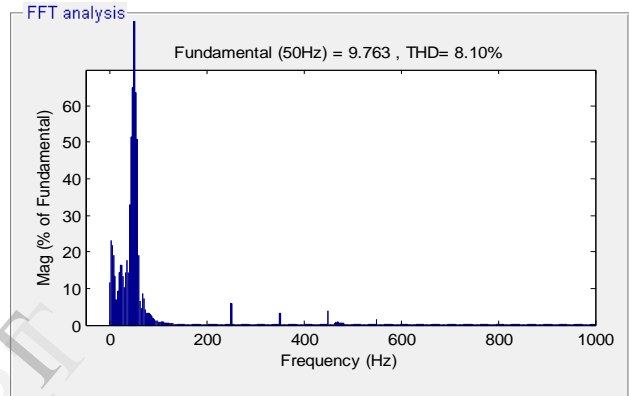Fig.8.Output Line Voltage of a five level inverter

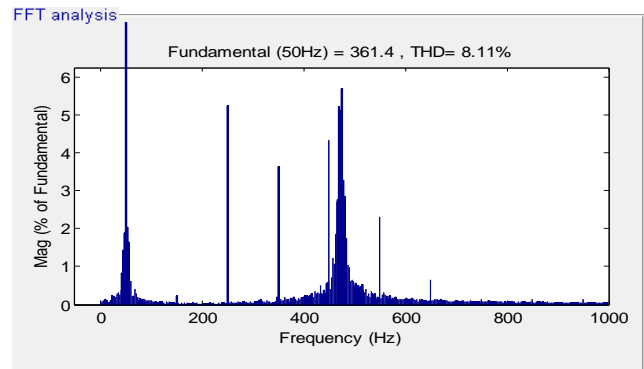Fig.9. Determination of THD of line current of five level inverter

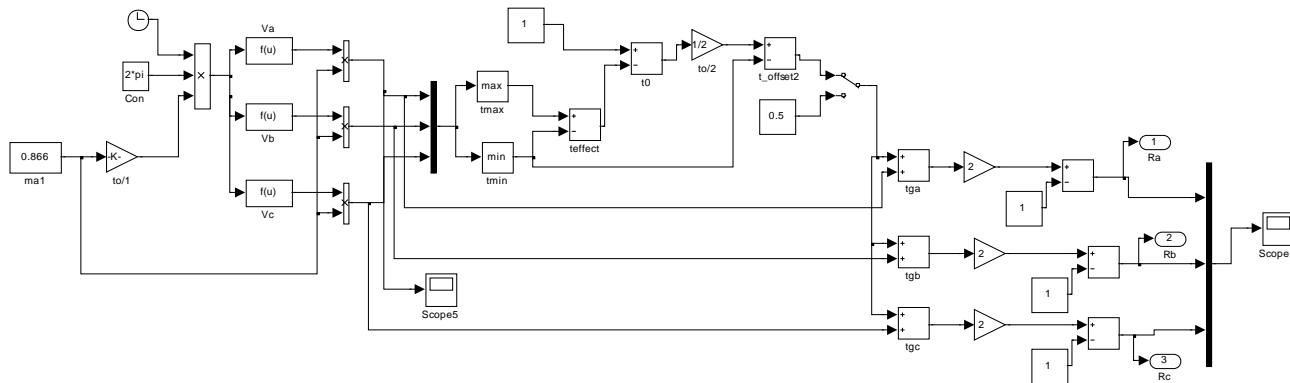Fig.10. Determination of THD of line voltage of five level inverter

Fig. 11 SIMULINK model for generating reference sinusoidal waves in SBSVPWM.

CONCLUSIONS:

In this paper, simulation analyses concerning the applications of CBSVPWM control strategy on the five level inverters fed Induction Motor are presented. From this analysis we can conclude that multilevel inverter can eliminate the harmonics produced by the normal inverter. From the simulation results obtained we can say that the total harmonic distortion is reduced by increasing the number of levels in the output voltage. Implementation of carrier based space vector pulse width modulation technique to generate gating pulses to the multi level inverter is easy when compared to normal SVPWM.

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