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FPGA Based Design of Band Stop IIR Filter using Multiplier-less Technique

Nirbhay Kumar Singh
ME student, ECE
NITTTR, Chandigarh-India

Amit Kumar Rana
ME student, ECE
NITTTR, Chandigarh-India

***Abstract*—In this current scenario, the demand of digital communication system is on peak, where Digital filter play an essential role. Digital filters [2] are mainly known to provided very minimum or ideally zero attenuation. In this paper, a recent technology FPGA based band stop infinite impulse response (IIR) with the implementation of a 16 tap multiplier less for digital signal processing applications because signals are subject to noise interference, hence filtering techniques are employed to remove noise from signals. The design of this IIR filter [1] on a field-programmable-gate-array(FPGA) using Spartan 3E xc3s1200efg320-5, and Virtex4, xc4vfx12sf363-12 chips from Xilinx Inc [3]. The Hardware Description Language (VHDL) is used for designing this IIR filter. The main aim of this paper is to give a comparison between Spartan 3E and Virtex4 on the basis of hardware utilization by a low-pass IIR filter. Here, the IIR filter is implemented using the Butterworth deign method as it meets the specifications with less complexity. Canonical Signed Digit (CSD) and Factored-Canonical Signed Digit (FCSD) representations are used to represent the filter coefficients and it is observed that the IIR filter with FCSD [5] representation is 53.426% faster than the Spartan3E chip for the given specifications.**

***Keywords*—**IIR filter, FPGA, VHDL, Butterworth, CSD, FCSD

I. INTRODUCTION

An IIR filter is commonly referred to as a recursive filter. There is a feedback loop that connects the output to the input in a recursive manner. In order to implement this filter [4], it is necessary to have knowledge of past, present, and future samples of the input, along with past values of the output. The realization [6] of a filter requires three essential factors: computational complexity [7], memory needs, and the implications of finite world length in the computations. There are three types of realization structures: direct form, parallel form, and cascade form.

The direct form structure consists of two types: direct form - I and direct form -II. The structure exhibits several forms of design. By carefully choosing the appropriate structure, it is possible to decrease computing complexity. The Direct form -II structure [8] is utilized in this paper.

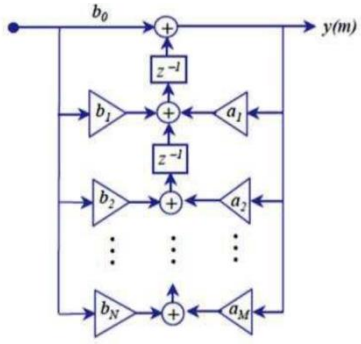

Fig.1.Realization of IIR [1]

The primary attributes of IIR filters consist of a low filter order [9], non-linear phase, and susceptibility to instability. The Butterworth IIR filter has a slower rate of attenuation, but its phase response is more linear when compared to Chebyshev-I & II and Elliptical filters [10]. The equation that describes the magnitude response of a Butterworth filter is as follows:

$$|H(j\Omega)| = \frac{A}{\sqrt{1 + (\Omega/\Omega c)^{2N}}} \quad (1)$$

In the context of filtering, the sign A represents the filter gain the symbol N represents the order of the filter, and the symbol Ωc represents the cut-off frequency for 3dB [11]

II. MULTIPLIER-LESS TECHNIQUES:

The "multiplier-less technique" in the context of digital signal processing (DSP) refers to methodologies or algorithms used to perform mathematical operations, such as multiplication or division, without explicitly using dedicated multiplication hardware or functional blocks [12]. Instead, it involves employing alternative techniques to achieve the same computational results with reduced hardware complexity and lower power consumption.

These techniques are particularly relevant in scenarios where hardware resources are limited or when optimizing [13] digital signal processing algorithms for implementation in resource-constrained environments, such as embedded systems, mobile devices, or specialized hardware like field-programmable gate arrays (FPGAs) [14]. Several

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approaches fall under the umbrella of multiplier-less techniques:

1. Shift-and-Add (Multiply-Accumulate - MAC):
Utilizes shift operations and additions to approximate multiplication. For example, binary shift operations can emulate multiplication by powers of two, and a sequence of additions can emulate partial products.
2. Look-Up Tables (LUTs) and Approximations: Pre-computed tables or approximations of multiplication factors stored in memory can be used to perform multiplication through table look-ups and additions.
3. Constant Coefficient Multipliers: Algorithms [15] or techniques specifically tailored for constant coefficients or common multiplication factors can reduce the need for complex multiplication operations.
4. Factoring and Reordering Operations**:** Rearranging equations or reordering mathematical operations to minimize the number of multiplications required. Techniques like distributed arithmetic fall into this category.
5. Addition-Subtraction Networks: Utilizes sequences of additions and subtractions [26] to approximate multiplication operations.
6. Algorithmic and Numerical Optimization: Optimization techniques specific to certain algorithms, such as those in digital filters or transforms, to reduce the number of multiplications or to simplify arithmetic operations.
These techniques are often employed in digital signal processing applications, including audio and video processing, image processing, communications [16], and more. They allow for efficient utilization of hardware resources by reducing the reliance on dedicated and power-hungry multiplication units, leading to more resource-efficient implementations without sacrificing computational accuracy or performance. However, they may introduce trade-offs[17] in terms of precision, accuracy, or increased computational complexity in certain cases. The choice of multiplier-less techniques depends on the specific application requirements and hardware constraints.

III. DIGITAL IIR FILTER

The choice between IIR and FIR (Finite Impulse Response) filters depends on the specific application, as both have their own advantages and trade-offs. IIR filters are often favored for applications where computational resources are limited, but they may exhibit more phase distortion than FIR filters. Always choose the type of filter that best suits the requirements of your particular application [20]

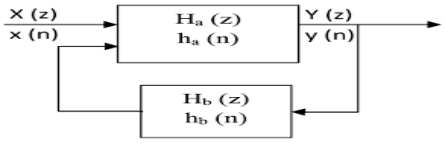

Fig.2. Basic block diagram of Digital IIR filter

Factored-Canonical Signed Digit (FCSD) representation is a modified form of Canonical Signed Digit (CSD) representation. FCSD representation replaces multiplication operations with addition and shift operations on the basis of a prime factor of coefficients. FCSD is the combination of factorization and Canonical Signed Digit representation of filter coefficients, which reduces the number of adders and also the cost of hardware. It gives a greater reduction in filter area, but there is a decrease in clock speed. The major drawback of this algorithm that it, increases the delay. The FCSD algorithm makes a trade-off between convergence calculation and complexity [18]. This example shows the comparison between CSD and factored-CSD algorithms:

```
Y = 99*X
  = (1100011)*X          % 99 in binary
  = (101'00101')*X       % 99 in signed digit format
  = (128-32+4-1)*X
  = (X<<7)-(X<<5) + (X<<2)-(X<<1)
CSD Cost = 4 Adders

Also,
  Y = 99*X
    = (33*3)*X
    = ((X<< 5+X)*(X<< 2-X)
FCSD Cost = 2 adders
```

Therefore, the above example concludes that the number of adders can be reduced by using the FCSD technique as compared to CSD.

IV.DESIGN SIMULATIONS

The required parameters for the implementation of a 16 tap multiplier less band stop IIR filter using the Butterworth, the filter length, cut off frequency, sampling frequency. In this simulation, the filter order is 16, the cut off frequency F_{c1} is 8.4 KHz, the cut off frequency F_{c2} is 13.2 KHz, the sampling frequency F_s is 48 KHz, and the attenuation is 3dB.The design specifications of an IIR filter are given in Table I [19]:

TABLE I. DESIGN SPECIFICATIONS BAND STOP OF FILTER

Filter Parameter	Value
Filter Length	16 Tap
Cut off Frequency1	8400 Hz
Cut off Frequency2	13200 Hz
Sampling Frequency	48000Hz
Attenuation	3dB

Table I shows the different parameters for designing of filter. In this paper, the Butterworth method is considered for designing the band stop IIR filter on the FPGA [21]. Overall, reducing computational complexity is an important consideration in filter design, as it can lead to more efficient and cost-effective implementations [18], particularly in applications with limited resources strict real-time processing requirements.
The Butterworth direct form-II method is considered in this work because it reduces computational complexity and increases speed performance [22], but the major drawback of this method is that it reduces accuracy. As the magnitude

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response of the band stop multiplier less IIR filter is shown in *Fig. 3*

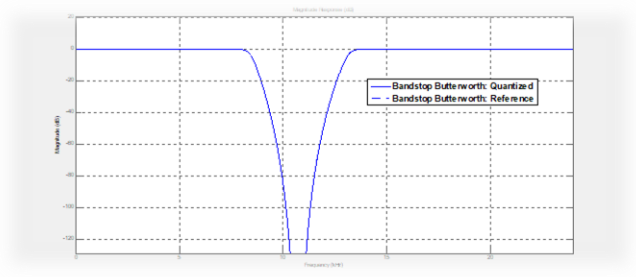

Fig.3. Magnitude Response of Low Pass IIR Filter

The phase response of the design IIR filter is shown in *Fig.4*. As IIR filters have non linear phase in general[23] but , the graph shows the Butterworth IIR filter has a slower rate of attenuation, but its phase response is more linear when compared to Chebyshev-I & II and Elliptical filters.

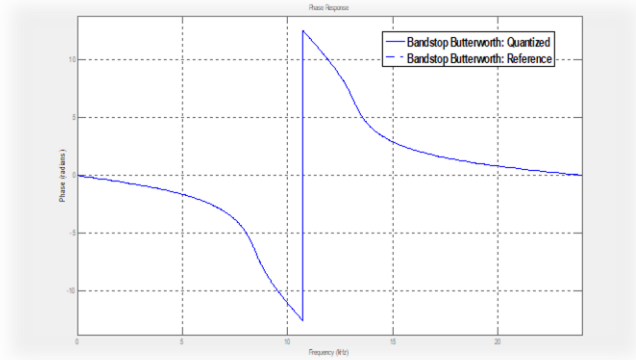

Fig.4. Phase Response of IIR Filter

The Impulse Response of IIR filter using the Butterworth window is shown in Fig.5.

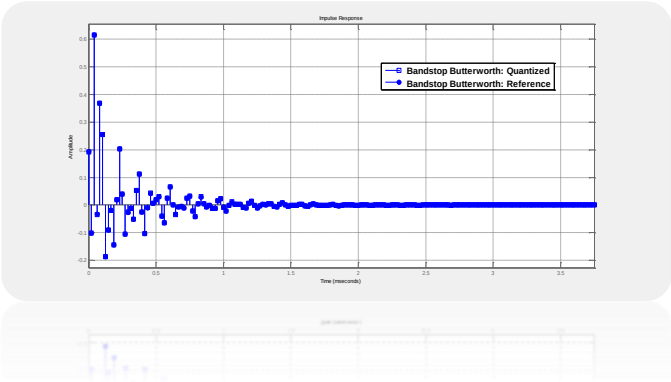

Fig.5. Impulse Response of the IIR Filter

The magnitude and phase response of a band stop IIR filter in a single graph are shown in *Fig.6.*

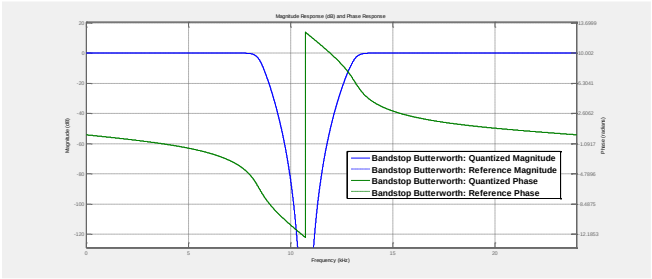

Fig.6. Magnitude and Phase Response of the IIR Filter

The pole–zero plot of IIR filter using the Butterworth window is shown in Fig.7.

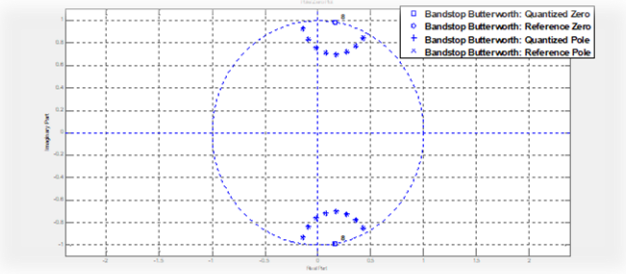

Fig.7. Pole –Zero Plot of the IIR Filter

V. FPGA SYNTHESIS

The proposed IIR band stop filter is implemented on two Xillinx's FPGA devices. Multiplier less IIR filter has been designed in MATLAB[24]. After that, it is further simulated on the FPGA using Spartan 3E,xc3s1200efg320-5, and Virtex 4,xc4vfx12sf363-12chips.The simulation results of CSD and factored-CSD based IIR filter using Spartan 3E, and Virtex 4 are shown in Figs.8 and 9 respectively. The filter responses on the FPGA are the same as on MATLAB.

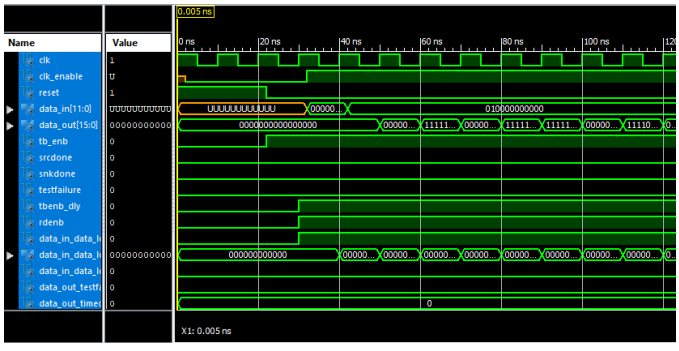

Fig.8. CSD based IIR filter input-output using Xilinx Spartan 3E

Here both the Simulation involves running IIR filters in a software environment, specifically utilizing the Xilinx [31] ISE tool. A test bench program is used to mimic the behavior of IIR filters by setting the inputs into the system. Figure 8 displays the Xilinx ISE Simulator outcomes for

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Spartan3E DSP [25], where as figure 9 exhibits the findings for Virtex4 as-

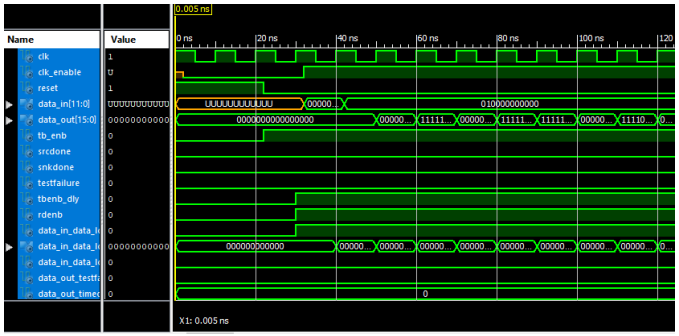

Fig.9. FCSD based IIR filter input-output using Xilinx Virtex4

The characteristics table of CSD and FCSD based IIR filter on Spartan 3E and Virtex4 chips[26] is given in Table II, III, IV, and V respectively. These tables show the availability and utilization of logic by Spartan 3E and Virtex4 chips [28].

TABLE II.THE CHARACTERISTICS TABLE OF SPARTAN 3E (CSD)

Logic Utilization	Used	Available	Utilization (%)
Slices	1956	8672	22%
Flip Flop	272	17344	1%
LUTs	3706	17344	21%

TABLE III.THE CHARACTERISTICS TABLE OF SPARTAN 3E (FCSD)

Logic Utilization	Used	Available	Utilization (%)
Slices	1934	8672	22%
Flip Flop	272	17344	1%
LUTs	3659	17344	21%

TABLE IV.THE CHARACTERISTICS TABLE OF VIRTEX 4(CSD)

Logic Utilization	Used	Available	Utilization (%)
Slices	1955	5472	35%
Flip Flop	272	10944	2%
LUTs	3704	10944	33%

TABLE V.THE CHARACTERISTICS TABLE OF VIRTEX 4(FCSD)

Logic Utilization	Used	Available	Utilization (%)
Slices	1923	5472	35%
Flip Flop	272	10944	2
LUTs	3637	10944	33%

A 16 tap multiplier less band stop IIR filter using CSD and FCSD has been implemented on Spartan3E and Virtex4 chips. VHDL is used for designing this filter. The result shows that the band stop IIR filter using CSD representation [27], consume 1956 slices, 272 flip flops, 3706 LUTs and FCSD representation consume 1934 slices, 272 flip flops, 3659 LUTs on Spartan3E and on the other hand, on Virtex4, the band stop IIR filter using FCSD representation [29], consume 1955 slices, 272 flip flops, 3704 LUTs and FCSD representation consume 1923 slices, 272 flip flops, 3637 LUTs. Hence we observe that less consumption in FCSD. The performance comparison between CSD and FCSD based IIR filter on Spartan 3E and Virtex4 chips[30] is summarized in Table VI.

TABLE VI. PERFORMANCE COMPARISON SPARTAN 3E & VIRTEX 4

Parameter	Spartan 3E		Virtex4	
	CSD	FCSD	CSD	FCSD
Slices	1956	1934	1955	1923
Flip Flop	272	272	272	272
LUTs	3706	3659	3704	3637
Speed (in ns)	170.510ns	170.074ns	85.034 ns	84.789 ns

Above table show that the FCSD representation, consume less slices and LUTs as compare to CSD representation. Spartan 3E and Virtex4 have minimum periods of 170.074 ns and 84.789ns, respectively. Hence, Spartan 3E has 50.145% more delay as compared to Virtex4.

VI. CONCLUSION

In this paper work, a design analysis of a 16 tap multiplier less digital band stop IIR filter on an FPGA is presented. The Butterworth design method is used direct form-II to design this IIR filter on MATLAB. After being implemented in MATLAB, the CSD and FCSD based IIR filter is further simulated on the FPGA using Spartan 3E and Virtex4 chips. Here, Simulation results show that the multiplier less IIR filter using Spartan 3E and Virtex4 have minimum period of 170.510 ns and 84.789ns respectively. Therefore, it is concluded that Virtex4, xc4vfx12sf363-12, is 50.145% better performance are achieved as compared to Spartan 3E, xc3s1200efg320-5. In future work, IIR filter design will perform based on optimal multiplier [25] to further moderate FPGA utilization.

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