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FPGA Implementation of Binary Pulse Compression Sequences with Superior Merit Factors

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Abstract

Binary codes have been widely used in radar and communication areas, but the synthesis of binary codes with good merit factor is a nonlinear multivariable optimization problem, which is usually difficult to tackle. To get the solution of above problem many global optimization algorithms like genetic algorithm, simulated annealing and tunneling algorithm were reported in the literature. However, there is no guarantee to get global optimum point. In this paper, a novel and efficient VLSI architecture is proposed to design Binary Pulse compression sequences with good Merit factor. The VLSI architecture is implemented on the Field Programmable Gate Array (FPGA) as it provides the flexibility of reconfigurability and reprogram ability. The implemented architecture overcomes the drawbacks of non guaranteed convergence of the earlier optimization algorithms.

***Keywords*:** FPGA, Pulse compression, Binary sequence, Ternary sequence, VLSI architecture.

1. INTRODUCTION

Pulse compression codes with low autocorrelation sidelobe levels and high merit factor are useful for radar [1], channel estimation, and spread spectrum communication applications. Pulse compression can be defined as a technique that allows the radar to utilize a long pulse to achieve large radiated energy but simultaneously obtaining the range- resolution of a short pulse. Theoretically, in pulse compression, the code is modulated onto the pulsed waveform during transmission. At the receiver, the code is used to combine the signal to achieve a high range resolution. Range-resolution is the ability of the radar receiver to identify nearby targets. The main criterion of good pulse compression is the Merit factor and discrimination. Merit factor is used to measure whether coded signal is a good or poor. This means that a code with high Merit factor is a good code while a code with low Merit factor is a poor code.

2. MERIT FACTOR (MF)

Golay [2] defined the merit factor (MF) as the ratio of mainlobe energy to sidelobe energy of Autocorrelation (AC) function of sequence S. The MF mathematically is defined as

$$MF = A(0) / 2 \sum |A(K)| \quad \text{where } k \neq 0 \quad \ldots\ldots\ldots\ldots 1$$

The denominator term represents the energy in the sidelobes.The merit factor MF must be as large as possible for good Sequence

3.NON BINARY PULSE COMPRESSION CODES.

A. Polyphase Code

Waveforms consisting more than two phases are called polyphase codes. The phase of sub pulse alternate among multiple values rather than 00 and 180 0. The sequence can be written as

$$\Phi n = 2\pi i(n-1)/p2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 2$$

B. Ternary Code

Ternary Code is the code that can be used to represent information and data. However ternary code uses 3 digits for representation of data. Therefore ternary code may also be called as 3-alphabet code. This code consists of 1, 0, and -1.

4. PROPOSED ARCHITECTURE

As the main lobe energy $A^2(0)$ of a given Binary sequence of length N is N^2 from equation 1, for the merit factor calculation of a Binary sequence, we need to calculate the side lobe energy of a Binary sequence. Since Merit factor is the main criterion for

good pulse compression sequences, therefore the Binary sequence having minimum sidelobe energy can be considered as the best Binary Pulse compression sequence. The proposed VLSI architecture for identification of the good Binary pulse compression is shown in the Fig. 1.The architecture mainly consists of eight blocks. They are sequence generator, sign conversion unit, multiplexer, multiplier, adder and accumulator unit, squaring unit, series of adder circuits, comparator and registers. The sequence generator is a synchronous counter. The counter consists of two inputs preset and clock.

At the beginning of counter operation the preset is set to one and it is bring back to zero. The architecture generates 3^N Binary sequences of length N. For all these 3 Sequences it calculates the sidelobe energy values, identifies and holds the sequence with minimum sidelobe energy. The sequence generator is a synchronous counter of length N which generates 3N sequences with 0's and 1's. These generated sequences are modified with the help of the sign conversion unit to get the Binary Pulse Compression sequence elements. As the Binary sequence consists of 0, +1 and -1, the sign conversion unit converts the bit '1' to 01, '0' to 00 and '-1' to 11. The multiplexer unit consists of inputs, select lines. The output of Counter block is given as select lines to the multiplexer. Depending on the combinations of the select lines, the corresponding input is given to the output.

The outputs of multiplexer units are applied as inputs to multiplier units. The Remaining hardware blocks are useful for computing, identifying and holding the lowest side lobe energy value of a Binary pulse compression sequence. The output register2 of Fig. 1 holds the good Binary pulse compression sequence. This sequence is represented by +1's, -1's and 0's. To convert this representation of the sequence to pure Binary sequences of 0, +1 and -1 we need to interface a little additional hardware to FPGA. For lower sequence length the proposed architecture generate all the 3N sequences, identifies and holds the best ternary sequence among the 3N sequences. In order to reduce the computing time and complexity for larger sequences of length N, the sequence generator of Fig. 1 can be modified to generate k bits dynamically and remaining (N-k) bits will be the fixed bits which can be taken from an already identified best sequence of length (N-k).

5. TECHNOLOGY AND TOOLS

The architecture shown in Fig. 1 has been authored in VHDL for 23-bit and 31-bit Binary Pulse compression sequences and its synthesis was done with Xilinx XST. Xilinx ISE Foundation 9.1i has been used for performing mapping, placing and routing. For Behavioral simulation and Place and route simulation Modelsim 6.0 has been used. The Synthesis tool was configured to optimize for area and high effort considerations. From the device utilization Summary the same Spartan-3 FPGA is useful for the implementation of higher lengths of the Binary Pulse Compression sequence.

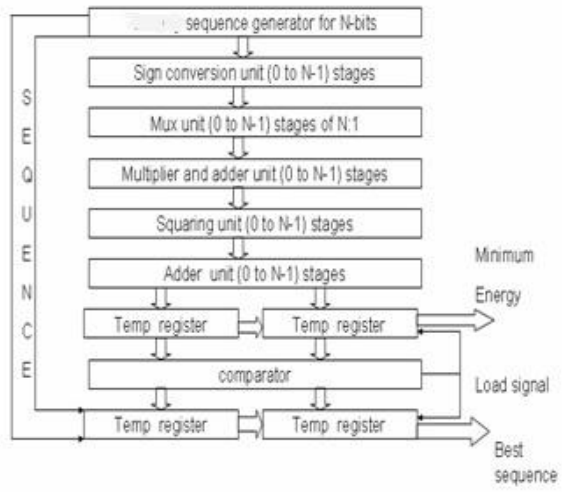

Fig.1. VLSI architecture for the identification of good Binary pulse compression sequence.

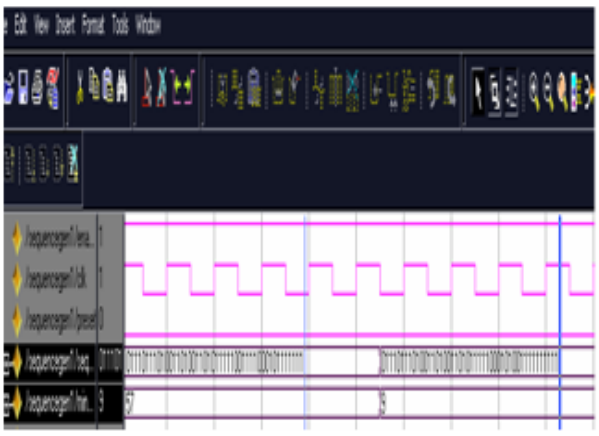

Fig. 2 Behavioral simulation result of a good 23-bit Binary Pulse compression sequence.

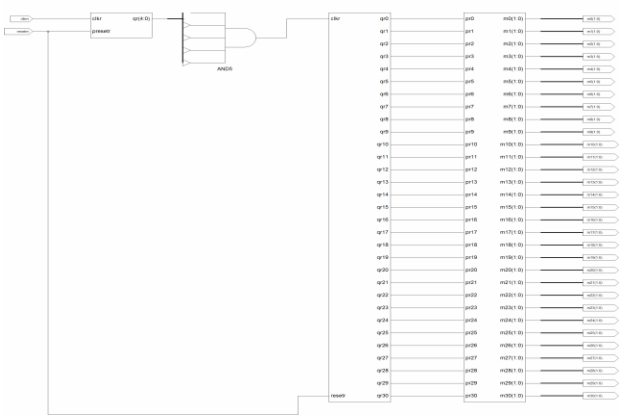

Fig. 6 RTL schematic of the proposed architecture

In table 1, column 1, shows sequence length, N and column 2, shows Merit Factor (MF).

Table I

Merit factor of synthesized Ternary sequences

Sequence Length (1)	MF (2)
21	14.0631
31	16.1533
37	10.4451
39	10.5225
41	10.6678
43	13.5700
51	14.0083
61	10.6369
63	08.2034
65	10.8659
67	08.691
69	10.4727
71	10.9136
73	9.8908
75	10.9764
77	08.6429
81	9.7225
83	10.5000
87	11.0860
89	10.2824
93	08.125
97	9.7438

An efficient VLSI architecture was proposed and implemented for the design of BInary sequences used in radar and communication systems for significantly improving the system performance. The synthesized Binary sequences have good Merit Factors. The synthesized Binary sequences are promising for practical application to radars and communications. It was also observed that the proposed architecture is giving good Merit Factor values for higher lengths. This shows the Superiority of the architecture.

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