FPGA Implementation of Data Acquisition System using XMK for Defense Applications

Rammohan Reddy Beeram
M.Tech in Embedded Systems
CVR College of Engineering (Autonomous)
Hyderabad (AP), India

Gudooru Ramakrishna Reddy
M.Tech in Embedded Systems
CVR College of Engineering (Autonomous)
Hyderabad (AP), India

Abstract: In defense applications of the real time missile system and during checkout before firing a missile it is required to monitor and control the functions of various subsystems. Sensors will be there for measuring process parameters, conditioning the signal and then input to the digital processing element for storage and retrieval of various parameters is the objective of modern Data Acquisition System (DAQ). The proposed DAQ system design is based on one single FPGA controlling all the sub systems with MicroBlaze Processor configured on Virtex-5 FPGA. The DAQ software includes Xilinx Microkernel (XMK), device drivers, application code for data storage and retrieval system. Multithreading, scheduling, timer and user interrupts gives a complete scope to fulfill the DAQ system to work in real-time environment. Development of such systems in advanced FPGAs allows considerable flexibility in terms of on-chip memory, Customization and production time which is not the case with DSP's and ARMs.

Keywords: Xilinx Microkernel (XMK); DAQ; RR Scheduling; GPIO; SCC; Interrupts;

1. INTRODUCTION

The data acquisition system converts a signal derived from a sensor into a sequence of digital values. The sensor is connected to an SCC (Signal Conditioning Circuit), which converts the signal into a potential. The SSC delivers an electrical signal input to digitizer, which contains an A/D converter. The digitizer produces a sequence of values representing the signal. A 16-channel ADC is combination of two 8-channel ADC's and is capable to output digital values from 16 varieties of sensors each connected to individual channel. The 8-bit data produced is stored sequentially in BRAM memory of Virtex-5 FPGA with time stamp. The time stamp allows user to retrieve and analyze the data either offline or online based on which user can invoke feedback network for control.

D/A Converter module produces samples and will interface directly with popular TTL, DTL or CMOS logic levels. The Proposed DAQ system gives total software control for data acquiring, storage, Interrupting and retrieving using Xilinx Microkernel (XMK) which is a robust, compact, flexible and also application oriented operating system. XMK programs are executed by FPGA MicroBlaze processor. The Embedded Development Kit (EDK) is a suite of tools and IP that can used to design a complete embedded processor system for implementation in a Xilinx FPGA device. Xilinx Platform Studio (XPS) is the development environment used for designing the hardware portion of embedded processor system. Multithreads, Scheduling, Interrupts and 3-stage pipelining add-ons and enhances scope makes the existence system replaceable by proposed DAQ system in real-time environment. Data is permanently stored in memory in real time and is a continuous process in this proposed system. A flexible report will be generated for analysis and decision making.

2. DAQ System

The DAQ System consists of 16 channel 8-bit ADC which can acquire data from 16 different kinds of sensors like pressure, temperature, humidity, the acquired analog information is converted to digital form and given to FPGA as input for further processing.Virtex-5 XUPV5LX110T evaluation platform is able store this digital data sequentially in contiguous memory locations based on user logic with system clock so that user can retrieve data in desired time and channel by selecting appropriate option from the IO device like keyboard for control. Similarly the data is converted back to analog form by using DAC interfaced as other subsystem in DAQ. The level shifters used in DAQ allow the voltage compatibility between FPGA, ADC and DAC devices. The proposed system is the software integration of FPGA based data acquisition system which is shown below in Figure1. ADC0809, DAC0808, Level shifters, PS2, MicroBlaze, XMK are core elements in DAQ system.

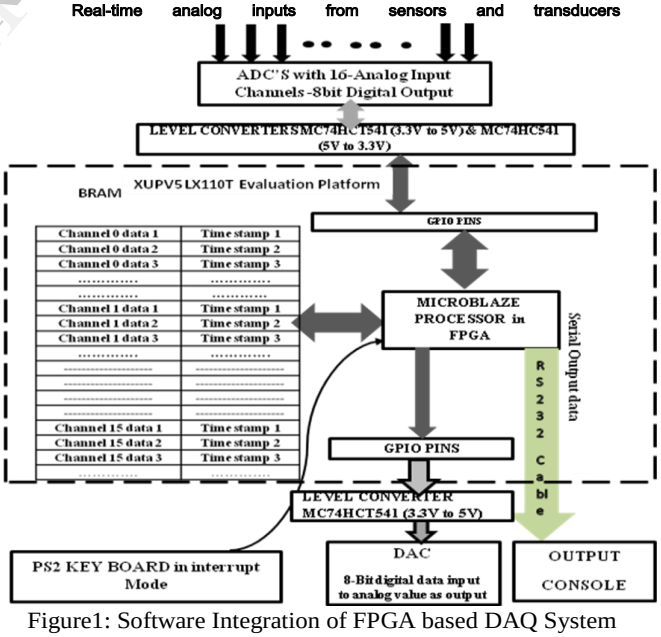

Figure1: Software Integration of FPGA based DAQ System

3. HARDWARE PLATFORM

3.1 Xilinx Virtex-5 FPGA

The **Xilinx XUPV5-LX110T** is a versatile general purpose development board powered by the Virtex-5 FPGA. It is a feature-rich general purpose evaluation and development platform, includes on-board memory and industry standard connectivity interfaces, and delivers a versatile development platform for embedded applications.

IJERT

3.2 MicroBlaze Processor

MicroBlaze is the industry-leader in FPGA-based soft processors, with advanced architecture options like AXI or PLB interface, Memory Management Unit (MMU), instruction and data-side cache, configurable pipeline depth, Floating-Point unit (FPU), and much more. MicroBlaze is a 32-bit RISC Harvard architecture soft processor core. Highly flexible architecture, plus a rich instruction set optimized for embedded applications, delivers the exact processing system at the lowest system cost possible.

The LogiCORE MicroBlaze Micro Controller System (MCS) is a complete standalone processor system intended for controller applications. It is highly integrated and includes the MicroBlaze processor, local memory for program and data storage as well as a tightly coupled I/O module implementing a standard set of peripherals. MicroBlaze can be user configurable cache size, pipeline depth (3-stage or 5-stage), embedded peripherals, memory management unit, and bus-interfaces

3.3 PLB Interface

The PLB Interface Module provides the interface to the PLB and implements PLB protocol logic. PLB Interface Module is a bi-directional interface between a user IP core and the PLB bus standard. To simplify the process of attaching a XPS UART Lite to the PLB, the core make use of a portable, pre-designed bus interface called PLB Interface Module, that takes care of the bus interface signals, bus protocols, and other interfaces.

3.4 GPIO

The XPS GPIO design provides a general purpose input/output interface to a Processor Local Bus (PLB). The XPS GPIO can be configured as either a single or a dual channel device. The channel width is configurable and when both channels are enabled, the channel width of each of the channels can be configured individually.

3.5 PS2 Keyboard

The LogiCORE IP XPS PS2 Controller is a PLB (Processor Local Bus) slave that is designed to control PS2 devices such as keyboard for external user interrupts. The PS2 protocol is a simple bidirectional serial protocol

3.6 Interrupt Controller

In DAQ era interrupts are available in the form of timers, kernel system timer and external source like mouse and keyboard. The four timers used here are configured as Timer0 in interrupt mode for scheduling purpose, Timer1 is for real time clock and is configured in interrupt mode, Timer2 and Timer3 is used for producing time delays for ADC and DAC functionality respectively.

Table 1: Interrupt sequence from Interrupt Controller

DAQ System interrupt input	Priority
Timer 0 Interrupt for real time clock	1
PS2 Keyboard Interrupt	2
Timer 1 Interrupt for scheduler	3

As MicroBlaze processor has only one interrupt pin, multiple interrupts are connected through interrupt controller as inputs and output of the interrupt controller is connected to the interrupt pin of the MicroBlaze processor.

3.7 UARTLITE

The XPS Universal Asynchronous Receiver Transmitter (UART) Lite Interface connects to the PLB (Processor Local Bus) and provides the controller interface for asynchronous serial data transfer. The PLB interface module Supports 8-bit bus interfaces with One transmit and one receive channel (full duplex mode). The UART Control Module consists of RX module, TX module, parameterized baud rate generator (BRG) and a Control Unit. It incorporates the state machine for initialization and start & stop bit control logic.

3.8 DIGITIZER

A digitizer converts one or more channels of analog signal to a sequence of corresponding digital values. The heart of a digitizer is an A/D converter, a device that samples an analog signal and converts the sample to a digital value. The proposed DAQ System has ADC0809 data acquisition component which is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique.

ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications.ADC performance specifications are generally categorized as DC accuracy and dynamic performance. Most applications use ADCs to measure a relatively static, DC-like signal (for example, a temperature sensor or strain-gauge voltage) or a dynamic signal (such as processing of a voice signal or tone detection). The application determines which specifications the designer will consider the most important.

The process of analog to digital conversion always involves comparing two analogue signals:an input signal and some reference signal.A comparator circuit is essentially a high-gain differential amplifier. When Vin > Vref the output of the comparator swings to the positive supply rail, and so the output is “1”, if Vin < Vref the output voltage swings to the earth rail, “0”. Thus, the comparator gives a clear indication of which of two voltages is the larger.

3.9 Signal Conditioning Circuit

A DAQ system converts a signal derived from a sensor into a sequence of digital values. The sensor is connected to an SCC (Signal conditioning circuit), which converts the signal into a potential. The SCC is in turn connected to a digitizer, which contains an A/D converter. The digitizer produces a sequence of values representing the signal.Figure2 shows the conversion of physical parameters like pressure, temperature into voltages, digital values using signal conditioning circuit

Figure2: Interfacing of Signal Conditioning Circuit (SCC)

IJERT

3.10 DAC Converter

The Application program running on FPGA drives data from memory and inputs to DAC system. The DAC0808 is an 8-bit monolithic digital-to-analog converter featuring a full scale output current settling time of 150 ns. The current 'I' is given by Expression-1. The LF351 is JFET input operational amplifier with an internally compensated input offset voltage. The JFET input device provides wide bandwidth, low input bias currents and offset currents.

$$I = \frac{V_{REF}}{R14}\left(\frac{D_0}{2}+\frac{D_1}{4}+\frac{D_2}{8}+\frac{D_3}{16}+\frac{D_4}{32}+\frac{D_5}{64}+\frac{D_6}{128}+\frac{D_7}{256}\right) \quad (1)$$

3.11 Level Shifters

An 3.3 V device like FPGA GPIO voltages can be interfaced with an ADC0809/DAC0808 with Level shifter for voltage compatibility.MC74HCT541, MC74HC541 are up and down shifters respectively, were used in this DAQ system.

4. SOFTWARE IMPLEMENTTION

4.1 XMK(Xilinx Micro Kernel):

Xilinx Microkernel (XMK or Xilkernel) is a small, robust, and modular kernel. It is highly integrated with the Platform Studio framework and is a free software library with the Xilinx Embedded Development Kit (EDK). It allows a very high degree of customization, letting users tailor the kernel to an optimal level both in terms of size and functionality. It supports the core features required in a lightweight embedded kernel, with a POSIX API. Xilkernel works on both the Micro Blaze and PowerPC 405 processors.

Xilkernel IPC services can be used to implement higher level services (such as networking, video, and audio) and subsequently run applications using these services. Typical embedded control applications are comprised of various tasks that need to be performed in a particular sequence or schedule. As the number of control tasks involved grows, it gets very hard to manually organize the sub-tasks and time-share the work that needs to be done. Breaking down tasks as individual applications and implementing them on an operating system (OS) is much more intuitive. It enables to write code at an abstract level, instead of at a small, micro controller level standalone code where many common and legacy applications rely on.

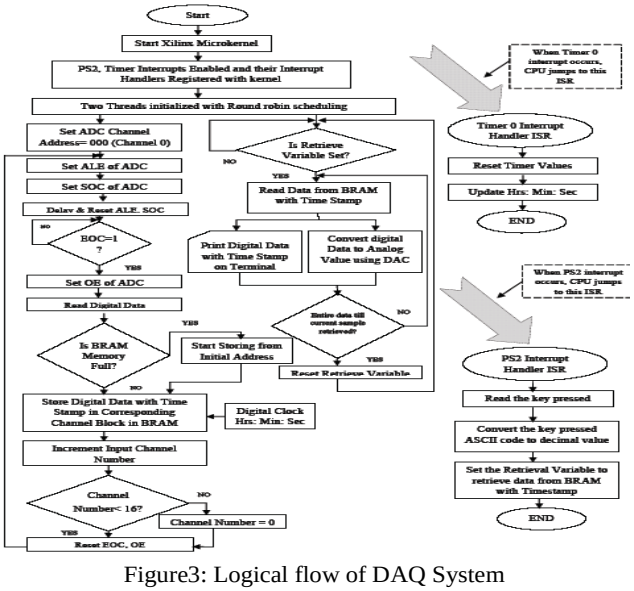

Figure3: Logical flow of DAQ System

OS services such as file systems, time management, etc. Xilkernel is a thin library that provides these essential services, porting or using common/open source libraries (such as graphics or network protocols) may also require some of these OS services.Figure3 shows the step-by-step execution flow for the proposed DAQ system.

4.2 Xilkernel as Scheduling Model

DAQ system uses SCHED_RR scheduling technique here, instead Xilkernel also supports priority-driven, preemptive scheduling with time slicing(SCHED_PRIO) or simple round-robin scheduling (SCHED_RR).Scheduling of threads must be configured statically at kernel generation time. In SCHED_RR.for these scheduling models, the length of the ready queue can also be configured.

4.3 Kernel customization

Xilkernel is highly customizable. Modules and individual parameters can be changed to suit the user application. The Xilinx Platform Studio (XPS) Software Platform Settings dialog box provides excellent support for easy configuration of parameters of Xilkernel. The configuration directives in the MSS specification have the corresponding implication on memory and code size of the resultant Xilkernel image. If a process context structures occupies x bytes of bss memory, then the total bss memory requirement for process contexts is (*max_pthreads*x*) bytes. Therefore, such parameters should be carefully tuned, and the final kernel image should be examined with the GNU size utility to make sure that memory requirements are met.

4.4 XMK Interrupts

The interrupt controller device in the system kernels. Adding this parameter automatically configures multiple interrupt support and the user-level interrupt handling API in the kernel can be configured. This also causes the kernel to automatically initialize the interrupt controller.

5. Result and Analysis

An Application program with all the above mentioned constraints is being written and downloaded as bit file onto FPGA flash memory. The proposed DAQ system was successfully implemented using MicroBlaze Processor configured on Virtex-5(XUPV5-LX110T) board using EDK XPS 12.4 tool with Xilinx Microkernel. The analog data from the sixteen channels are taken and processed by the ADC's and converts them into corresponding digital values. These digital values are stored into the memory along with time stamp. An will full key stroke of PS/2 keyboard retrieves data of corresponding channel by pressing corresponding channel number key on keyboard. Then acquiring process is done in background and retrieving process of the corresponding channel along with time stamp is done in foreground with the help of Round Robin scheduling. Also, Digital Value is converted to analog value by DAC. After retrieving process is completed, then acquiring process is done in foreground. Data Acquisition process never stops.

IJERT

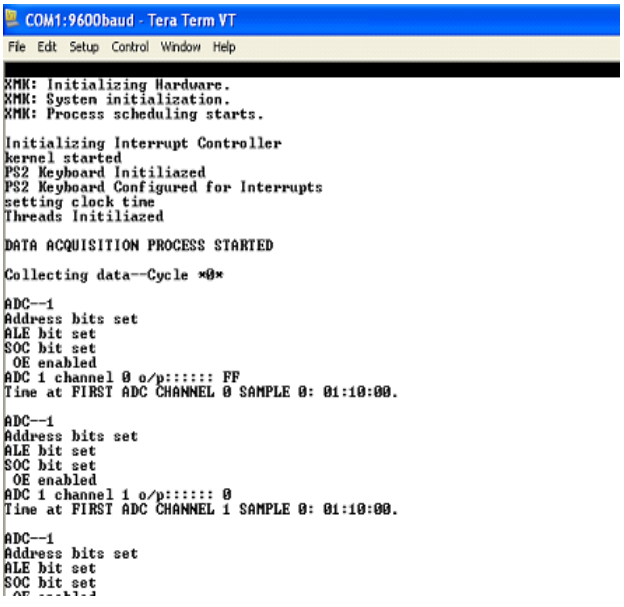

Figure4: Data acquiring process initialization by XMK

Figure4 shows the initialization process of kernel and all the 16-channels of DAQ system whereas Figure5 shows the data retrieving process with timestamp. The temperature to voltage and Voltage to Digital value representation is given in Table2.The system has been tested for various sensors like pressure and temperature. The interfacing of devices, RTD, components, PS/2 to FPGA environment is shown in figure 6. The proposed DAQ system tested will be developed as PCB and can be used to monitor missile health in defense.

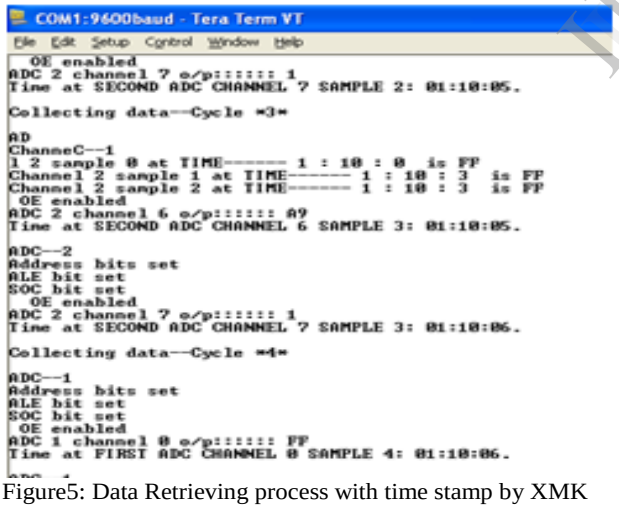

Figure5: Data Retrieving process with time stamp by XMK

Table2: Analog to Digital value representation

Temperature (^{0}C)	Analog Voltage From Transducer	Digital Output
28^{0}C	1.2	40
52^{0}C	3.5	B3
76^{0}C	3.9	CD
97^{0}C	4.9	FD
104^{0}C	5.1	FF

Figure6: A DAQ system with Interconnection, RTD sensor, Logic analyzer and components interconnected to FPGA

6. REFERENCES

[1].H.S. Murali & M.Meenakshi, "Design and Development of FPGA Based Data Acquisition System for Process Automation", CCSE, Volume 1, Issue 1, January 2013.
[2].B.Fletcher,"FPGA Embedded Processors, Revealing True System Performance", in Embedded Systems Conference, San Francisco, USA, ETP-367, March 2005.
[3].Anders Ronnholm, "Evaluation of Real-Time Operating Systems for Xilinx MicroBlaze CPU", M.S. Thesis, Department of Computer Science and Electronics,M.alardalens University,Vasteras,Sweden 2006.
[4].Gokhan Ugurel and Cuneyt F.Bazlamac, "Context Switching Time and Memory Footprint Comparison of Xilkernel and uC/OS-II on MicroBlaze", ELECO 2011 7th International Conference on Electrical and Electronics Engineering, 1-4 December, Bursa, TURKEY.
[5].Embedded Concepts, Tools and Techniques Reference Manual, EDK 12.4.
[6].Embedded Systems Tools Reference Manual, EDK 12.4.
[7].MicroBlaze Processor Reference guide, EDK 12.4.
[8].Xilkernel (Xilinx Micro Kernel) Reference Manual, EDK 12.4.
[9].XPS General Purpose Input/output (GPIO) IP Reference Manual, EDK 12.4.
[10].LogiCORE IP XPS PS2 Controller Reference Manual, EDK 12.4.
[11].LogiCORE IP XPS Timer/Counter Reference Manual, EDK 12.4.
[12].XPS UART Lite IP Reference Manual, EDK 12.4.
[13].LogiCORE IP XPS Interrupt Controller Reference Manual, EDK 12.4.
[14].http://forums.xilinx.com/
[15].http://www.fpga4fun.com/
[16].http://www.fpgadeveloper.com/
[17]. http://www.xilinx.com/support/index.htm

IJERT