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# FPGA Implementation of Digital Down Converter using Multiplier-Free Filter

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***Abstract-*** **In this paper, we concern with designing and implementing a Digital Down Converter (DDC) which is an essential block in case of designing a digital receiver with FPGA. In a Communication System, especially in some applications where the data is to be communicated confidentially, wide band of signals are used. In such scenarios, a wide band DDC with variable filter specifications are required. Though the received signal is RF signal with high data rates and IF stage is used to frequency shift the signal to fixed IF which is the input to ADC. This is sampled and fed as input to DDC. Digital Down Conversion is a technique used in communication systems that accepts the band limited high sampling rate modulated signal and recovers the original message signal from it through filtering action. Digital Down conversion is employed applications like multi-rate signal processing and also in case of designing channelized receivers. Wide band DDC means considering the decimation factor of filter between 8 to 32. In this paper, it is considered as 8. The proposed architecture can be realized coding it using Verilog HDL. Simulation is done using Xilinx ISE 12.4i design software, Modelsim 6.5c and it is targeted into Xilinx Virtex-5, XC5VLX110T FPGA.**

***Keywords: Digital Down Converter (DDC), Digital Receiver, Decimation, Virtex-5, Verilog HDL, FPGA, Modelsim 6.5c, Chipscope Pro Analyzer.***

## I. INTRODUCTION

Communication plays vital part in day to day life for transfer of information. Thought there are various modes of communication, Digital communication has been popular at present. It is the process of transferring information in terms of bits. The main blocks of communication system are a transmitter, channel and a receiver. The DDC presented in this paper is the key component of receiver. The output of ADC i.e., digital IF signal is fed to DDC as an input. The speed of ADC depends on band of interest according to Nyquist's criteria which states that the signal to be sampled at a rate at least double the bandwidth of interest. DDC allows the frequency band of interest to be moved down the spectrum to baseband signal near to 0Hz such that further processing of signals become easier.

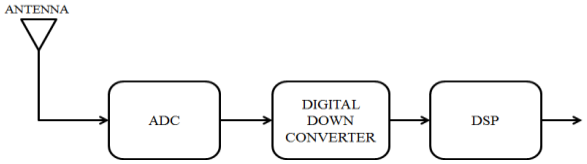


Figure 1: Block Diagram of Digital Receiver

## II. OVERVIEW OF DDC

DDC is a technique which takes band limited high sampling rate digitized signal, shifts the band of interest to a lower frequency and reduces the sample rate while retaining all the information. It converts a digitized real signal centered at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency by using a mixer. Also in addition to down conversion, DDC's typically decimate to a lower sampling rate by using a several stages of decimation filters. The decimated signal with lower data rates is easier to process on a low speed DSP processor.

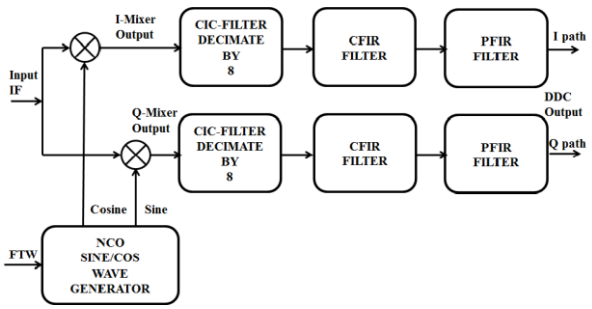


Figure 2: Block Diagram of DDC

DDC consists of five basic blocks.

i. Direct Digital Synthesizer (DDS).
ii. Mixer.
iii. Cascaded Integrator Comb (CIC) filter.
iv. Compensating FIR (CFIR) filter.
v. Programmable FIR (PFIR) filter.

### *A. Direct Digital Synthesizer (DDS)*

Direct Digital Synthesizer also called as Numerically Controlled Oscillator generates a complex sinusoid at the intermediate frequency. It provides a flexible architecture which enables easy programmability such as on-the-fly frequency/phase. A sine wave can be generated by rotating a vector around the phase wheel.

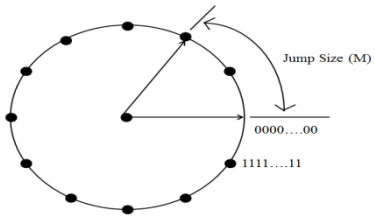


Figure 3: Digital Phase Wheel

DDS consists of two parts.

- ***Phase Accumulator (PA):***

The main part of the DDS system is the "Phase Accumulator" whose contents are updated once on each clock cycle. Each time the phase accumulator is triggered, the tuning word or phase increment ($\Delta f$) is added to the contents of phase accumulator.

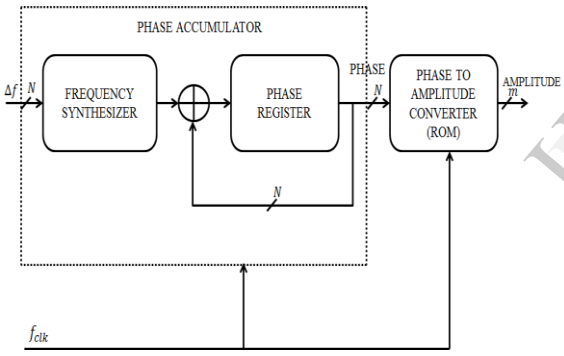


Figure 4: Block Diagram of Direct Digital Synthesizer

This word forms phase step-size between reference clock updates; it effectively sets how many points to skip around the phase wheel. PA replaces the address counter to introduce a function known as a "phase wheel" which can be visualized as a vector rotating around the phase circle. Each point of a phase wheel corresponds to the sample phases of a full sine wave. Each time PA receives the clock pulse, the PA increases the stored number in the phase register by adding FTW to that register. Tuning frequency is obtained by using the below formula,

$$f_{out} = \frac{(\Delta f * f_{clk})}{2^N}$$

Where

$\Delta f$ is the Frequency Tuning Word

$f_{out}$ is the required output frequency

$N$ is number of bits required to represent FTW

$f_{clk}$ is Clock frequency

Frequency Tuning Word (FTW) forms a "hopping" process to skip the N-bit phase points of the phase wheel. These N-bit phase points are known as phase step size or phase jump size. The control over the jump size constitutes the Frequency Tuning resolution of the DDS system. The larger the jump size, the faster the PA overflows to complete the generation of a sine-wave cycle.

The output of Phase Accumulator (in degrees) is obtained by using the below formula,

$$Phase\ Accumulator\ Output\ PA = \frac{(n * \Delta f * 360°)}{2^N}$$

- ***Phase to Amplitude Converter (PAC):***

Phase to Amplitude Converter (PAC) or Look Up Table (LUT) is configure as Sine/Cosine LUT. It used the N-bit output from the Phase Accumulator (PA) phase word as an address into a waveform Look Up Table (LUT) to provide corresponding amplitude of sine wave. The output value at the phase to amplitude converter may be expressed by,

$$PAC\ output\ x(n) = sin(PA)$$

If "N" represents the width of the truncated phase, a sine/cos LUT can be simply a ROM containing $2^N$ samples that crate the sample domain waveform from the phase received from the PA. In other words, it converts the phases from a PA to amplitudes. These digital phases are also the memory addresses used to retrieve the corresponding amplitudes from the sine LUT.

### *B. Mixer*

A mixer is used to convert IF signal to baseband signal by multiplying the input signal to complex sinusoidal signal $\cos(wt) - j\sin(wt) = e^{-jwt}$ which is generated by NCO thus giving two signals as output which are 90 degrees out of phase with each other i.e.,

i. In-Phase signal
ii. Quadrature-Phase signal

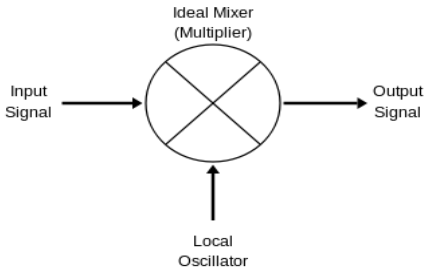


Figure 5: Block Diagram of an Ideal Mixer

This works on the following principle:

*Frequency(A) * Frequency(B) = Frequency(A-B) + Frequency(A+B).*

But aliases obtain at the mixer stage due to the difference frequencies which are removed in the further stages using filtering techniques.

*C. CIC Filter*

Cascaded Integrated Comb filter or Hogenauer filters are multi-rate filters used for realizing large sample rate changes in digital systems. These are multiplierless structures, consisting of only adders, subtractors and registers. They are typically employed in applications that have large excess sampling rate i.e., system sampling rate is much larger than the bandwidth of the signal.

Basically, it is a cascade of digital integrators followed by a cascade of combs (digital differentiators) in equal number. Between the integrators and the combs there is a digital switch or decimator, used to lower the sampling frequency of the combs signals w.r.t. sampling frequency of the integrators.

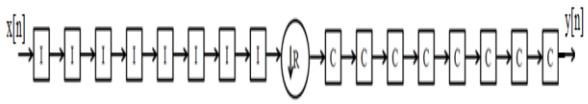


Figure 6: Block diagram of CIC decimating filter

The two basic building blocks of a CIC filter are as follows.

1. *An Integrator:* The integrator section consists of "N" ideal integrator stages operating at the high sampling rate ($f_s$). Each stage is implemented as a one-pole IIR filter with a unity feedback coefficient. It is also known as an accumulator.

The basic structure of a single stage integrator is shown in the following figure.

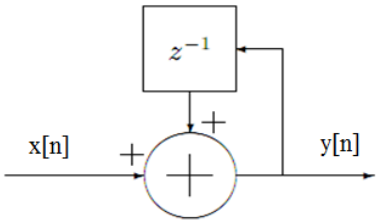


Figure 7: Block diagram of an Integrator

The transfer function of an integrator from above diagram can be found as:

$$y[n] = x[n] + y[n-1]$$

In z-plane, it can be given as:

$$H_I(Z) = \frac{1}{(1 - Z^{-1})}$$

The power response is basically a low pass filter with a 20dB per decade (-6dB per octave) roll off, but with an infinite gain at DC. This is due to single pole at z=1; the output can grow without bound for a bounded input. In other words, single integrator by itself is unstable.

2. *Comb:* The comb section operates at the low sampling rate "$f_s$/R" where "R" is the integer rate change or decimation factor. This section consists of comb stages with a differential delay of "M" samples per stage.

The basic structure of single comb is shown in the following figure.

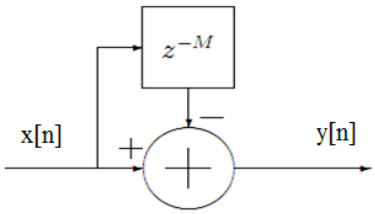


Figure 8: Basic structure of Comb

The differential delay is a filter design parameter used to control the filter's frequency response. "M" is restricted to either "1" or "2".

The transfer function of single comb stage, referenced to the high input sampling rate is:

$$y[n] = x[n] - x[n - RM]$$

In Z-domain, it is given as:

$$H_C(Z) = 1 - Z^{-RM}$$

Between "I" and "C" sections there is a rate change switch called decimator which subsamples the output of the last integrator stage, reducing the sampling rate from "$f_s$" to "$f_s/R$".

The system transfer function for the composite CIC filter referenced to the high sampling rate is given as:

$$H_{cic}(Z) = H_I^N(Z) * H_C^N(Z) = \frac{(1 - Z^{-RM})^N}{(1 - Z^{-1})^N} = \left[\sum_{k=0}^{RM-1} Z^{-k}\right]^N$$

The frequency response is found by evaluating above equation at $z=e^{j2\pi f}$. The magnitude frequency response for a CIC filter with a decimation factor of 8 is shown in the following figure.

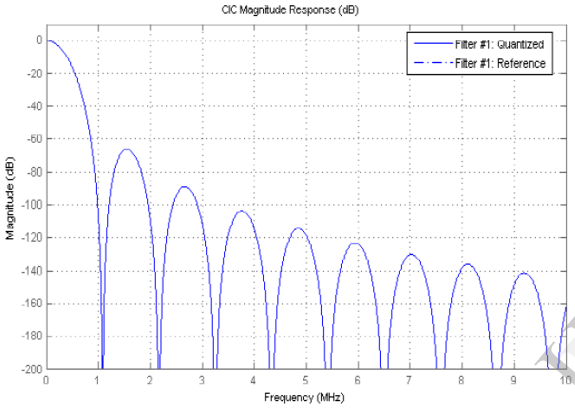


Figure 9: Frequency Response Characteristics of CIC filter with decimation factor of 8

The transfer function of CIC filter in Z-plane yields a sinc function which is shown as follows.

$$|H(f)| = \left|\frac{\sin \pi RMf}{\sin(\pi f)}\right|^N$$

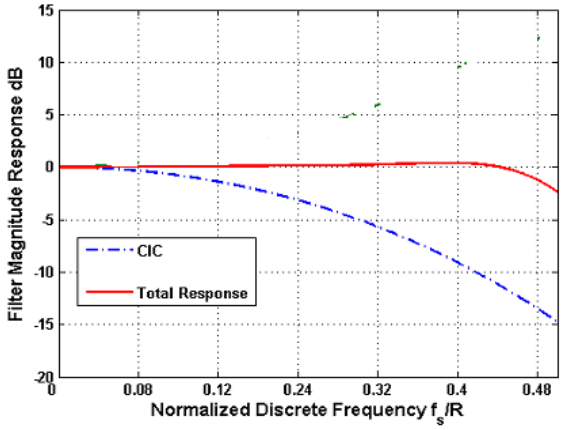


Figure 10: Magnitude Response showing pass band droop in CIC filter

In CIC filter, there is a disadvantage that it exhibits pass band droop. So, CFIR filter is used to compensate this.

*D. CFIR Filter*

The output of the CIC filter has a sinc shape which is not suitable for most applications. A "clean up filter" can be applied at the CIC output to correct for the pass band droop as well as to achieve the desired cutoff frequency and filter shape. This filter typically decimates by a factor of "2" or "4" to minimize the output sample.

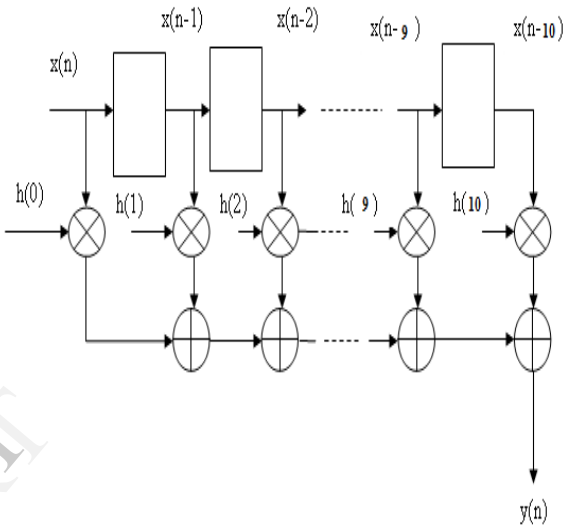


Figure 11: Basic structure of CFIR filter

The difference equation of CFIR filter showing the relation between the inputs and outputs is as follows:

$$y(n) = b_0x(n) + b_1x(n-1) + \ldots\ldots\ldots + b_Px(n-P)$$

Where P is the filter order, x(n) is the input signal, y(n) is the output signal and $b_i$ are the filter coefficients. The previous equation can also be expessed as follows:

$$y(n) = \sum_{i=0}^{P} b_i x(n-i)$$

For this filter 11 coefficients are chosen with 24-bits precision.

The magnitude response of CFIR filter is shown in the following equation.

$$H(f) = \left|MR\frac{\sin \pi f}{\sin(\pi RMf)}\right|^N \approx \left|\frac{\pi MRf}{\sin(\pi RMf)}\right|^N = |\sin c^{-1}(MRf)|^N$$

Filter response of CIC and CFIR together is shown in the below figure.

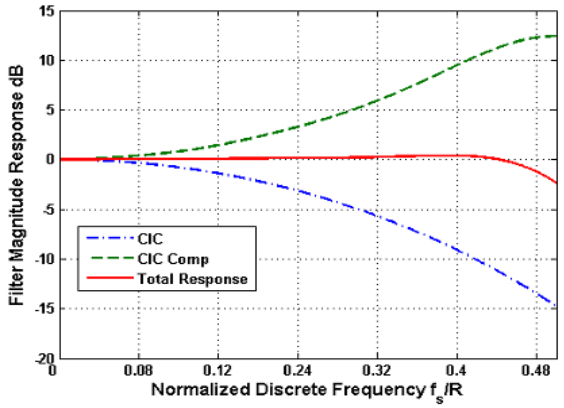


Figure 12: Magnitude Response of CFIR Filter

*E. Programmable FIR filter:*

For the final stage, an equiripple filter is chosen which provides an additional filtering, decimation by 2.
The output from PFIR is the final down converted output. All other characteristics is same as that of CFIR filter except the number of filter coefficients chosen are 41.

## III. IMPLEMENTATION ON FPGA

An advantage of using an FPGA for DDC is that we can customize the filter chain to exactly meet our requirements. ASSPs don't offer the design flexibility or integration attainable in an FPGA.

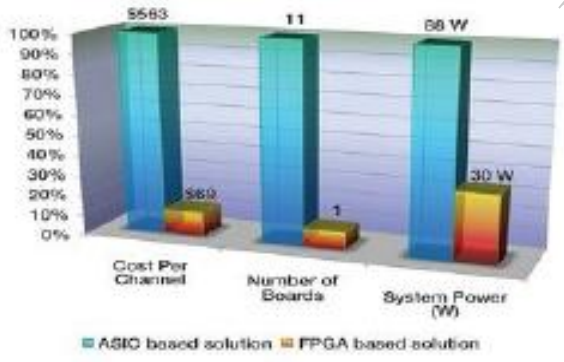


Figure 13: Comparision of ASIC and FPGA

During the design, a behavioral model of the complete DDC is developed using Xilinx ISE software by writing verilog code for each individual block and their operation is tested by simulating the design using ISE simulator and Modelsim simulator. Later the design is synthesized and implemented on FPGA by generating a bit file of the design and programming, configuring the FPGA with the .bit file. The Xilinx FPGA design flow is shown below.

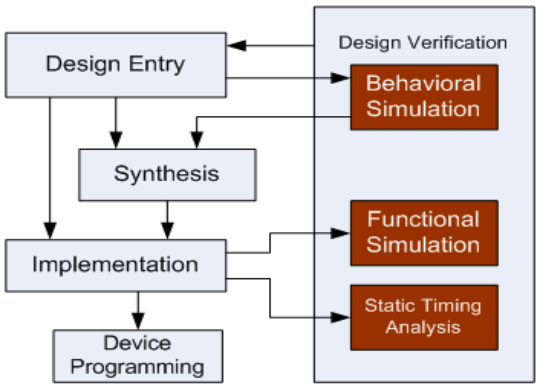


Figure 14: Xilinx FPGA design flow

The correct operation of the design in the FPGA design is tested using Chipscope Pro Analyzer tool which uses three main blocks to analyze any part of DDC. These blocks are generated using IP Core generator tool in Xilinx ISE. The blocks are:

### *1. ICON:*

Integrated Controller is used as an interface between the other two blocks and PC using JTAG which is connected to FPGA on which the design is programmed.

### *2. ILA:*

Integrated Logic Analyzer is used to control the inputs of any part of DDC thus achieving Controllability of inner Circuits.

### *3. VIO:*

Virtual Input Output is used to observe the outputs of any part of DDC thus achieving observability.

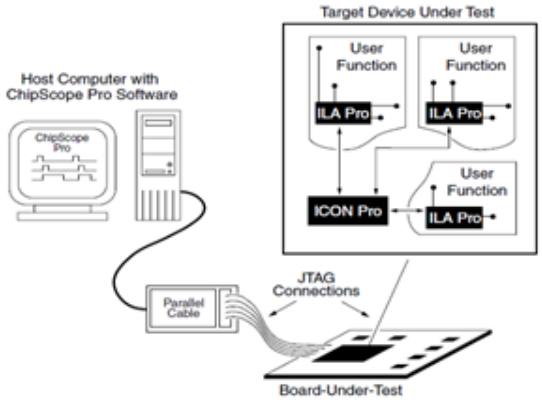


Figure 15: Chipscope Pro Block Diagram

Thus, board level testing has also been performed.

## IV. RESULTS AND DISCUSSIONS

### 1. *RTL Schematic*

The RTL schematic of Digital Down Converter with its internal blocks is shown in Figure 16.

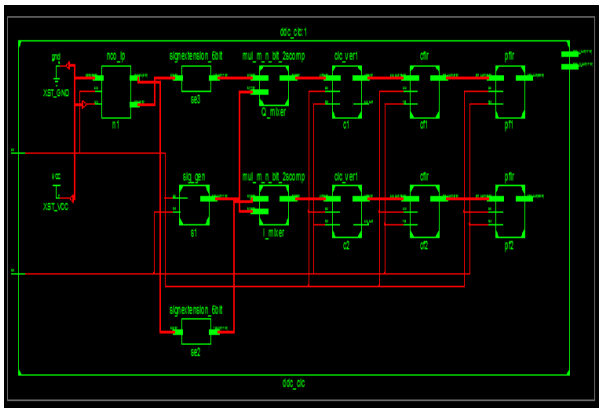

Figure 16: RTL schematic of DDC with back to back connected Mixer, CIC filter, CFIR and PFIR filters.

### 2. *Simulation Results*

The simulation results of DDS/NCO with carrier frequency for 5MHz with FTW = $(13421772)_{10}$ considering $f_{clk}$ as 100MHz we obtain sine and cosine outputs along with the phase accumulator output are shown in Figure 17.

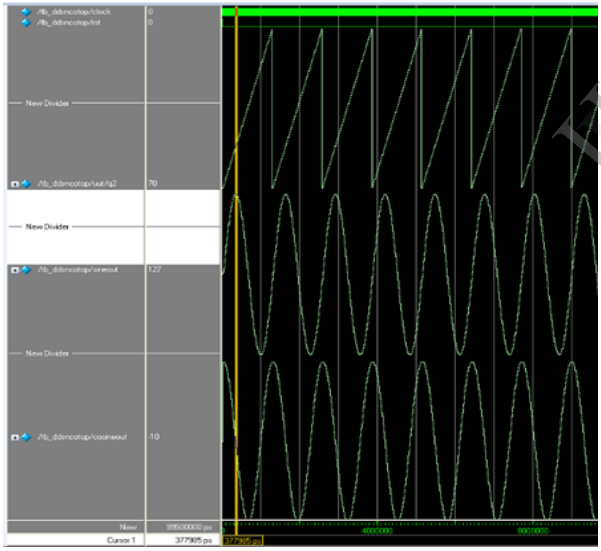

Figure 17: Simulation results of DDS/NCO in ModelSim

The simulation results of DDC with consideration of Mixer, CIC, CFIR and PFIR filters are shown in Figures 18 and 19.

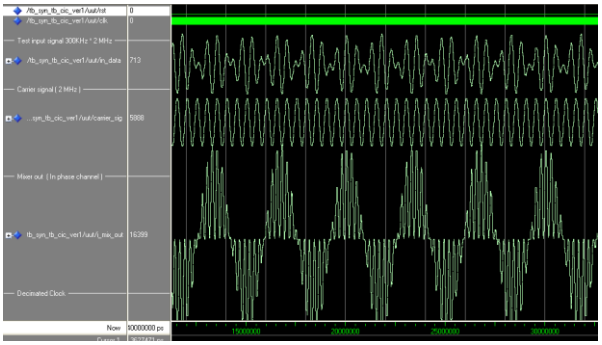

Figure 18: Simulation Results of DDC considering upto IF signal, NCO, Mixer

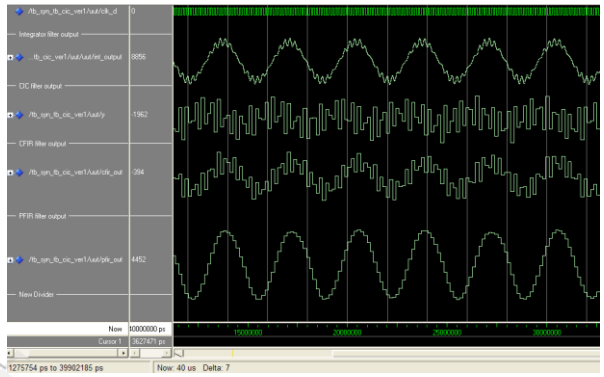

Figure 19: Simulation Results of DDC considering integrator, decimator, comb, CIC filter, CFIR filter and PFIR filter

The output of the PFIR filter is the down converted output which is the baseband signal.

### 3. *Device Utilization Summary*

The Device Utilization Summary of DDC is shown in Table 1.

Table 1: Device Utilization Summary of DDC

| Device Utilization Summary (estimated values) | | | [-] |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slice Registers | 2760 | 28800 | 9% |
| Number of Slice LUTs | 14280 | 28800 | 49% |
| Number of fully used LUT-FF pairs | 968 | 16072 | 6% |
| Number of bonded IOBs | 20 | 480 | 4% |
| Number of Block RAM/FIFO | 2 | 60 | 3% |
| Number of BUFG/BUFGCTRLs | 2 | 32 | 6% |
| Number of DSP48Es | 16 | 48 | 33% |

*4. Timing Summary*

Speed Grade: -1
Minimum period: 2.329ns (Max Frequency 429.3MHz)
Minimum input arrival time before clock: 4.894ns
Maximum output required time after clock: 90.150ns
Maximum combinational path delay: No path found

*5. FPGA Prototyping*

The design of DDC is verified on Xilinx Virtex-5, XUPV5LX110T FPGA board by using Xilinx iMPACT device configuration tool. The output of DDC on Virtex-5 XUPV5LX110T FPGA board with bouncing pattern of LEDs indicating the different sampled values of DDC output is shown in Figure 20.

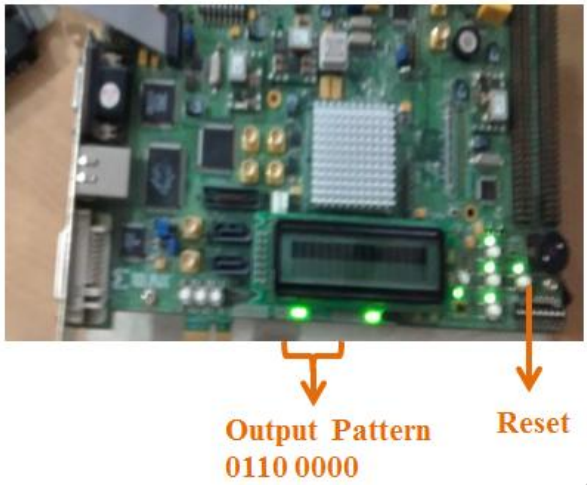


Figure 20: Output of DDC on Xilinx Virtex-5 XUPV5LX110T Evaluation board

*6. Chipscope Pro Results*

After porting the .bit file on FPGA, the results obtained on FPGA are observed using Chipscope Pro software.

Figure 21 shows the NCO output result from Chipscope Pro Analyzer.

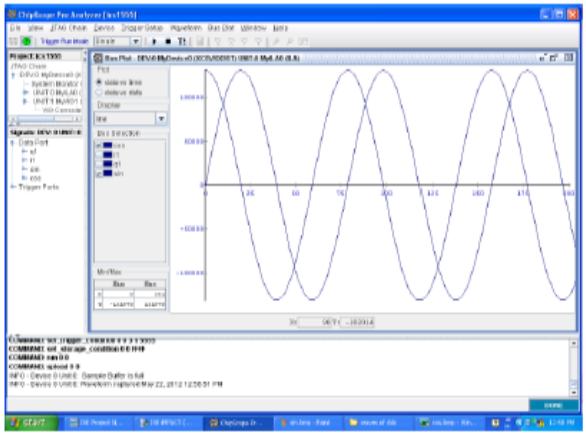

Figure 21: NCO output result from Chipscope Pro Analyzer

Figures 22 and 23 show the I-Mixer and Q-Mixer output from Chipscope Pro Analyzer.

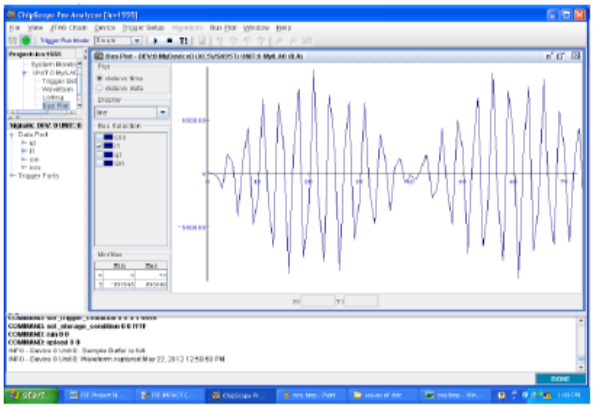

Figure 22: I-Mixer output result from Chipscope Pro Analyzer

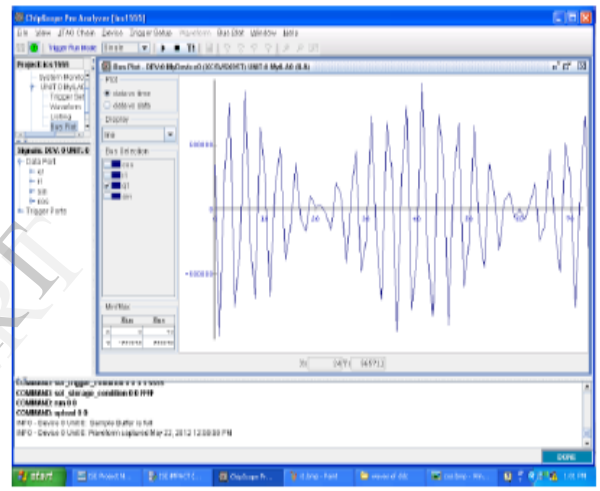

Figure 23: Q-Mixer output result from Chipscope Pro Analyzer

Figure 24 shows the output result observed using Chipscope Pro Analyzer.

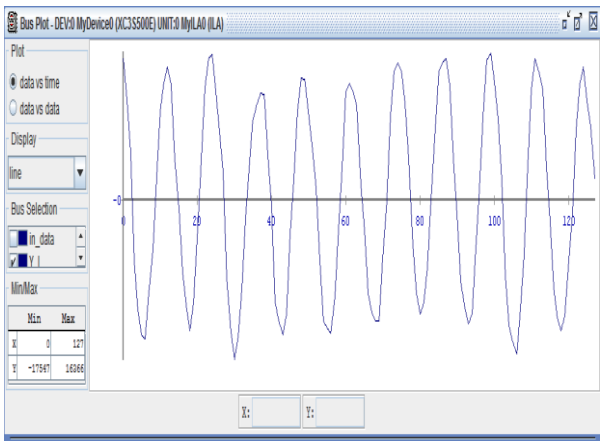


Figure 24: I-Channel DDC output result from Chipscope Pro Analyzer

## V. CONCLUSION

In this paper, we have presented the design and implementation of Digital Down Converter for an IF signal of 5.5MHz.

The DDC is successfully designed in Xilinx ISE Design Suite 12.4 platform with Verilog HDL. The design is simulated for functionality by using Xilinx ISE simulator tool and implemented on Xilinx Virtex-5 XUPV5LX110T FPGA board. The synthesized DDC has 28567 LUT slices, 4960 slice registers and 32 DSP48Es. Timing analysis show that the critical path is 2.329ns i.e., maximum clock frequency is 429.369MHz.

An extension to this work, we can extend single channel DDC to multi-channel DDC and implement the function as it is with using single ADC at the input.

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