FPGA Implementation of MMS Transceiver Using CDMA

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Abstract

This paper presents efficient architectures for IS-95B CDMA Transceivers are modeled and optimized for hardware implementation on FPGA. The efficiency of the transceivers is improved by incorporating Spread Spectrum Analysis, developed for mobile communication for transmitting and receiving of MMS. The spread spectrum analyzer improves the performance of the transceivers at lower SNR levels. The architecture applies a new schema implementing viterbi decoder and thereby results in reduced computation operations on memory requirements. The model is implemented in Xilinx Vertex-II FPGA chip using Verilog Hardware Description Language. The MMS can be transmit and receive in CDMA technology by implementing the FPGA. The FPGA device delivers a satisfactory performance with a reduction in memory and with maximum net delays within the allowable limits of the maximum rate of 9.6Kbps.

This project will be implemented using Verilog Hardware Description Language. Simulation will be done to get the NETLIST. Simulation and Synthesis can be done using Xilinx tools.

Keywords*: IS-95B CDMA, Interleaver, Viterbi Decoder, Field Programmable Gate array (FPGA), Verilog HDL*

1. Introduction

Wireless communication is enjoying its fastest growth period in history due to enabling technologies which permit widespread deployment. Cellular technology has grown tremendously, both in terms of traffic and the services it offers. One of the most promising cellular standards is the IS-95B Code Division Multiple Access (CDMA) system. The advantages of IS-95A CDMA standard over other standards are Optimum subscriber Station Power Management, Bandwidth Recycling, Efficient Power Control, Provision of Soft handoffs, Multi Layered Diversity and Compatibility with variable rate vocoders Service providers are deploying these systems in their markets, where there are mounting demands for higher capacity. The forward link frequency is in the range of (869-894) MHz and the reverse link frequency is in the range of (824-849) MHz In Mobile Communication transmission from the base station to mobile receiver are on the forward link and the transmission from the mobile user to the base station are on the reverse link.

Cellular technology has grown tremendously both in terms of traffic and services, the need for data high speed data transmission has increased. The mobile telecommunication industry faces the problem providing technology that is able to support a variety of services ranging from voice communication with a bit rate of few Kbps to wireless multimedia in which bit rate up to 2 Mbps. This tremendous growth has also been fuelled by the recent improvements in the capacity of wireless links due to the use of multiple access techniques. The idea is to transmit signals simultaneously through a linear band limited channel without inter channel or inter symbol interference

In the recent years the IS-95B CDMA transceivers,
on a FPGA platform has attracted the attention of academic, research and industry community. Most of the reputed literature discusses the design of Traffic channel since the architectures of sync, pilot, and paging channels in the forward link and the access channels in the reverse link are subsets of the traffic channel. A typical Forward Link and Reverse Link Traffic Channel Architectures are shown in figures 1 and 2. The building blocks of a Transceiver consist of Spread Spectrum analyzer, Frame builder, clock master. In this paper a High performance and low cost IS-95B Transceiver is realized by designing a novel spread spectrum analyzer and a frame builder. The complete IS-95B transceiver along with the proposed spread spectrum analyzer is implemented on a XILINX Vertex-II FPGA and tested. The remainder of the paper is organized as follows: Section(2) focuses on proposed Spread Spectrum Analyzer and emphasizes on IS-95B architecture and frame builder Section(3) concentrate on convolutional decoding section(4) focuses on viterbi decoder implementation, Section(5) focuses on Results, FPGA implementation and section (6) focuses on Conclusion.

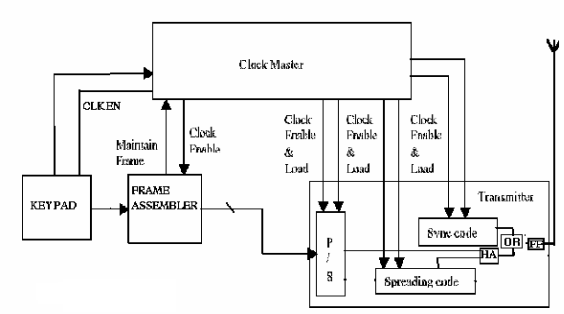


Figure 1.1 Forward link

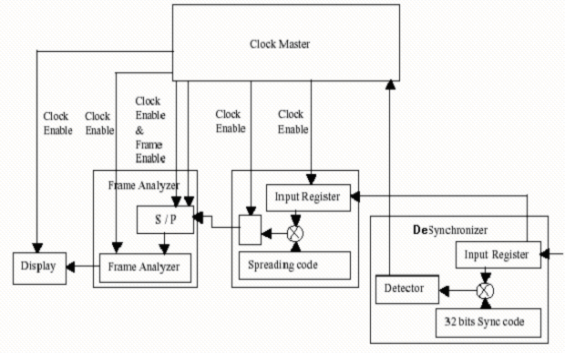


Figure 1.2 Reverse link

2. Spread Spectrum Analyzer

Spread Spectrum (SS) is a technique whereby modulated waveform is modulated (spreaded) a second time in such a way as to generate an expanded –bandwidth wideband signal that does not significantly interfere with

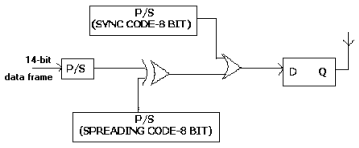


Figure 2.1 Spreading

other signals. The bandwidth expansion is achieved by a second modulation means that is independent of the information message. The applications and potential advantages of spread spectrum systems include the following (1) Improved interference rejection (2) Code division multiplexing for CDMA applications (3) Low-density power spectra for signal hiding (4) High-resolution ranging (5) Secure communications (6) Anti-jam capability (7) Increased capacity and spectral efficiency in some mobile-cellular personal communications system applications

The extensively used techniques in mobile radio systems are (1) Direct-Sequence Spread Spectrum (DS-SS) (2) Frequency Hopping Spread Spectrum (FH-SS)

2.1 Spread Spectrum Algorithm

There are different multiple access schemes for spreading the user data. In this paper direct sequence spreading (DS-CDMA) is used. In DS-CDMA the data signal is directly multiplied by a digital code signal. Spreading Code Selection Criteria i.e. the basic properties of spreading codes are that they have low cross-correlation between the desired and interfering users, and good auto correlation properties to separate the multipath components.

A spreading code can be short or long path delay, the number of users, cell size, etc. are all factors that influence the selection of short or long code. When the number of users is small, and the codes are very short, we focus more on the maximum correlation property when choosing the spreading code to minimize the maximum peak even cross-correlation. Orthogonal codes like Walsh codes are used in our design.

A tree structured orthogonal codes are shown in figure 2.1.

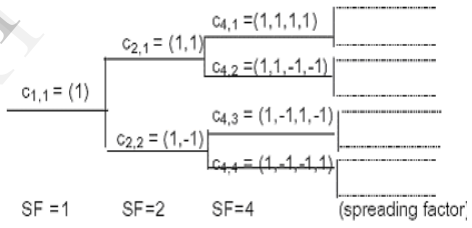


Figure 2.2 Tree structure

The spreading signal is a Walsh code sequence that has a chip rate which is orders of magnitudes greater than the data rate of the message.

All users in CDMA system use the same frequency and may transmit simultaneously. Each user has its own Walsh codeword which is approximately orthogonal to all other codes. The receiver performs the time correlation to detect only the specific desired codeword. All other codeword appear as noise due to decorrelation. For detection of the message signal the receiver needs to know the codeword used by the transmitter. Each user operates independently with no knowledge of the other users.

Channel data rates are very high in CDMA systems. Consequently, the symbol (chip) duration is very short and usually much less than the channel delay spread. Since Walsh sequences have low auto-correlation, multi path which is delayed by more than a chip will appear as noise. A RAKE receiver can be used to improve reception by collecting time delayed versions of the required signal. In CDMA there is no absolute limit on the number of users. Multi path

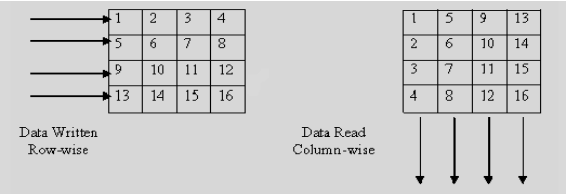
fading may be substantially reduced because the signal is spread over a large spectrum.

2.2 IS-95B for 2.5G CDMA

A cellular system based on Code Division Multiple Access (CDMA) was developed by Qualcomm, Inc. And standardized by the Telecommunications Industry Association (TIA) as an Interim standard (IS-95). This system supports a variable number of users in 1.25MHz wide channels using direct sequence spread spectrum.

`Code division multiple access systems are an extension of direct-sequence spread-spectrum (DS-SS) and frequency-hopped spread-spectrum (FH-SS) systems. They provide multiple access capabilities. In CDMA each user is provided with an individual, distinctive pseudo noise (PN) code. If these codes are uncorrelated with each other then with in the same mobile cell k independent users can transmit at the same time and in the same radio bandwidth. The receivers decorrelate (despread) the information and regenerate only the desired data sequence.

In IS-95B CDMA architecture an Intra-frame Rectangular Block interleaving is performed on each frame length. It writes in column wise and reads out row wise. It maintains 2 memory pages of size (16 x 24) each. When one is being written on, the other is read out. Each page contains a single instance of data for one 20 ms frame. Conceptually bits are written in to a two dimensional matrix row wise and read it from column wise. The mitigating burst errors to improve error correction when the symbols are decoded at the receiver.



2.3 Frame Assembler

The digital signals are easy to transmit and less affected by noise. Each 16-bit stream is compressed to a data stream of 4-bit which is then converted to 14-bit frame by the frame assembler and then transmitted. The frame assembler module builds a 14-bit frame which comprises of an Header (4bits), selector (2bits), user1 data (4bits), user2 data (4bits) in order as shown in figure 2.3.

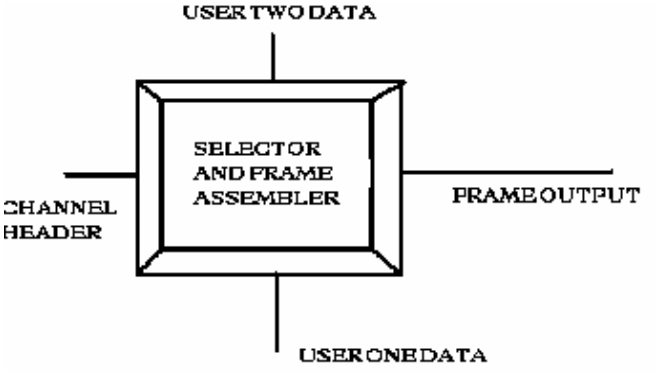


Figure 2.3 Frame Assembler

2.4 Channel Header

The channel Header is a 4-bit segment of the frame. The channel could be any of the following:

REQ	0011
ACK	1100
Communication 1-2	1010
Communication 2-1	0101
Closed	0111

2.5 User Data

The data section of this frame will be used in order to exchange data between user1 and user2. The input compressed data is given to the frame assembler where the Header & user2_data are assembled with the user1_data 14-bit data is out for transmission. The protocol layers used to generate this frame is illustrated in figure 2.4.

Link Access Layer ; generate sync code; generate frame
MAC: Assemble user data, channel Header
Physical Layer; Spreading

Figure 2.4 Protocol Layers

The Link access Layer generates the synchronous code and the frame. The Medium Access Layer (MAC) assembles the user data of channel header to frame. The Actual transmission of data frame via CDMA is the responsibility of the user support Physical Layer.

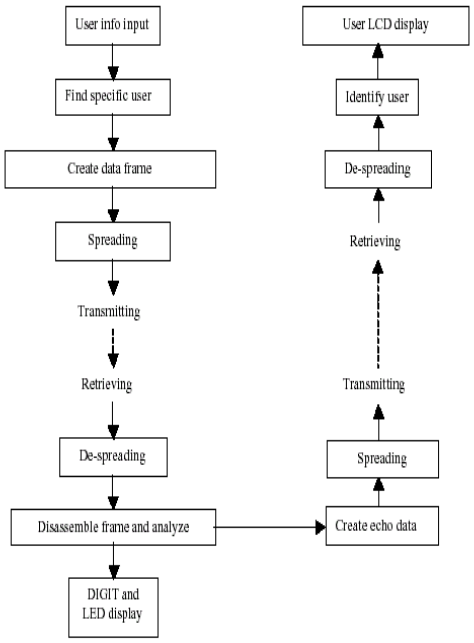


Figure 2.5 Communication

3. Convolutional Decoding

The Viterbi algorithm is commonly used for decoding the convolutional code, a widely used channel decoding techniques. The Viterbi algorithm is to find a maximum-likelihood sequence of state transitions, equivalently a path, in a trellis by assigning a transition metric to possible state transitions. A transition metric is called a branch metric, and the cumulative branch metrics along the path from the initial state to a given state is called the path metric of the state. When two or more paths end at the same state, the path with the smallest (or largest) path metric is selected as the most likely path. The survivor path obtained by back tracing in time corresponds to the decoded output. The configuration of the convolution codes is disparate in each communication standard which imparts different requirements of the viterbi decoder. Thus a reconfigurable Viterbi decoder with low power consumption and high throughput is a key challenge for future portable devices. Viterbi decoding has the advantage that it has a fixed decoding time but its computational requirements grow exponentially as a function of the constraint length, so it is usually limited in practice to a constraint lengths of K = 9 or less. The recent related works reveal that the implementation of the Viterbi decoder on FPGA is certainly a contemporary issue. The authors have implemented a systolic array based Adaptive Viterbi decoder with constraint length 9 and a code rate of ½ using XILINX Virtex-II FPGAs. In a Reconfigurable Viterbi decoder based on an area efficient Add-compare-select (ACS) Architecture with constraint length varying from 7 to 10 implemented using Xilinx Virtex device is presented. In another Reconfigurable Viterbi fabric with constraint length ranging from 3 to 9 and code rate of ½ - 1/3 is implemented using Xilinx Virtex-II FPGA device. Conventional Viterbi decoders, those discussed above suffers from the fact that they require enormous amount of memory. The memory wasted is due to the storing up of error metric at each state and at each level. The wastage can be avoided by the proposed scheme.

4. A New-Fangled Scheme for Viterbi Decoder Implementation

The Viterbi decoder that decodes the convolutional encoded data with a rate of *k/n* (Number of bits into convolutional encoder (k)/ number of bits in output symbol (n)) constraint length K and frame length L bits consists of the following three functional units.

_ Encoder Engine
_ Branch metric generator
_ Add-Compare-Select (ACS) unit and

Three RAM Tables

_ Branch and Path Metric Memory
_ Present State Memory
_ Survivor Memory

The encoder Engine replicates the Convolutional encoder at the receiver and calculates the next state and the output for the various given states and inputs simultaneously. This reduces the memory requirement of the entire trellis structure. 2*2(k-1)*n XOR operations are performed with the received n bits and the generated output n bits at each of the 2(k-1) states in the branch metric unit. Parallel architecture is used to enhance the speed of the decoder Branch metric unit is used to calculate branch metrics. The branch metrics are difference values between received code symbol and the corresponding branch words from the encoder trellis. The Path Metric Unit calculates new path metric values and decision values. Because each state can be achieved from two states from the earlier stage, there are two possible path metrics coming to the current state. The Path Metric Unit adds the branch metric to path metrics and typically selects the smaller one and makes decision. The Path Metric Unit stores the result of the addition as path metric for current state. An Add Compare Select (ACS) unit receives two branch metrics and path metrics. It adds each incoming the corresponding path metric and compares the two results to select a smaller one. The path metric of the state is updated with the selected one. An ACS unit can be time-shared between multiple modules, but it incurs more power dissipation due to the control circuitry. Survivor Path Memory stores the survivor path of each state selected by the ACS module. The number of registers used in this memory is equal to the number of states (i.e. 2(k-1)) in the Convolutional encoder. Each register is used for storing each survivor path. The algorithm could be still improved in a field where the probability of error could be pre-estimated. In such a case a threshold could be fixed and if a path

metric exceeds the threshold, it could be eliminated, thereby conserving space and computation time

5. Results

5.1. Simulation

The main objective of this paper is to implement the IS-95B transceiver inside a single FPGA. The Verilog coding for all the modules were done and simulated. This Verilog HDL is a general purpose hardware description language that is easy to learn and use. This language allows different levels of abstraction to be mixed in the same model. Model technology's powerful new version of its industry-leading HDL simulation tool, ModelSim 5.5, is aimed at today's multimillion gate ASIC and FPGA designs. ModelSim 5.5 offers significant enhancement in memory utilization, interactive debug features, test bench and regression test support, and offers substantial performance improvements for Verilog. The Simulation results for Power control scheme, Convolutional encoder, CRC generators, Walsh Code generator, Data burst randomizer, Block interleaver and Viterbi decoder can also observe. The comparison results between the conventional Interleaver and the proposed Interleaver is shown, the first distance is the number of bit positions by which the consecutive input bits are separated (at the output). The second distance is the number of bit positions by which the alternate input bits are separated and so on. From this it is clear that the proposed interleaver is superior than regular Rectangular window. A simulation graph, comparing various N mod M interleavers with respect to Distance is also included. The Memory requirement of the Conventional Viterbi Decoder and the Proposed scheme are compared for various values of constraint length with convolutional encoder rate 1/2 and 1/3 is illustrated. For Conventional Viterbi decoders, when we change the code rate from ½ to 1/3, the memory requirement (Bits required) increases rapidly with the increase in value of Constraint length. But for the proposed decoder even for the change in code rate from ½ to 1/3, the memory requirement value increases slightly. So the Proposed interleaver is adaptable for different rates of convolutional encoding.

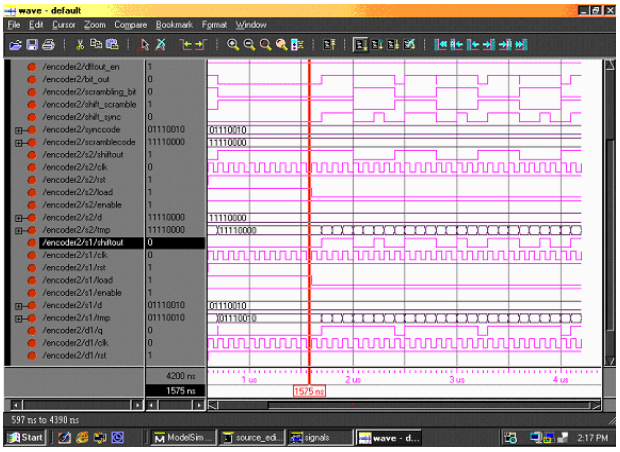


Figure 5.1 Simulation report for transmitter

5.2. FPGA Implementation

The target device chosen for implementation is
XILINX Virtex-II FPGA family chip. The IS-95B CDMA
Transceiver at the Base station and at the Mobile station is implemented in VIRTEX-II FPGA family chip. The implementation results for the transceiver architectures at the Base station and at the mobile units are provided. The FPGA hardware uses 88% of a 1200 slice VIRTEX-II FPGA device and delivers a satisfactory performance with a reduction in memory by 7.6% (for encoder rate 1/2),40.9% (for encoder rate 1/3) and with maximum net delays much within the allowable limits of maximum data rate of 9.6Kbps. Also the comparison results for the proposed interleaver with conventional interleaver in terms of SNR Vs BER. The conventional interleaver will have 0.15 BER and the proposed interleaver will have only 0.087 Bit error rate(lesser than conventional interleaver). Thus the proposed Interleaver improves the performance of the transceivers at lower SNR levels. Also the architecture applies a new-fangled scheme for implementing Viterbi decoder and thereby results in reduced computation operations and memory requirements.

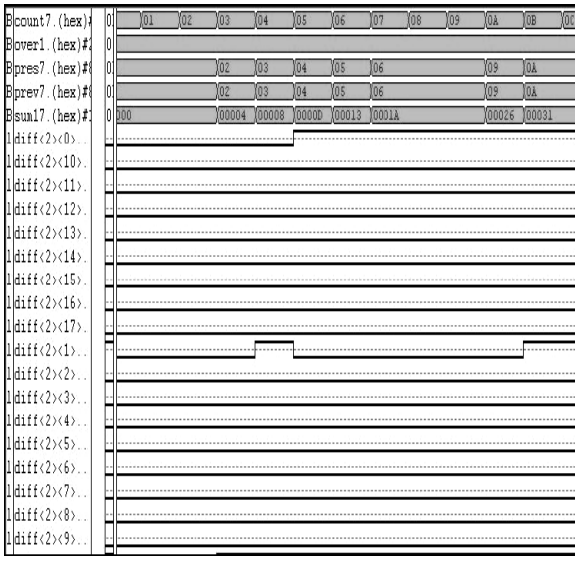


Figure 5.2 Simulation for Power Control Scheme

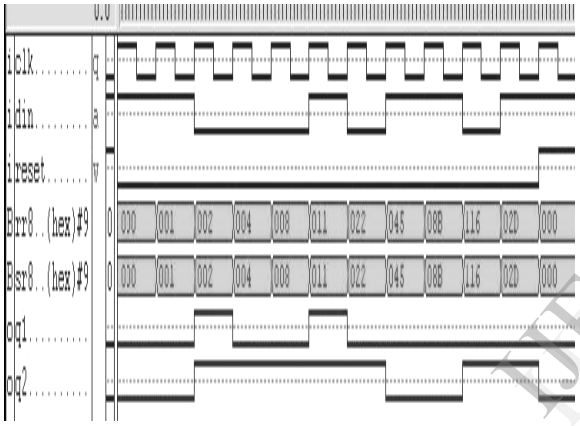


Figure 5.3 Simulation for convolutional encoder

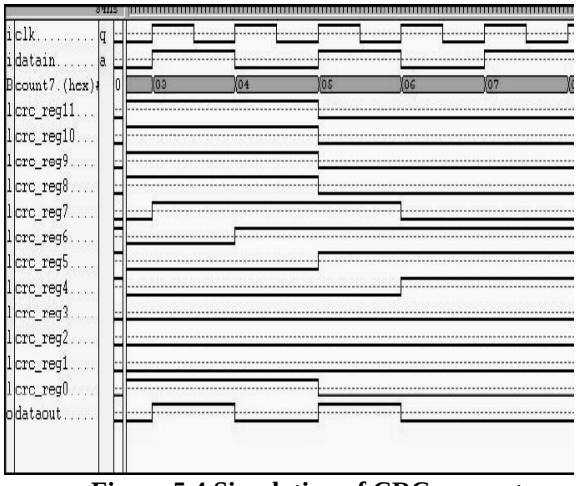


Figure 5.4 Simulation of CRC generator

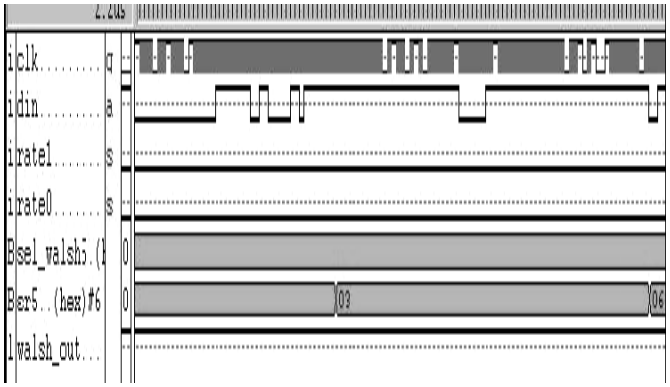


Figure 5.5 Simulation Results of Data Burst Randomizer

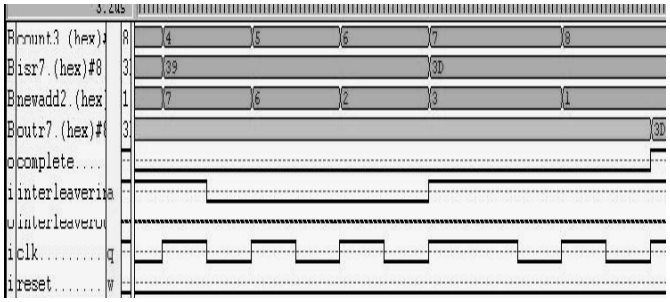


Figure5.6 Simulation Results of interleaver

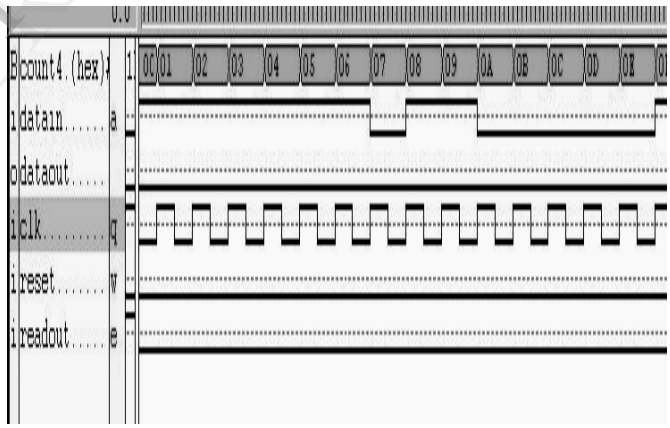


Figure 5.7 Simulation Results of Viterbi Decoder

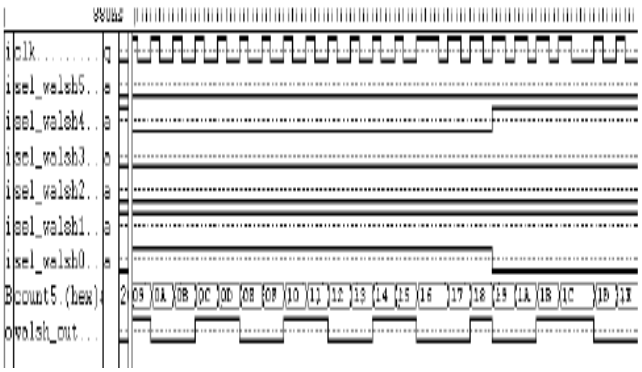


Figure 5.8 Simulation results of Walsh code Generator

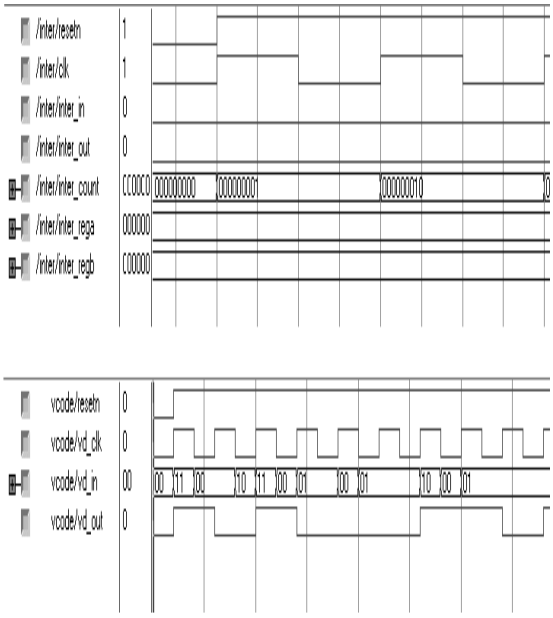


Figure 5.9 Simulation Results of the Proposed Interleaver and the Proposed Viterbi Decoder

6. Conclusion

The design scheme is top-down following the hierarchy tree. Speed, resource Stability and testability are the four main concerns in our design experiments. Centralized control is adopted here rather than distributed control to meet resource requirement. Pipelines are used in some components to meet the speed requirement. Only one globe system clock and one globe reset are used in the design for the consideration of stability.

The future enhancements that may be incorporated. Here we have used single user for the transmission and we can communicate for multiple users. The IS-95B CDMA for forward link and reverse link written in Verilog has been presented. An optimum FPGA implementation of the same has been accomplished successfully. From the BER vs E/No analysis it is studied that the interleaver proposed in this paper is more efficient than the conventional Block interleaver.

The simulation results substantiated the successful implementation of the various modules discussed
earlier and the implementation in FPGA ensure that the chip will work after fabrication. FPGA implementation results in terms of decoding speed, resource usage and BER have been obtained using a tailored test bench. The paper will be extended to 4G Technology in the near future and the design could be worked on reducing power consumption

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