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FPGA Implementation of Multi-DDS System for Magnetic Resonance Imaging Transmitter

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***Abstract*—Digital Up-conversion is the core technology in digital Magnetic Resonance Imaging (MRI) transmitter. With the demand on the performance and functionality of digital MRI transmitter increases highly, it is particularly necessary to develop high-efficient up-conversion technology. Multi-DDS system proposed in this paper combines parallel processing thinking with theory of Direct Digital Synthesizer and utilizes the simultaneous operation of multiple traditional DDS unit. Meanwhile, it takes advantage of rich logic resources in FPGA to achieve IF signal with large bandwidth, high sampling rate on a low clock hardware platform. The proposed system is designed using Xilinx System Generator (XSG). This architecture offer an alternative through a graphical user interface that combines MATLAB, Simulink and XSG and explore important aspects concerned to hardware implementation.**

Keywords—Digital Up-conversion; MRI; high-efficient; parallel processing; Multi-DDS system; Xilinx System Generator; MATLAB; Simulink

I. INTRODUCTION

Depending on its flexibility, small size and low development costs, digital MRI transmitter is widely used in the field of MRI signal processing. The traditional MRI signal transmitting process includes the generation of the base-band signal, modulated to the intermediate frequency, digital-to-analog conversion, modulated to a radio frequency and antenna transmits. Wherein the steps of generation of the base-band signal, modulated to the intermediate frequency and digital-to-analog conversion are implemented by digital MRI transmitter. Fig.1 shows the traditional digital up-conversion process.

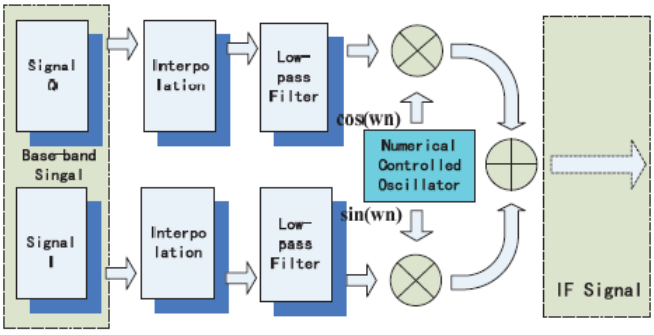

Fig. 1 Traditional digital up-conversion process

Nowadays, with the demand for high performance and functionality digital MRI transmitter, especially the increasing requirements on resolution and real-time system in imaging, the large bandwidth base-band signals have been put to use. At the same time, in order to make the digitizing hardware to meet the requirements, ultra high-speed ADC / DAC and digital processing chip must be used which will face a lot of challenges both in techniques and costs. In order to take advantage of limited hardware resources to achieve higher indicators of digital MRI transmitter, this paper pays attentions on the critical multi-DDS technology in high-performance digital up-conversion. And it implements this algorithm on FPGA hardware platform. High-efficient digital up-conversion processing which is based on multi-DDS technology is shown in Fig.2.

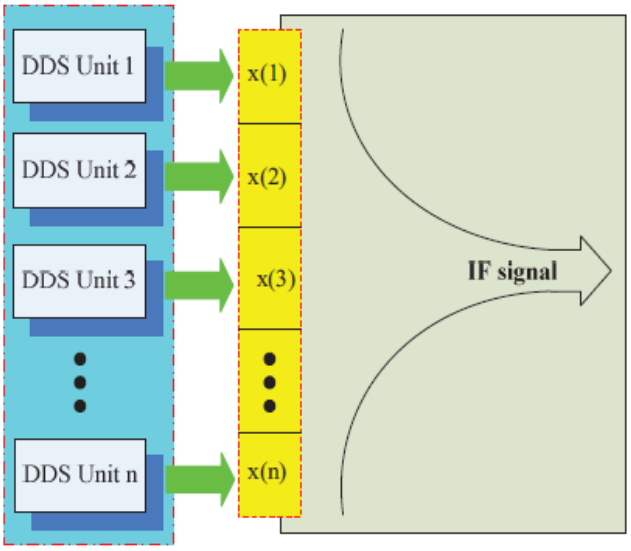

Fig. 2 High efficient digital up-conversion processing

II. XILINX SYSTEM GENERATOR

Xilinx System Generator (XSG) is an integrated design environment (IDE) for FPGAs, which uses Simulink, as a development environment and is presented in the form of blockset. It has an integrated design flow, to move directly to the configuration file (*. bit) necessary for programming the FPGA.

One of the most important features of Xilinx System Generator is possessed abstraction arithmetic that is working with representation in fixed point with a precision arbitrary, including quantization and overflow. You can also perform simulations both as a fixed point double precision. XSG automatically generates Verilog code and a draft of the ISE model being developed. Make hierarchical Verilog synthesis, expansion and mapping hardware, in addition to generating a user constraint file (UCF), simulation and testbench and test vectors among other things.

Xilinx System Generator was created primarily to deal with complex Digital Signal Processing (DSP) applications, but it has other applications like the theme of this work. The blocks in Xilinx System Generator operate with Boolean values or arbitrary values in fixed point, for a better approach to hardware implementation. In contrast Simulink works with numbers of double-precision floating point. The connection between blocks Xilinx System Generator and Simulink blocks are the gateway blocks. Fig. 3 shows the design flow.

Fig. 3 XSG Design Flow

III. BASIC DDS SYSTEM

Direct Digital Synthesizer (DDS) usually refers to look-up table (LUT) based sinusoid generators. A DDS is a technique to generate frequency- and phase-tunable output signals. It uses digital data processing blocks with a fixed-frequency precision clock to generate a sinusoidal signal. Fig. 4 shows the basic structure of single DDS unit.

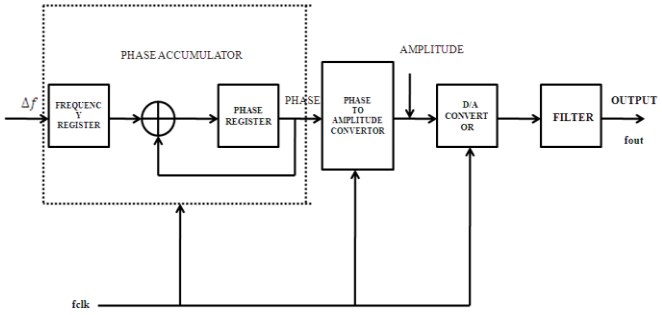

Fig. 4 basic structure of Single DDS unit

The main part of the DDS system is the phase accumulator whose contents are updated once on each clock cycle. Each time the phase accumulator is triggered, the tuning word or phase increment, Δf is added to the contents of the phase accumulator. The 'phase wheel' can be visualized as a vector rotating around the phase circle as illustrated in Fig. 5.

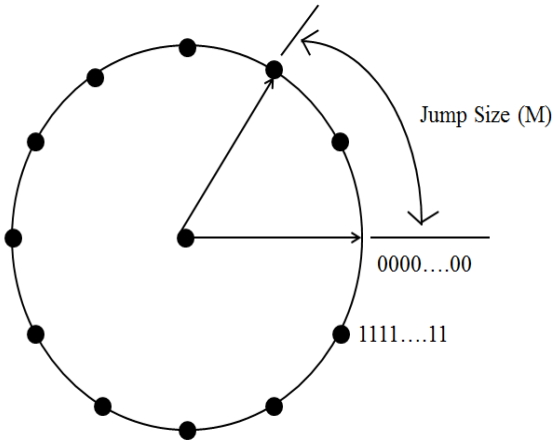

Fig. 5 Digital Phase wheel

In Fig. 5, every point of the phase wheel corresponds to the sample phases of a full sine-wave. When the vector rotates around the wheel, a phase accumulator is visualized to generate equivalent phases of a sine-wave signal. One revolution of vector rotation of the phase wheel at a constant speed produces a finished cycle of an output sine-wave. The revolution of the phase wheel represents an overflow in the phase accumulator. Nevertheless, this complete output sine-wave is linear and is unsuitable to be applied directly to generate a sine-wave signal.

Hence, a sine LUT is used to convert the output phases to sine-wave digital amplitudes. A DAC chip is then used to convert these amplitudes to an analog signal.

The magnitude of phase increment is based on the frequency tuning word Δf. This frequency tuning word forms a 'hopping' process to skip the N-bit phase points of the phase wheel. These N-bit phase points are known as phase step size or phase jump size. The control over the jump size constitutes the frequency tuning resolution of the DDS system. The larger the jump size, the faster the phase accumulator overflows to complete the generation of a sine-wave cycle. Any changes in the frequency tuning word result in immediate changes in the output frequency. The output frequency is inversely proportional to the number of samples per cycle. When the output frequency increases, the total samples per unit cycle decrease.

However, the Nyquist sampling theory dictates a complete sine-wave must have at least two samples per cycle to construct the output waveform. Thus, the maximum frequency of an output sine wave is half of the DDS system clock.

In summary, the frequency of a sine-wave signal can be expressed by the equation below:

$$f_{out} = \frac{\Delta f}{2^N} f_{system} \quad (1)$$

$$\Delta f = \frac{f_{out} \times 2^N}{f_{system}} \quad (2)$$

f_{out} = the frequency of an output sine wave signal
Δf = frequency tuning word
N = N-bit of a phase accumulator
f_{system} = system frequency

Thus, to generate a signal with larger IF frequency a DAC chip with greater conversion rate is required. That requests FPGA clock to reach beyond 250MHz which is very difficult to achieve in practical applications. To solve this problem, we combine the parallel processing thinking with DDS theory and propose a multi-phase DDS algorithm. By this way the large bandwidth IF signal can be generated directly with low system clock. Although the use of multi-DDS technology will occupy more hardware resources, it generates IF signal which means signal modulation and filtering processes are omitted. So the utilization of system resources is still very high.

IV. PROPOSED DESIGN

An 8-core DDS module does not really contain eight individual DDS cores. It is labeled as an 8-core module because it generates eight samples at a time. The productivity of the 8-core DDS system is similar to the system formed by eight DDS cores. The benefit of using an 8-core DDS module is that it composes a sine-wave with 8 times more samples than a single DDS core system.

The 8-core DDS module as shown in Fig. 6 has three major parts. The first part on the left is a phase register used to calculate the frequency tuning word for phase increment. The second part is a 2 GHz DDS system that performs phase accumulation and phase-to-amplitude conversion. The final part on the right is a mock system of a Digital to Analog Converter (DAC) chip, which is used to construct the sine-wave. The DAC block is not really a digital-to-analog converter. It is a pseudo module used to receive de-interleaved samples from DB0 and DB1. In the DAC block, these de-interleaved samples would be reconstructed as a complete sine-wave to SINE output port.

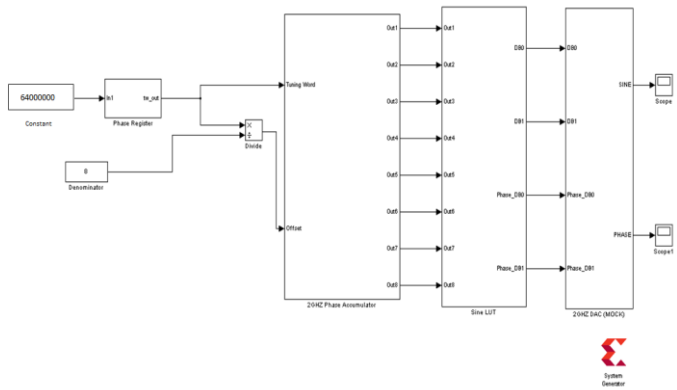

Fig. 6 Simulink model of 8-Core DDS system

A. Phase Register and minimum phase offset calculation

The phase register is used to calculate the frequency tuning word based on the output frequency. Here output frequency is chosen as 64MHz which is the resonance frequency for MRI transmitter. The phase register block contains a mathematical equation for calculating the frequency tuning word of an output frequency. For example, the frequency tuning word for a 64 MHz sine-wave is Δf = 8589934.Further the eight phase offsets are generated and are given as input to the phase accumulator.

B. Phase Accumulator

The phase accumulator block has eight adders as shown in Fig. 7. Each adder outputs a sample phase by adding a phase offset with an accumulated phase from the accumulator. The notion of generating eight consecutive sample phases (forming the samples in numerical order) is similar to a DDS system with eight DDS cores operating in parallel.

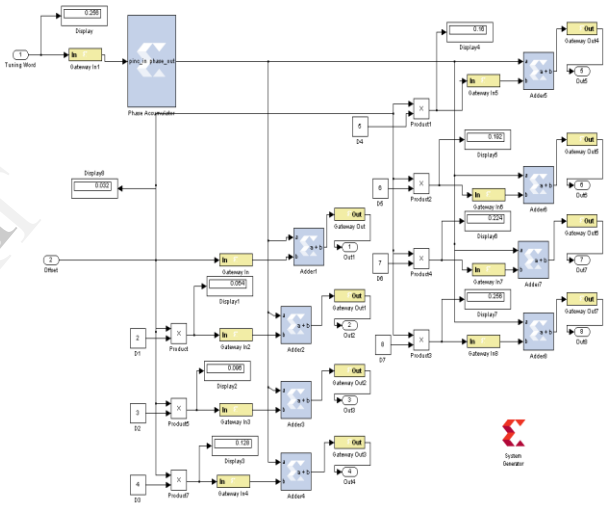

Fig. 7 Phase Accumulator

The phase accumulator generates an accumulated phase on every 250 MHz .The accumulated phase is shifted to eight sample phases by eight phase offsets over a unit time. Therefore, 8 x 250 MHz = 2GHz sample rate is achieved. The simulation results of eight sample phases is shown below in Fig. 8

Fig. 8 Simulation results of eight sample phases

C. Sine Lookpup Table Module

The sine LUT module as shown in Fig. 8 requires four multiplexer blocks, eight LUT blocks and a counter block to build up the system. The reason for using eight sets of sine LUTs is to make sure that the conversion of phases into amplitudes is at the maximum 250 MHz speed.

When a clock is triggered, the counter starts to count in ascending order. The 1st and 2nd samples are transferred to the DAC block through MUX 1 and MUX 3 via d0 when the counter is zero. When the counter counts 1 on the second clock cycle, the 3rd and 4th samples are transferred to the DAC block through MUX 1 and MUX 3 via d1. On the third clock cycle, the counter counts 2. The 5th and 6th samples are transferred to the DAC block through MUX 1 and MUX 3 via d2. Lastly, 7th and 8th samples are shifted out from MUX 1 and MUX3 via d3 when the counter counts 3.

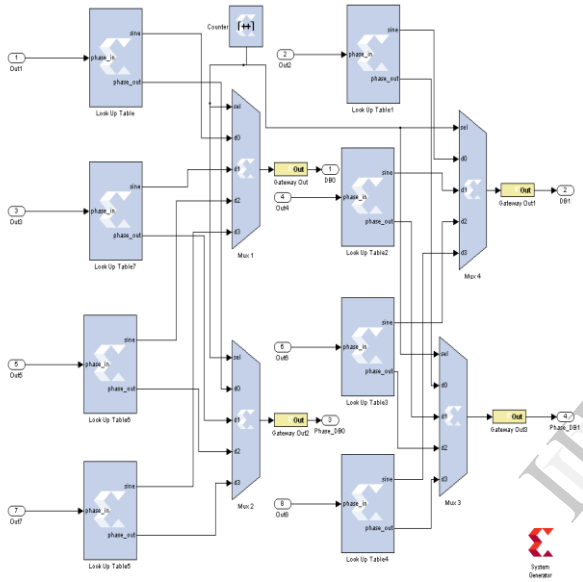

Fig. 9 Sine Lookup Table Module

D. DAC Module (Mock)

The DAC block in Fig. 6 is only a mock module. It does not actually work like a real DAC chip. But it does multiplex four data paths (DB0, DB1, Phase_DB0 and Phase_DB1) into two outputs (SINE and PHASE).

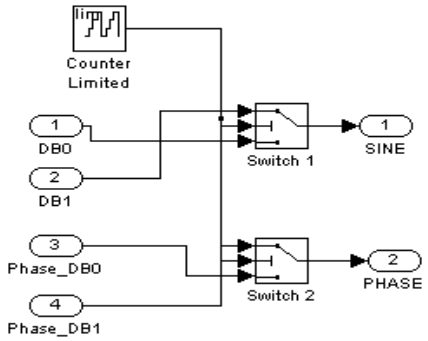

Fig. 10 DAC Module (Mock)

Each data path runs at 1GSPS. Consequently, Switch1 interleaves the data on DB0 and DB1 to a single output on SINE and Switch2 interleaves the data on Phase_DB0 and Phase_DB1 to a single output on PHASE. The switching process doubles up the sampling frequency of 1GSPS to 2GSPS. Matlab plots the results of both SINE and PHASE to provide a clear idea of the relationship between a phase and sine amplitude of an output signal.

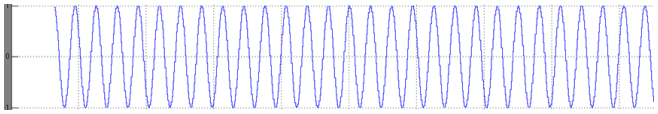

Fig. 11 Simulation result of 64MHz using MATLAB

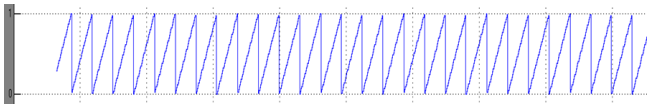

Fig. 12 Phase of 64MHz using MATLAB

V. RESULTS

A. Simulation results

The System Generator tool converts the design of Xilinx blockset based 8-Core DDS system into Verilog HDL. The simulation results of 8-Core DDS system using Xilinx ISE 12.4 tool is shown in Fig. 12.

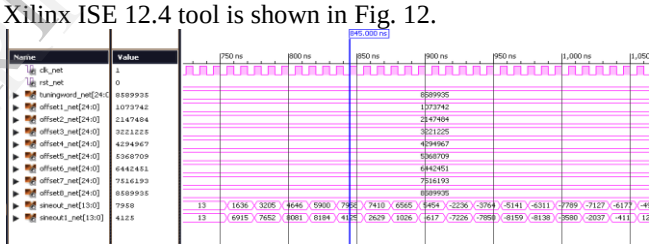

Fig. 13 Simulation results of 8-Core DDS system

B. FPGA Implementation of 8-Core DDS system

In this paper, the hardware platform is based onVirtex5 XCV5lx-110t FPGA from Xilinx Inc. The FPGA works at 250MHz, and utilizes the eight-phase DDS technology to achieve an IF signal of 64MHz frequency with 2GHz sampling rate.

The implementation results are captured using Chipscope Pro Analyzer which is used to verify all the internal signals and nodes within Virtex-5 FPGA board. Fig. 13 shows the bus plot view of Chipscope.

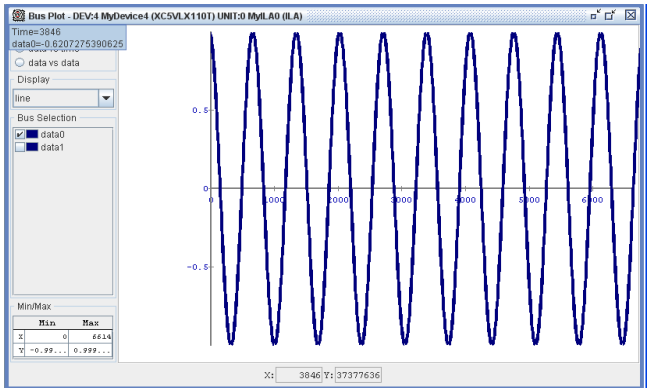

Fig. 14 Bus plot view of Chipscope

VI. CONCLUSION

In this paper, we researched an efficient digital-up conversion process. By using Multi-DDS technology which based on parallel processing, a large bandwidth signal can be produced at a lower hardware clock. Besides that this solution eliminates the need for filtering and modulation process and directly generates IF signal. The program has been implemented in FPGA hardware platform and achieved very good results.Further the proposed system can be able to generate frequencies in the range from 100KHz to 750MHz.

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