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Front End To Back End VLSI Design For Convolution Encoder

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Abstract

For many digital communication system bandwidth and transmission power are limited resource and it is well known that the use of feed forward convolution encoder plays a fundamental role to increasing power and spectrum efficiency. The development of error correction technique with increasing coding gain has a limit, arising from the channel capacity. Convolution code is channel code, which extensively used in communication system.

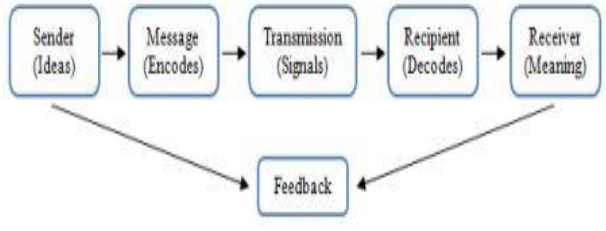
The paper describes in three phases of Feed Forward convolution Encoder. System level design as first phase, containing trellis diagram and state table RTL vie of feed forward convolution encoder also explains timing waveform and parameter require for developing the convolution encoder. Circuit level design using MOS transistor as second phase and then Layout or Physical design of feed forward convolution encoder as third phase and finally explain the application and conclusion.

1. Introduction

This paper is an introductory tutorial on, a new technique of error correction coding developed in the 1990s. The reader is expected to be familiar with the basic concepts of channel coding, although we briefly and informally review the most important terms. The paper starts with a short overview of channel coding and the reader is reminded the concept of convolution encoding. Shannon shows that the development of error correction technique with increasing coading gain has a limit, arising from the channel capacity. Convolutional codes are channel codes, which are extensively used in communication systems like GSM (global system for mobile communications) and Interim standard IS-95.We introduce a strategy to present convolutional codes without using mathematical structures. In this project, we will discuss our method to implement convolutional encoding and Viterbi Algorithm. It is unique design of Convolution Encoder in the all the three phases. The convolution encoder is a circuit that performs the convolution encoding scheme to encode data before transmission over a channel in digital communications system.

2.0 Channel Coding

The main aim of a digital communication system is to transmit information reliably over a channel. The available amount of transmitter power and bandwidth are the major constraints in the design of a digital communication system. The channel can be coaxial cables, microwave links, or fiber optic. The channel is subject to various types of noise, distortion, and interference. Also some communication systems have limitation on transmitter power. All these may lead to errors. Consequently we may need some form of error control encoding to recover the information reliably. Convolution codes are extensively used for real time error correction. The position of the channel encoder is shown in following block diagram of the elements of a digital communication system



Basic dig of convolution encoder

2.1.1Feed forward Error Correction.

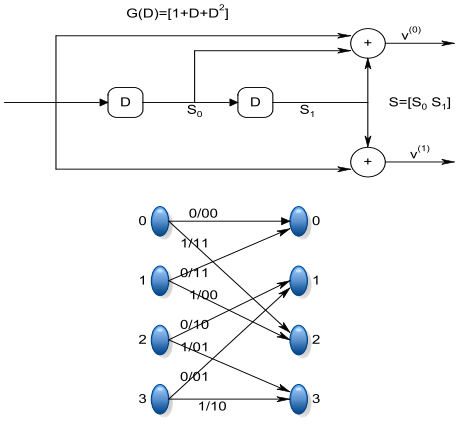
The purpose of forward error correction (FEC) is to improve the capacity of a channel by adding some carefully designed redundant information to the data being transmitted through the channel. The process of adding this redundant information is known as channel coding. Convolution coding and backward coding are the two major forms of channel coding. Convolution codes operate on serial data, one or a few bits at a time. Block codes operate on relatively large (typically, up to a couple of hundred bytes) message blocks. There are a variety of useful convolution and block codes, and a variety of algorithms for decoding the received coded information sequences to recover the original data.

The task of channel coding is to encode the information sent over a communication channel in such a way that in the presence of channel noise, errors can

be detected and/or corrected. We describe only here only feed forward convolution encoder:

2.1.2 Feed Forward Convolution Encoder.

Requires that the encoder should also be capable of correcting a certain number of errors, i.e. it should be capable of locating the positions where the errors occurred. Since Feed forward error correction (FEC) codes require only simplex communication, they are especially attractive in wireless communication systems, helping to improve the energy efficiency of the system. In the rest of this paper we deal with binary FEC codes only.



Feed forward convolution encoder and their state diagram

The above figure shows that the block dig of the Forward error correction with the state diagram form the state diagram the state Table is shown in below. The state Table shows the output of encoder depends on present state and next state.

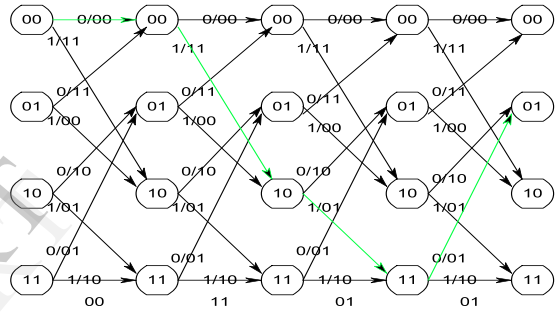
Input U	Present State(S1,S0)	Next State(S1,S0)	Output(V1,V2)
0	00	00	00
1	00	10	11
0	01	00	11
1	01	10	00
0	10	01	10
1	10	11	01
0	11	01	01
1	11	11	10

State table of feed forward Convolution Encoder

The convolution encoder is basically a finite state machine. The K bit input is fed to the constrain length K shift register and the n output are calculated from the generator polynomial by the Modulo-2 addition.

Convolution encoder can be describe for the forward error correction in terms of state table, state diagram and trellis diagram. The state is defined as the contents of the shift register of the encoder. In state table output symbol can be described as a function of input signal and the state. State diagram shows the transition between different state Trellis diagrams is the description of state diagram of the encoder by the time line i.e. represents its time unit with separate states diagram.

The encoding sequence **0110** to the forward error correction and then output sequence is **00 11 01 01** it shown by the dark green line in trellis diag.



Trellis diagram of feed forward encoder

The above diagram shows the trellis diagram of Feed Forward convolution encoder it has the state 00, 01.10 and 11 as the encoder is in present state and the switch to next state then the output has been change suppose the encoder has present state is 00 and it is switch to the next state has a clock signal is 0 the output is 00 and it is represented as 0/00. Similarly the output is same state but the clock signal is 1 then output is 11 and it is represented as 1/11. In this way all the state are shows in the trellis diagram

Since project has three phases System level, Circuit level, and Transistor level design (chip layout).

3.1System Level Design

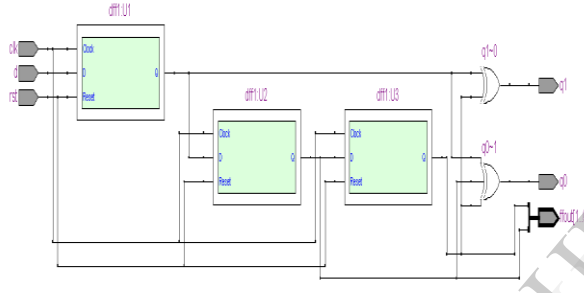
In the first phase of system level design of feed forward convolution encoder Quartus II i.e Qsys system integration tool is used to create design with fast and easy system-level integration. In this we seen the RTL view and the Timing diagram of convolution encoder and analyses the Total logic element, combinational function and dedicated logic resister used in both the cases. Also we have to shows Total Thermal power dissipation, core dynamic Thermal power dissipation and I/O Thermal power dissipation For the feed forward convolution encoder

The RTL View and Technology Map Viewer provide a hierarchy list that displays a representation of the project hierarchy and a schematic view that displays the components of the design element we want to examine. The hierarchy list expands as you navigate through the schematic view. we can also open the implementation of a design instance by double-clicking an instance in the hierarchy list.

In the schematic view, different default colors are used to discern different design elements. For example:

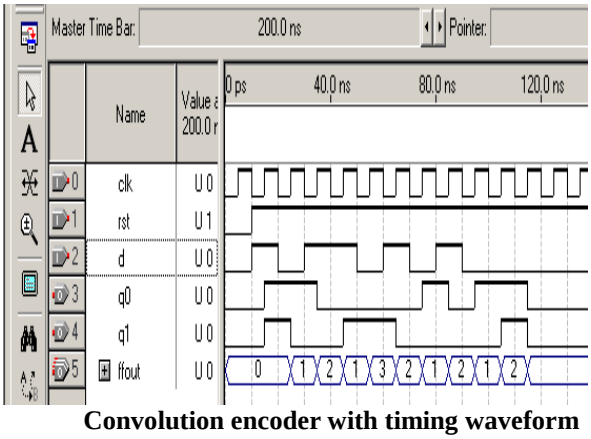
All encrypted design and I/O pins instances appear gray.

- All state machine nodes appear yellow (RTL Viewer only).
- All logic cells and I/O cells for which you can view the underlying internal implementation appear blue (Technology Map Viewer only).
- All RAM blocks and DSP blocks appear blue.
- All other design instances appear light green.



Convolution encoder with RTL

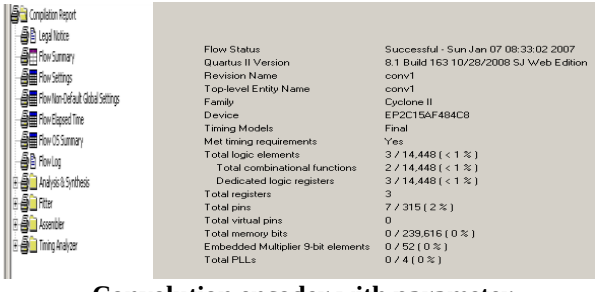
The above figure shows the RTL view of Feed Forward convolution Encoder (FCE). It consists of three FF and two AND gate the logical connection is shown is shown in the above figure. It has three input clk, data and rst (reset) signal and the output is q0 and q1 shown in the figure.



Convolution encoder with timing waveform

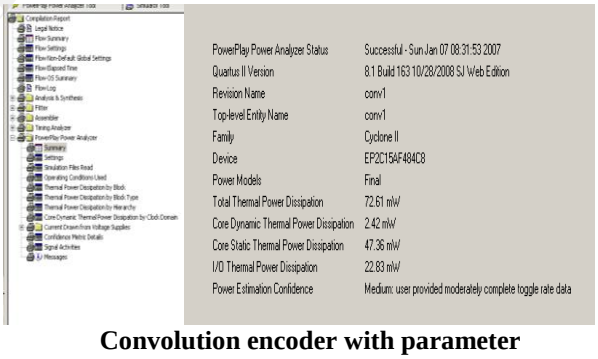
The above figure shows the timing diagram of FCE. The output Q1, Q0 and ffout is depend upon the clk, rst and the data d which is shown on the above fig.

The output Q1, Q0 and FFout is depend upon the clk, rst and the i/p data d (101101) which is shown on the above figure and the respective timing wave form of qois110001 and the output q1 is 100110 where the Reset signal is initiated at falling edge of the first clock signal.



Convolution encoder with parameter

The above figure the parameter used in the FCE in which Total logic element is 1outof 14448 , total combinational function 2/14448 and the dedicated logic register is 3/14448, total pins is 3, total memory bit used used is 0 and other parameter is shown in above table

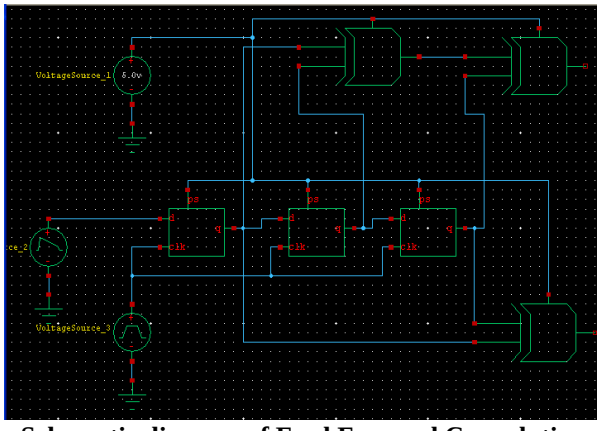


Convolution encoder with parameter

The parameter table 2 shows Total Thermal power dissipation, core dynamic Thermal power dissipation and i/o Thermal power dissipation. for the Feed Forward convolution Encoder.

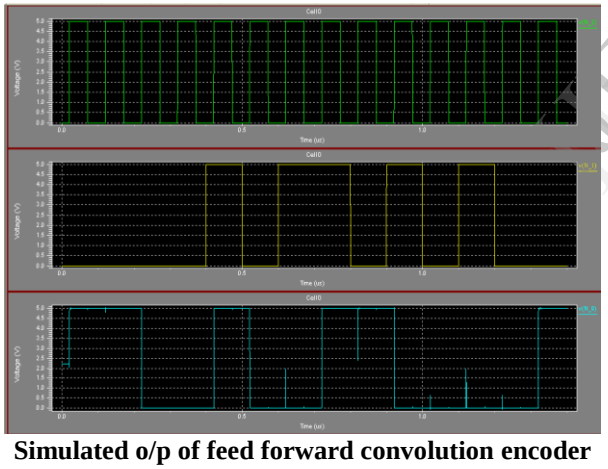
3.2 Circuit Level Design

To design second phase of convolution encode, circuit schematic design Feed forward convolution encoder was not too complicated as it involves a three Flip-Flop, three EX-OR gate, and voltages sources and their connections all of which we were familiar with their workings and their implementation using MOSFETs. Figure shows schematic block of feed forward convolution encoder



Schematic diagram of Feed Forward Convolution Encoder

The above fig shows the circuit level design (using MOS Transistor). It consists of three FF acts as shift resister combine with the EX-OR gate and the output Q1, Q2 shows at the EX-OR o/p. The following fig shows the relevant timing waveform of circuit level design of FCE. This waveform is same as that of convolution encoder at system level design.



Simulated o/p of feed forward convolution encoder

The relevant waveform of circuit level design of Feed Forward Convolution Encoder. The output Q1, Q0 and FFout is depend upon the clk, rst and the i/p data d (101101) which is shown on the above figure and the respective timing wave form of q1 is 100110 where the Reset signal is initiated at falling edge of the first clock signal. From above discussion it is clear that the timing waveform obtained at circuit level design and system level design are same (i.e. in both cases the output q1 is 100110) and hence it clear that the design at both the level is true for same data input for (FEC).

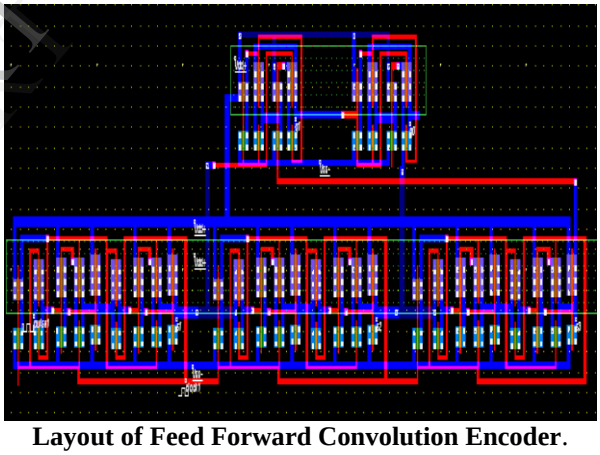
3.3 Transistor Level Design

Ii is the Third phase of design. To developed this stage, it require the cells which are XOR, flip-flop and T-gate. Each of these individual cells were carefully design and optimized for minimal area use in coordination with the desired W/L for the final layout of our chip.

Once the dimensions for each block (XORs, T-Gate, flip-flops) were optimized, we laid them in a higher level cell which included the outline of the maximum size and the six contact pads. We then completed the interconnections, making minor alterations to lower-level cells when necessary.

It should be noted that our submitted layout had the dimensions 221 λ x 222 λ, a subtle, but all the same, a reduction in size compared to the allowed dimensions of 230 λ x 230 λ. This means that our chip has the physical dimensions of 552.5µm x 555µm.

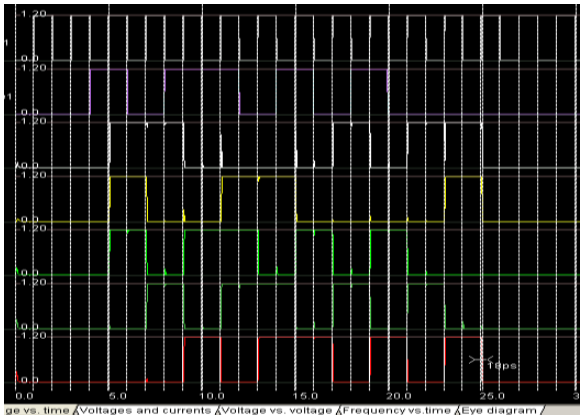
The following figure shows the layout of feed forward convolution encoder.



Layout of Feed Forward Convolution Encoder.

Chip Layout Discussion

Most of the transistors in our layout were of minimal, but properly ratioed, sizes. This design decision was made solely because of area constraints. Our functional blocks occupy a significant amount of space on the chip and, as well, so do interconnects. This decision was rationalized by the fact that we would only be driving a 10pF load and operating this chip at fairly low frequencies (few MHz) and in optimal operating conditions (room temperature). The minimal gate widths make for a slower pull of current, but this was acceptable for our purposes, as long as we ratio our transistors correctly.



Wave form of transistor level design

The above figure shows the relevant waveform of Transistor Level design of Feed Forward Convolution Encoder. The output Q1, Q0 and FFout is depend upon the clk, rst and the i/p data d (101101) which is shown on the above figure indicated by violet line and the respective timing wave form of q1 is 100110 indicated by yellow line where the Reset signal is initiated at falling edge of the first clock signal. From above discussion it is clear that, design at System level, Circuit level and the Transistor level match because the timing waveform at three stage are same or equal (i.e. input data 101101 is applied at all the three phases of design and the output at q1 is 100110 at all the three phases all the circuit design at three stages is match for same data). Hence our aims is true.

4.0 Conclusion:

The contribution of this paper is to provide a simulating tool that teaches efficiently the convolution encoding in digital communication, and wireless communication courses. In this paper we have work on three phases of VLSI Design 1). System Level Design [VHDL coding] 2).Circuit level design using MOS Transistor. 3). Layout or Physical level design and we have found that all three level the relevant waveform are same in feed forward convolution encoder. Hence our aims is true.

5.0 Application:

Convolution code are extensively used in numerous application in order to achieve reliable data transfer , including digital video, radio, mobile communication, and satellite communication with hard decision code

1) A satellite modem or sat modem is a modem used to establish data transfer using a communication satellite as a relay. There is a wide range of satellite modems from cheap device for home internet access to expensive multifunction equipment for enterprise use. A satellite modems main function is to transfer input bit stream to radio signal to vice-versa

2) A Viterbi decoder uses the Viterbi algorithm for decoding bit stream that has been encoded using Forward error correction based on convolution code. The viterbi decoding algorithm is widely used in the following area

Decoding trellis coded modulation (TCM), the technique used in telephone –line modems to squeeze high spectral efficiency out of 3 khz bandwidth analog telephone lines. The TCM is also used in the PSK31digital mode for amateur ratio and sometime in the radio relay and satellite communication

3) Another concern of coding theory is designing codes that help synchronization. A code may be designed so that a phase shift can be easily detected and corrected and that multiple signals can be sent on the same channel

4) Another application of codes, used in some mobile phone systems, is code division multiple access (CDMA). Ea h phone is assigned a code sequence that is approximately uncorrelated with the codes of other phones. When transmitting, the code word is used to modulate the data bits representing the voice message. At the receiver, a demodulation process is performed to recover the data. The properties of this class of codes allow many users (with different codes) to use the same radio channel at the same time. To the receiver, the signals of other users will appear to the demodulator only as a low-level noise.

5) Another general class of codes are the automatic repeat request (ARQ) codes. In these codes the sender adds redundancy to each message for error checking, usually by adding check bits. If the check bits are not consistent with the rest of the message when it arrives, the receiver will ask the sender to retransmit the message. All but the simplest wide area network protocols use ARQ. Common protocols include SLDC (IBM), TCP (Internet), X.25 (International).

6.0 References

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