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Generation of Gaussian Pulses using FPGA for Simulating Nuclear Counting System

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***Abstract*- Nuclear radiation counting system is used for the measurement of the nuclear radiation level by counting the electric pulses, which are produced by the detector. Radiation causes hazard for human being. So before real measurement, it is a safe way to simulate this counting system by similar type of electric pulses generated from detector (GM) like Gaussian Pulses. In this work, internally Gaussian Pulses are generated by FPGA technique using VHDL code and finally Nuclear Counting System is simulated. Initially digital values of Gaussian pulse have been generated in FPGA and controlled by a rotary switch. Then these values are transferred to the input of a DAC through SPI bus. DAC output generates Gaussian pulses and is fed to the input of ADC. When the ADC output value is between higher than lower threshold value Lower Level Detection (LLD) and lower than higher threshold value Upper Level Detection (ULD) then counter counts those values over a period of one second and stores the counting value in register. The LLD & ULD value is set 0.86V to 1.6V respectively and it can be changed depending on requirements. Finally the stored counting values are displayed on LCD. Associate firmware has been developed by Xilinx ISE Design suite 9.2 using VHDL code and tested on Xilinx Spartan 3E Starter board. This technique has low power consumption, high speed and low developing time and cost. So this system can be successfully used for the study of Nuclear Counting System especially for Single Channel Analyzer, Multichannel Analyzer for measurement of radio activity, dose rate, etc.**

Keywords- FPGA, SPI, VHDL, Gaussian pulse

I. INTRODUCTION

The nuclear radiation cannot be detected by human senses. Therefore, an equipment namely, Nuclear Radiation Counting System, is required to detect and measure that radiation level. In this system, when radiation hits to the window of GM detector, then electric pulses are produced as output of the detector depending on the level of intensity of radiation. It was seen that these electric pulses are similar to Gaussian Pulses generated by FPGA. FPGA has entered in almost all fields of electronics from medical instrument to consumer electronics due to its great flexibility to configure hardware by software. The generated Gaussian pulses were displayed, measured and compared by Digital Storage Oscilloscope.

Many researchers have reported their design and application on FPGA based system, MCA and SCA related things. For example A. Ezzatpanah Latifi developed design and construction of an accurate timing Single Channel Analyzer [5]. Amitkumar Singh designed and simulated a system on FPGA Based Digital Multi Channel Analyzer for Nuclear Spectroscopy Application [6]. From this scientific information; the proposed system was focused on a new technology applied in Nuclear Counting System. Since this design is FPGA based which can be reconfigured by software then it takes less time to modify design thus is more flexible than existing counting system.

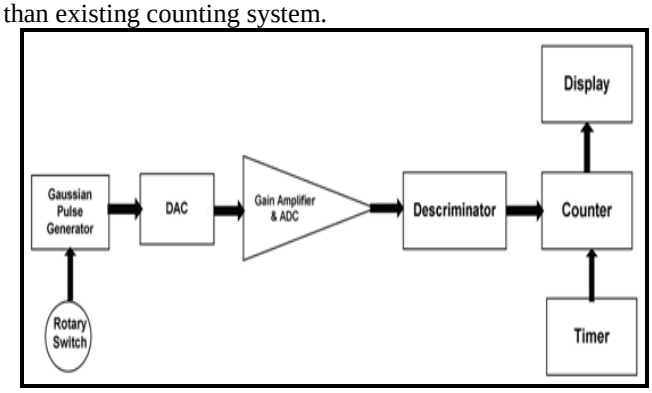

Fig.1. Basic diagram of the FPGA based Nuclear Counting System using Gaussian Pulse

II. DESIGN SCENARIO

Basic Scenario of the designed counting system is shown in Fig.1. The system consists of Gaussian pulse generator, gain amplifier & ADC, discriminator, counter, timer and display unit. Gaussian pulse generator produce Gaussian pulses used as electric pulses, Amplifier is used for two functions, shaping and amplifying these electric pulses. The discriminator produces a TTL logic signal, when the incoming pulse fulfills the energy range criteria, which is defined by the user selectable lower - and upper level. Counters are used for counting the logic signal from the discriminator for certain interval time (counting time). User sets the counting time through the timer in order of seconds, minutes or hours.

In traditional system for Nuclear Counting System design needs individual circuit for amplifier, discriminator, counter and timer but in FPGA based system it is possible to design all these circuits in a single system as an integrated device.

III. SYSTEM METHODOLOGY

In this paper, we present FPGA implementation for designing Gaussian pulse generator, pulse detector works as discriminator, two16 bit counters, bin to BCD counter, LCD driver and pre divider. DAC, ADC & gain amplifier are configured by FPGA. FPGA uses a Serial Peripheral Interface (SPI) to communicate with the DAC, ADC and gain amplifier chip. The designed system was implemented by using ISE foundation 9.2 and VHDL. Fig. 2 shows functional block diagram of Nuclear Counting System.

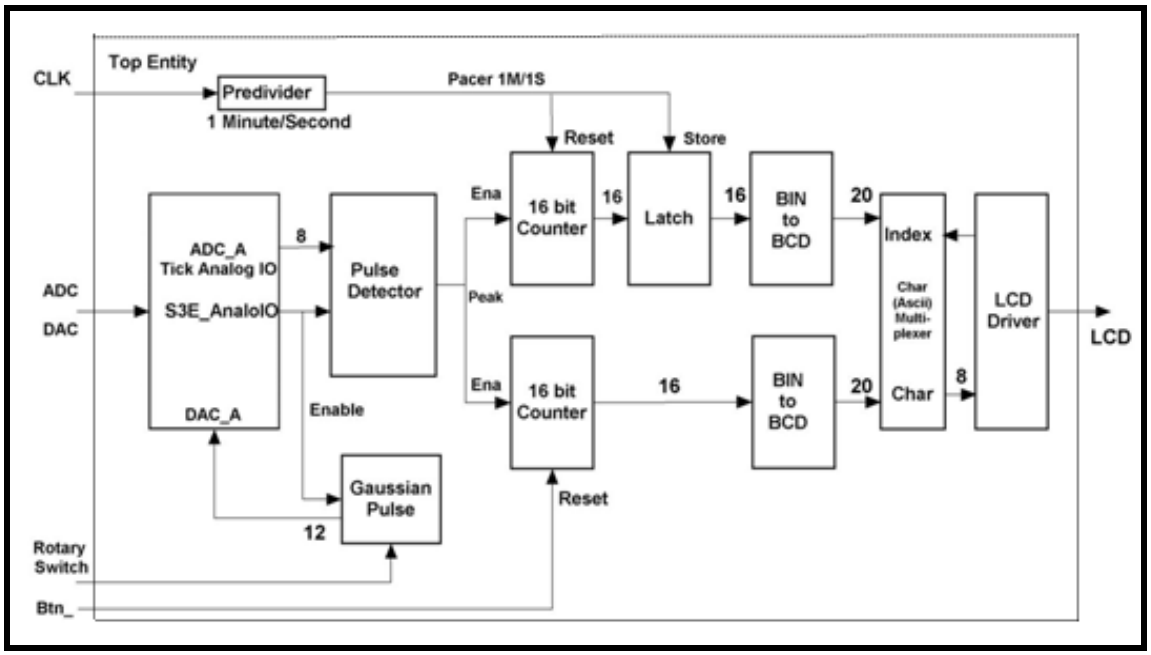

Fig.2. Functional Block diagram of FPGA based Gaussian Pulse Generator & Nuclear Counting System

Specification of components of the Counting System is shown in table I.

TABLE I. Specification of components of the Counting System

Sl. No.	Components name	Quantity	Description
1.	Rotary switch	1	Rotary switch
2.	Xilinx FPGA	1	XC3S500E FG-320Spartan-3E FPGA
3.	DAC		LTC2624
4.	ADC	1	LT1407A
5.	Programmable-gain amplifier	1	LTC6912
6.	Clock oscillator	1	50 MHz Oscillator CLK_50MHz: (C9)
7.	LCD	1	Character LCD
8.	LED	8	Eight discrete LEDs

A. FPGA based Nuclear Counting System

The following section presents a description of the various components of the Nuclear Counting System in fig. 2. These components are configured by FPGA including SPI interface which connects the FPGA to major external devices DAC, gain amplifier and ADC. The other components in the developed system have been designed by FPGA using VHDL code.

B. Gaussian Pulse Generator

Gaussian pulse has been generated in FPGA by VHDL code and the amplitude and frequency of these pulses are controlled by a rotary switch. This Gaussian Pulse is used as electric pulse instead of detector output pulse. This pulse goes out by DAC and then feed to ADC through SPI bus.

The amplitude of this pulse in this design is 0.86V to 1.6V and it can also be varied depending on requirements. The frequency of these Gaussian pulses is varied from 454Hz to 2 KHz. In Fig.3: & Fig.3 shows the Flow diagram of generated Gaussian Pulse and RTL schematic design respectively. The generated pulses were displayed, measured and compared with Digital Storage Oscilloscope.

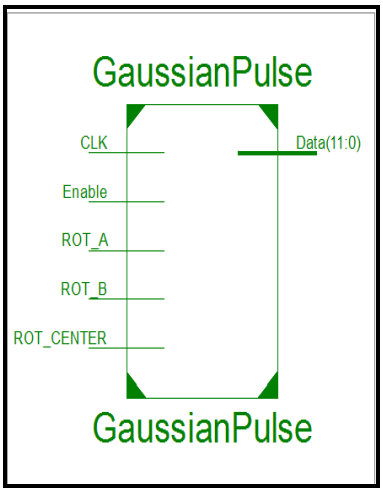

Fig.3. RTL Schematic Design of Gaussian Pulse

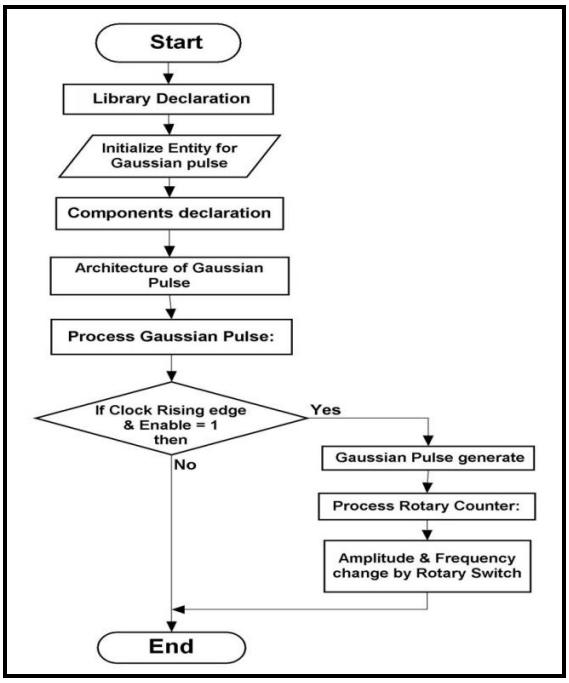

Fig.4. Flow diagram of generated Gaussian Pulse

C. DAC

The DAC device is a Linear Technology LTC2624 quad DAC with 12-bit unsigned resolution. The outputs from the DAC appear on the J5 header (Fig. 5 :). The FPGA uses a Serial Peripheral Interface (SPI) to communicate digital values to DAC channels [1].The SPI bus is a full-duplex, synchronous, character-oriented channel employing a simple four-wire interface. A bus master - the FPGA drives the bus clock signal (SPI_SCK), DAC_CS slave select signal Low and transmits serial data (SPI_MOSI) to the selected bus slave-the DAC. At the same time, the bus slave provides serial data (SPI_MISO) back to the bus master [1].

After transmitting all 32 data bits, the FPGA completes the SPI bus transaction by returning the DAC_CS slave select signal High. The High-going edge starts the actual digital-to-analog conversion process within the DAC [1].

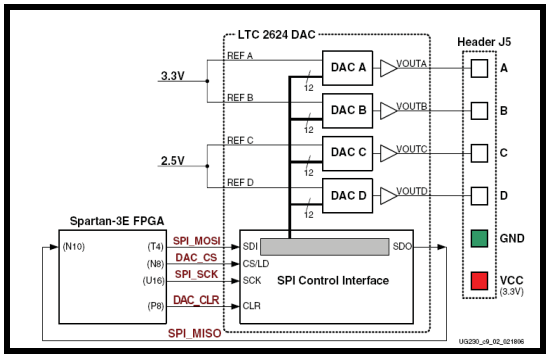

Fig.5. Detail view of DAC [1]

D. Gain Amplifier and ADC

The Spartan-3E Starter Kit board includes an SPI-compatible, two channels Analog-to-Digital Converter (ADC) and a Gain amplifier (programmable scaling pre-amplifier) which works as analog IO.

The analog IO circuit consists of a Linear Technology LTC6912-1 programmable gain amplifier that scales the incoming analog signal on header J7 (Fig. 6). The output of Pre-amplifier connects to a Linear Technology LTC1407A-1 ADC [1]. Both the pre-amplifier and the ADC are serially programmed or controlled by the FPGA. The SPI_MOSI, SPI_MISO, and SPI_SCK signals are the bus interface signals between the FPGA, ADC and the gain amplifier. The AMP_CS signal is the active-Low slave select input to the amplifier. The analog IO circuit converts the analog voltage to a 14-bit digital representation. [1].

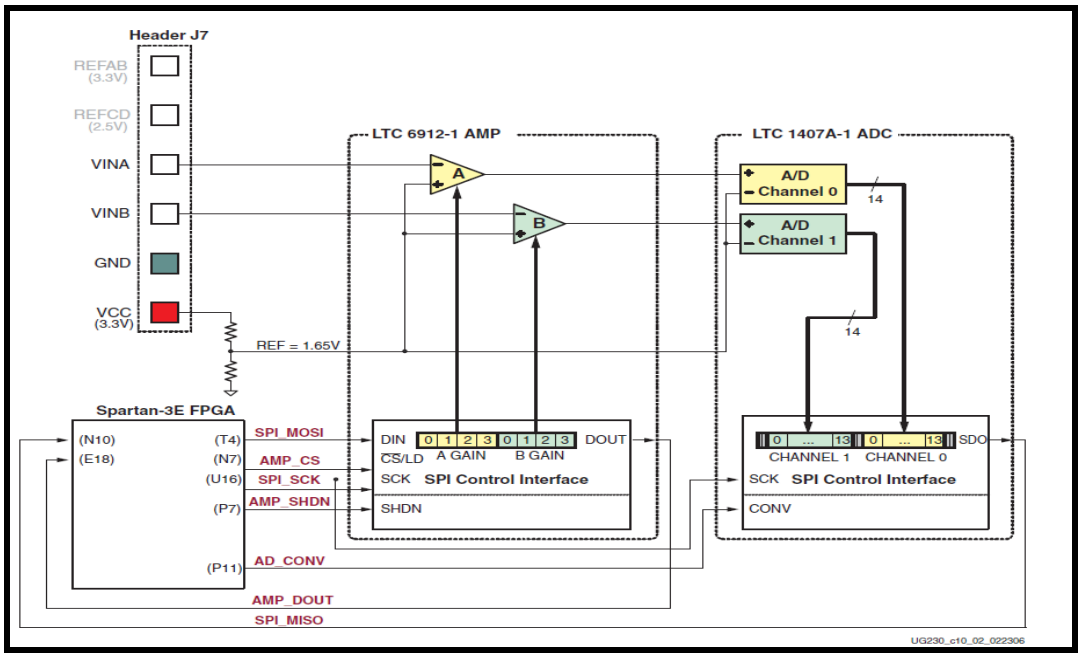

Fig.6. Detail view of Gain Amplifier and ADC [1]

E. Discriminator

When the ADC output value is between higher than lower threshold value (LLD) and lower than higher threshold value (ULD), then pulse detector gives the peak found signal to the counter to increase the count value. In this design ULD and LLD is set for window as a Voltage Range is LLD = 0.86m Volt and ULD = 1.6 Volt.

F. Counter

When pulse detector found peak, it provides a peak found signal to counter and as a result, count value increases. Two 16 bit counters are used in counter circuit. One of the counters counts over a period of one second and stores the counting value in register and another one is used for total count.

G. Timer

50MHz clock frequency is pre divided to 1 second for using reset 16 bit Counter and data held in Latch.

H. Display

Finally the stored counting values are given to LCD through other necessary processing circuits. In addition, maximum peak value, total counts and counts per second are also displayed to LCD through LCD driver circuit.

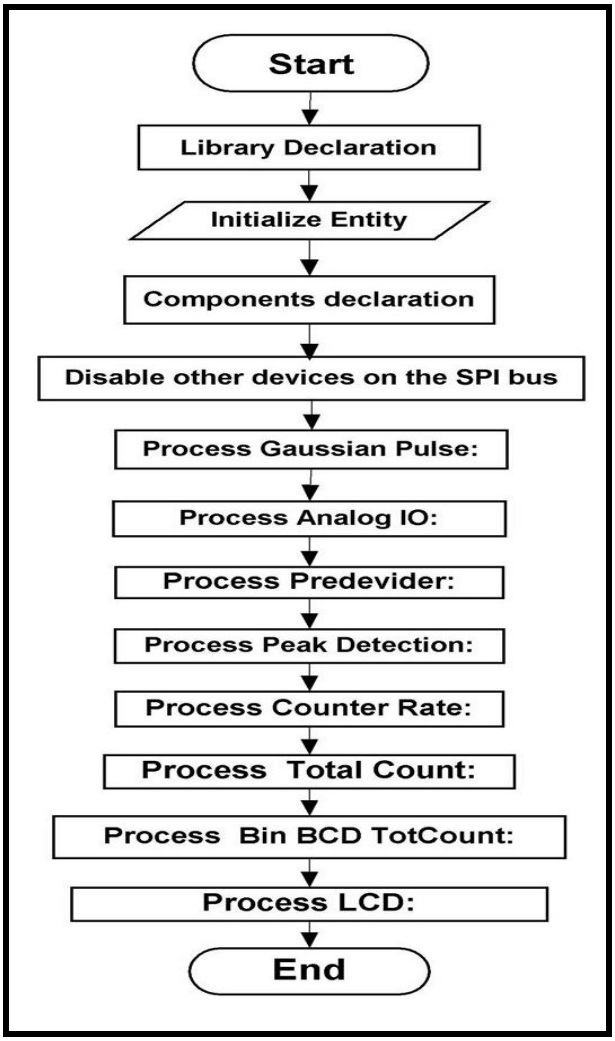

Fig. 7. Flow diagram of FPGA based Counting System

I. Software description

All the units of the system were designed, described in VHDL-modules and synthesized by Xilinx ISE Design suite 9.2. The System has been implemented on Xilinx Spartan-3E Starter board. The flow diagram of the VHDL code and RTL schematic with all entities and components of the Nuclear Counting System is shown in the following Fig.7 and 8.

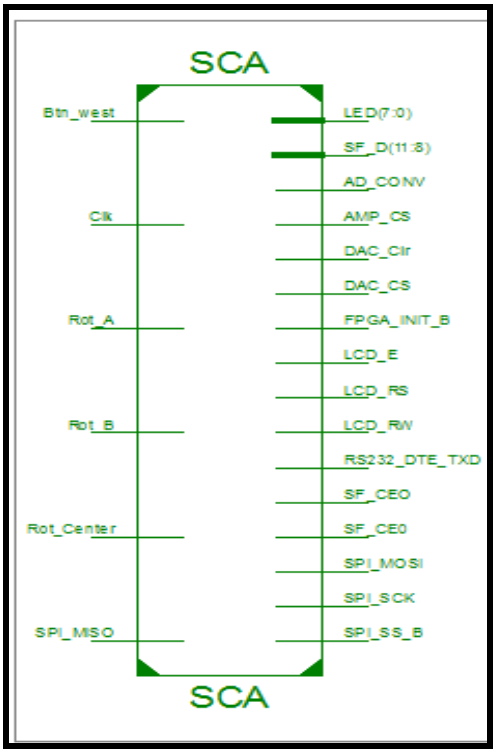

Fig. 8. RTL Schematic after simulation

IV. EXPERIMENTAL SETUP & RESULTS

In this design, FPGA based Nuclear Counting System has been simulated by Xilinx ISE Design suite 9.2 using VHDL code and tested on a Spartan-3E Starter board. In this technique internally generated Gaussian Pulses has also been used as instead of radiation which displayed, measured and compared by Digital Storage Oscilloscope and these pulses is given to ADC of the FPGA based system. After detecting a peak, pulse detector provides this signal to counter for process to display equivalent count per sec of Gaussian Pulse and Max value of Gaussian Pulse in LCD. (Window Voltage Range for FPGA based SCA is LLD = 0.86 Volt and ULD = 1.6 Volt.

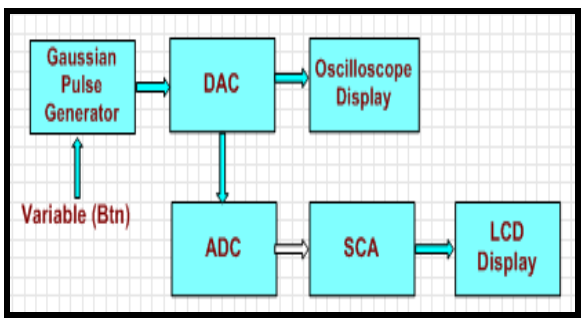

Fig. 9. Block diagram of experimental setup

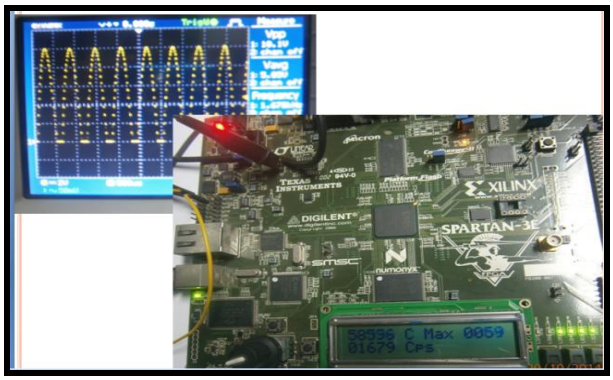

Fig. 10. Gaussian Pulse based Nuclear Counting

Fig. 11. Generated Gaussian pulse frequency (In Oscilloscope) compared with the counting system

Table II. Generated Gaussian pulse frequency (in Oscilloscope) compared with developed Nuclear Counting System

No. of Observation	Generated Gaussian pulse Frequency from Oscilloscope (KHz)	Generated Gaussian pulse Frequency equivalent to CPS	From Counting System (CPS)	Max Value
1.	1.947	1947	1947	45
2.	1.816	1816	1816	52
3.	1.679	1679	1679	59
4.	1.584	1584	1584	68
5.	1.521	1521	1521	72
6.	1.425	1425	1425	78
7.	1.369	1369	1369	92
8.	1.221	1221	1221	96
9.	1.102	1102	1102	116
10.	1.043	1043	1043	122

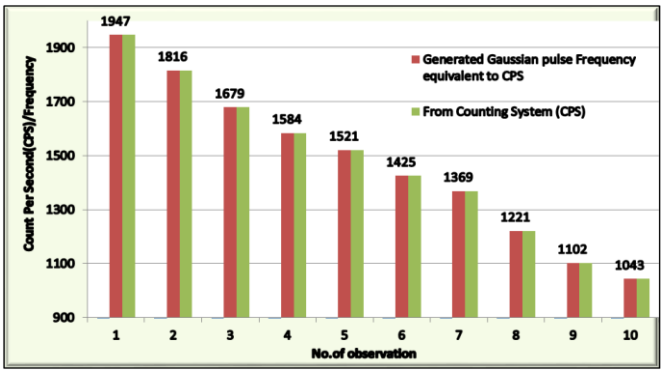

Fig. 12. Two results are compared and shown in chart

In above graph, counts per second (CPS) is from the FPGA based System and frequency of generated Gaussian pulse from Oscilloscope in KHz. For convenient of plotting chart all data is taken in CPS is shown in Fig. 12. FPGA counting system is showing almost similar results between two systems.

V. CONCLUSION

Lack of awareness occupational worker, patient and their attendant get unwanted radiation dose. Because of radiation hazards so many diseases occur and in the long run death. For growing awareness in the people about radiation, it is need to develop facility available for radiation detection and monitoring. In order to meet the above requirements a flexible, portable and fast FPGA Nuclear Counting System can be design and develop. This paper has mainly given emphasis on the design, simulation and implementation of Gaussian pulse based Nuclear Counting System. As the design is FPGA based so the system has flexibility to configure hardware. This FPGA based system can replace complex analog nuclear counter circuitry. The VHDL (Hardware Description Language) design for Gaussian pulse based Nuclear Counting System has been developed and tested on Spartan-3E Starter board. Finally a successful result has been carried out by this developed system. Future objective of this work is to develop detector circuitry including PC based data acquisition system through USB port using LabVIEW.

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