International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 8, August - 2014

Harmonic Reduction in New PWM Switching Scheme of Hybrid Multilevel Inverter

Ankur Chourasiya
PG Scholar
Dept. of Electrical Engineering
SATI, Vidisha
Madhya Pradesh, India

S. S. Thakur
Assistant Professor
Dept. of Electrical Engineering
SATI, Vidisha
Madhya Pradesh, India

S. P. Phulambrikar,
Associate Professor & HOD
Dept. of Electrical Engineering
SATI, Vidisha
Madhya Pradesh, India

***Abstract*--This paper describes a harmonics reduced in a hybrid cascaded multilevel inverter circuit with new pulse width modulation (PWM) scheme. A pulse width modulations proposed method [7] are uses reduce switching device. Then to reduced the switching losses and also reduced the harmonics in proposed inverter circuit. These topologies are a combination of a conventional inverter and hybrid inverter. These topology used the combined form of a new seven level hybrid cascaded multilevel inverter. The multilevel carrier based pulse width modulation methods are used in this topologies of a seven level output voltage wave forms is shown in FFT window MATLABE/SIMULINK is used to simulate the inverter circuit operation and control signals.**

***Key words*- Multilevel Inverter (MLT), Hybrid Cascaded Multilevel Inverter, Pulse width modulation (PWM).**

1. INTRODUCTION

Inverter converts DC power into Ac power at required output voltage and frequency. Inverter produces uninterrupted power supplies. In industries then are many applications on inverter such as adjustable-speed of AC machine, induction heating, high voltage DC Transmission (HVDC), flexible AC transmission line (FACT) e.t.c. In Industries uses inductive loads hence a power quality problems in a power system is more. Then more harmonics, low power received and more voltage sag. All these problems with a three level inverter can be short out by higher level inverter circuit. A multilevel inverter has been introduced as an alternative in high power and medium voltage situation subsequently; several multilevel inverter topologies have been developed. Multilevel inverters are uses a large switching devices as compared to ordinary inverter circuits. a multilevel inverter are emerging day by day because of short switching devices and switching losses. Hence this paper describes a new approach for reduced switching devices and a reduced switching loss hence overcomes a harmonics in a inverter circuit. This paper focus on a new seven level hybrid cascaded multilevel inverter (HCMLI) with only eight switches and produces a seven level output voltage with a low harmonics. When uses a two asymmetric DC voltage sources .all these features are not available in other seven level inverters.

2. MULTILEVEL INVERTER

Multilevel inverter is very versatile and is uses for power electronics topology for high power application. The multilevel inverter has a very low electromagnetic interference (EMI) and it efficiency is high compare to conventional inverter. Multilevel inverter is a latest alternative to implement low frequency based inverters with low output voltage distortion. Basic multilevel topologies are of three types. Figure 1.1 shown in bellow:-

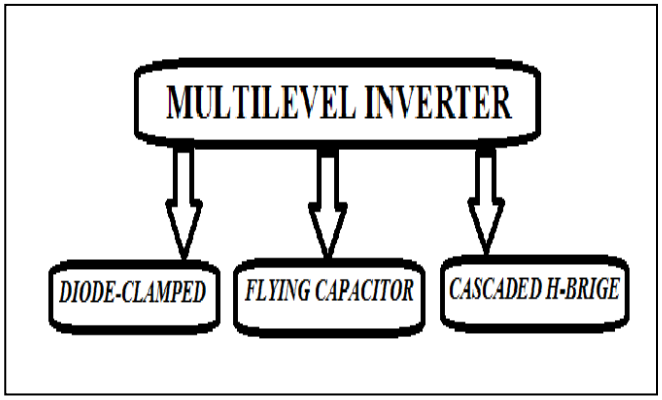

Figure 1.1 Multilevel inverter topologies

All three topologies of a multilevel inverter can be used in reactive power compensation without having the voltage unbalance problem. Diode clamping is not needed in flying capacitor and cascaded inverter configuration and balancing capacitors are not needed in diode clamped and cascaded inverterconfiguration. in cascaded inverter configuration requires the least number of components.

2.1 DIODE-CLAMPED MULTILEVEL INVERTER:

The diode clamped topology is shown in fig 2.1 this inverter is also called as a neutral point converter. This figure shows a three level neutral point converter. It was the first widely popular multilevel inverter topology. It is extensively used in industrial application this three levels neutral point converter uses capacitor to generate intermediate voltage level and voltages across the switches are only half cycle in dc input. These inverters most commonly used in high power and medium power voltages.

DISADVANTAGES-

1. In case of diode clamped inverter only single dc voltage source is used.

2. It have a higher switches, diodes and capacitor are used then the overall cost of this inverter is high.

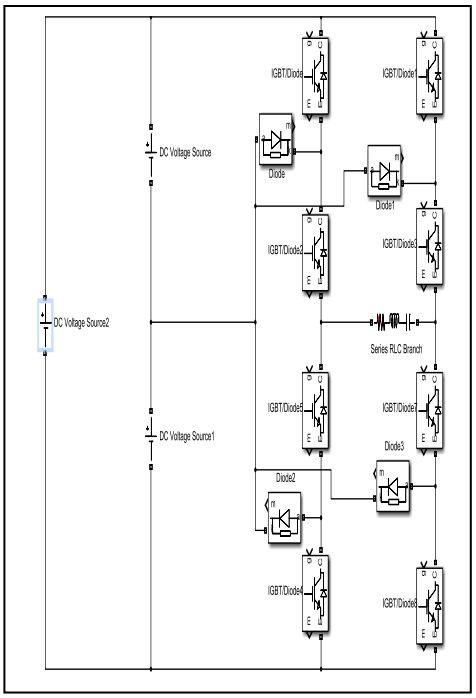

Figure -2.1Three level diode clamped MLI

2.2 FLYING CAPACITOR INVERTER:-

The flying capacitor topologies are shown in figure 2.2. Flying capacitor inverter is a good alternative to overcome some of the neutral point clamped inverter topology. Drawbacks of these inverter topologies can be overcome by additional levels and voltage clamping. These topologies doesn't require additional clamped diode, and it provides a reduce switching states. That can be used to control the capacitor charge even under load with DC source.

DISADVANTAGES:-

1. Flying capacitor inverter topology requires larger structures.

2. Large numbers of capacitors are used to initialize the charge of capacitors which requires an additional circuit.

3. It uses a single DC source only.

4. Cost is high.

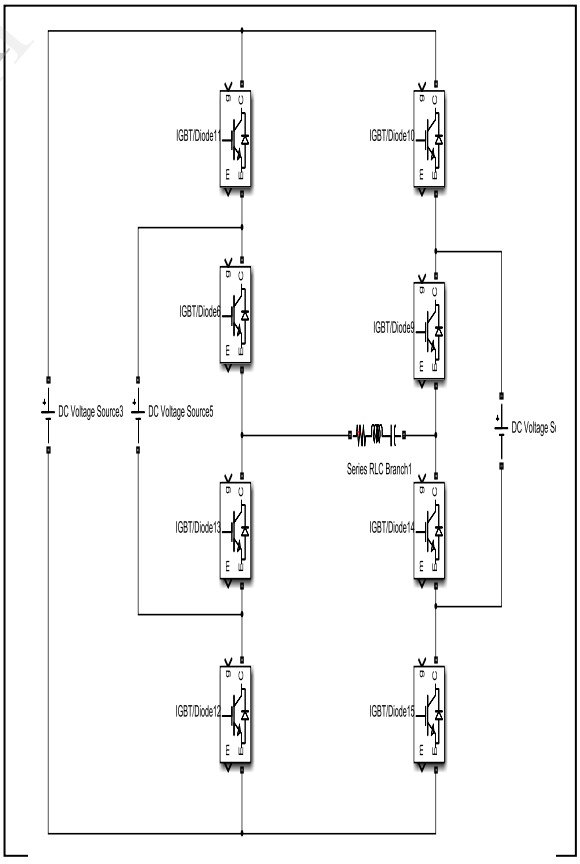

Figure-2.2 Flying capacitor multilevel inverter.

2.3 CASCADED H- BRIDGE MULTILEVEL INVERTER-

The cascaded multilevel inverter topology consist of number of Hbridge inverter unit with a separate DC source of each topology and are connected in cascaded or series circuit. Each H-bridge can produce different voltage levels.

In figure 2.3 shown H-bridge multilevel inverter topologies which produces seven level output voltages, such as $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$. This topology uses 12 switches and 3 voltage sources as shown in figure 1.4.

DISADVANTAGES:-

1. H bridge cascaded inverter topologies requires a large number of switches and many DC voltages sources.

2. Overall cost is higher.

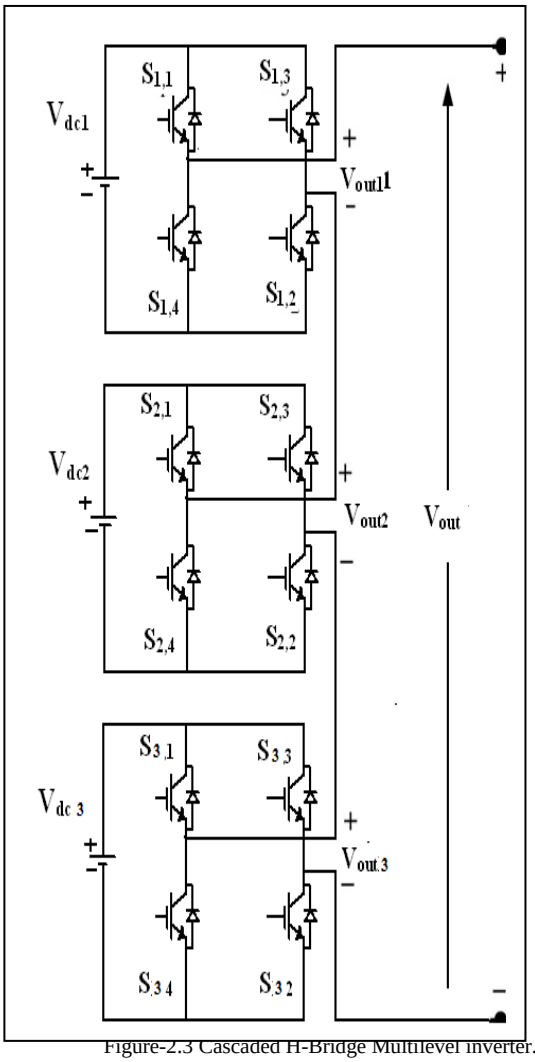

Figure-2.3 Cascaded H-Bridge Multilevel inverter.

3. PROPOSED H-BRIDGE SYSTEM

3.1 BLOCK DIAGRAM OF PROPESED SEVEN LEVEL CASCADEDH-BRIDGE MULTILEVEL INVERTER CIRCUIT.

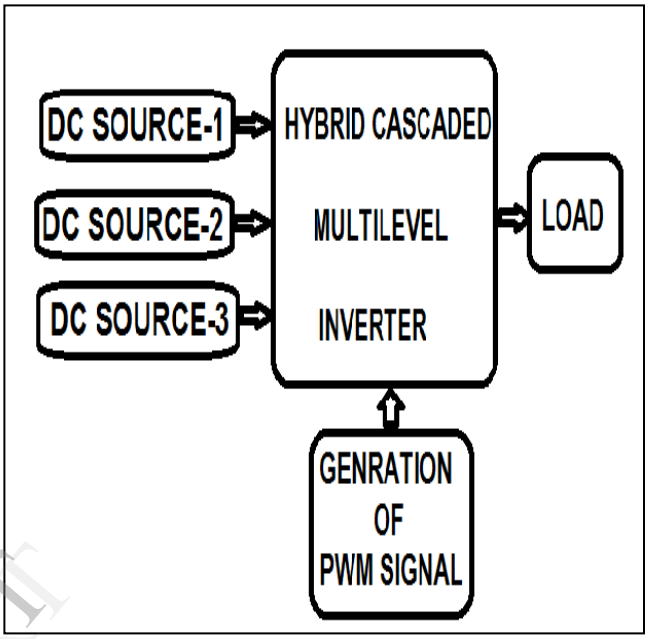

Figure-3.1 Proposed block diagram.

This proposed method shown in figure 3.1, seven level hybrid cascaded multilevel inverter with a pulse width modulation method is designed by reducing a number of switches hence reduces switching losses. This inverter topologies are used only eight switches, four capacitors and three asymmetrical voltage sources. This method is a combination of three inverter circuit first is a H-bridge inverter and another uses two conventional inverter, To form a new proposed seven level cascaded H-bridge multilevel inverter. This topology uses a multi carrier based new PWM method, used to produced a seven level output voltage. This inverter circuit is used in a hybrid electric vehicles and electrical vehicles.

3.2 SIMULATION WORK

3.2.1 Simulation diagram:-

A simulation diagram are shown in a figure 3.2 using MATLAB/SIMULINK.

The simulation block diagram has seven level Cascaded hybrid multilevel inverter. This topology is H-bridge inverter and two normal conventional inverters are combined to form a new seven level cascaded hybrid multilevel inverters. The

three inverter circuit are connected in cascaded manner .as shown in figure-3.2

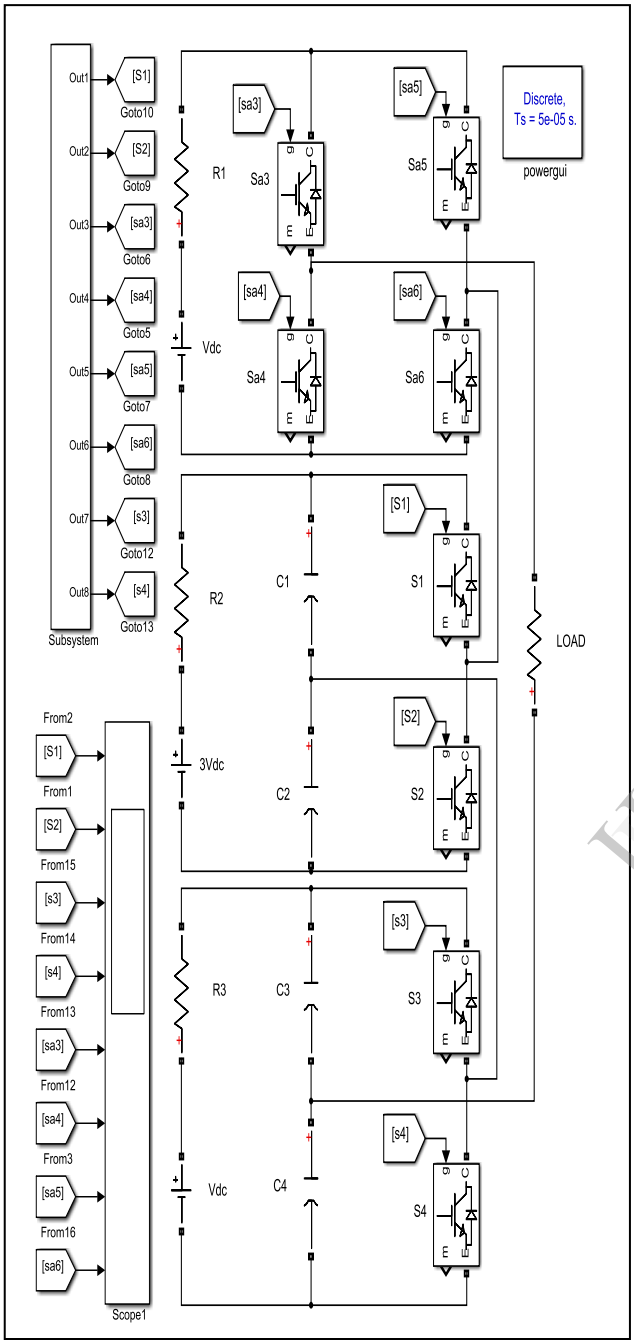

Figure-3.2 Seven-level HMLI simulation diagram.

3.2.2 Proposed PWM signal for hybrid multilevel inverter:- Generation of pulse width modulation signal formula shown in tabel-1

TABEL-1 Pulse generation formula

Sn	Hybrid PWM mixing operation
S1	A1
S2	$\overline{A1}$
S3	A3
S4	$\overline{A3}$
Sa3	PWM*((A2*A1)+($\overline{A2}$*$\overline{A1}$))
Sa4	$\overline{PWM}$+((A2*A1)+($\overline{A2}$*$\overline{A1}$))
Sa5	PWM*$\overline{((A2*A1)+(\overline{A2}*\overline{A1}))}$
Sa6	$\overline{PWM}$+((A2*A1)+($\overline{A2}$*$\overline{A1}$))

These pulses are given for eight switches. Two conventional inverter has a S_1, S_2, S_3, S_4 and H-bridge inverter has four pulse Sa_3, Sa_4, Sa_5, Sa_6. The figure 3.3 shows output of pulse width modulation. These are a new carrier based pulse width modulation output wave. This PWM signal generate a new proposed signals with a combination of logical operation as shown in a table-1.

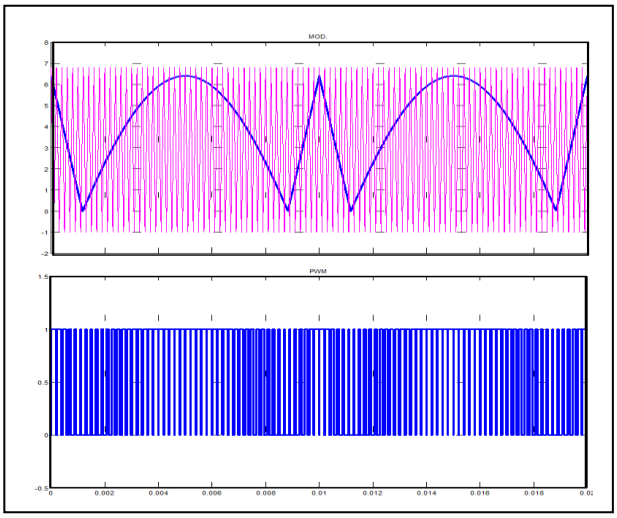

Figure-3.3 Output of a PWM

4. RESULT:-

This new seven level H-bridge cascaded multilevel inverter topologies are implemented in MATLAB/SIMULINK software. HMLI with eight switches is shown in figure-3.2 and control signals for all eight switches with new logical scheme, output wave forms are shown in figure - 4.1.

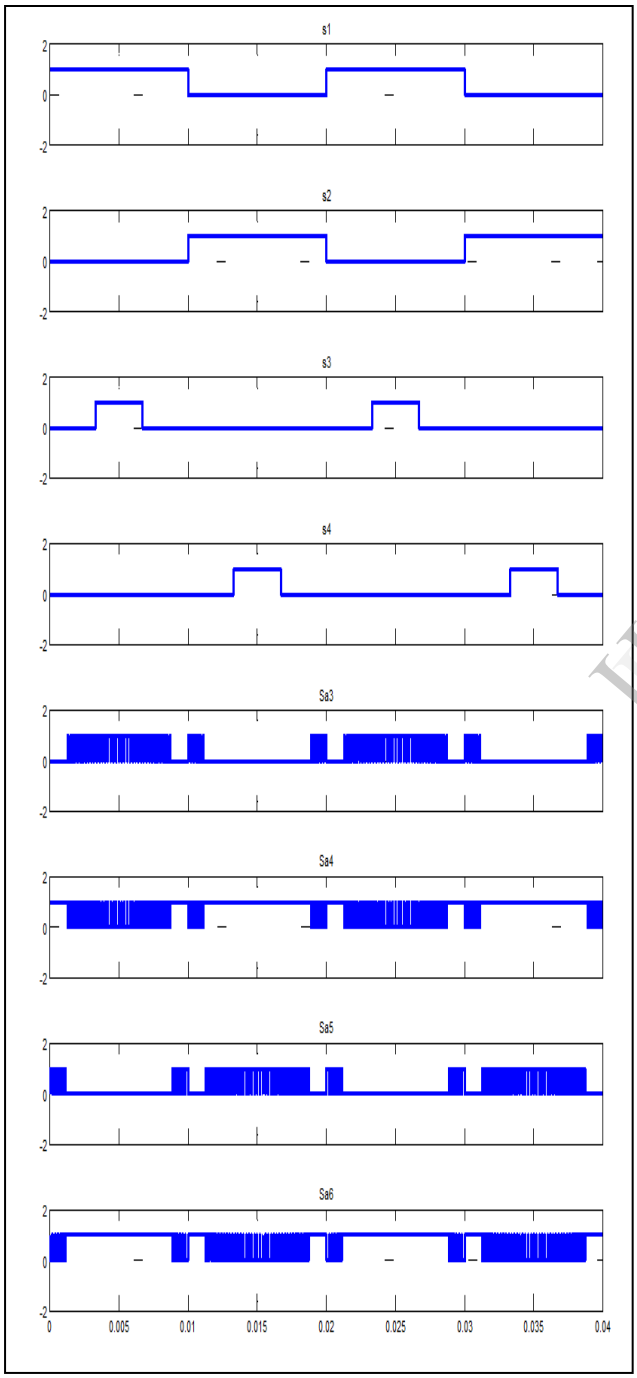

Figure-4.1 Control signals for seven levels HMLI.

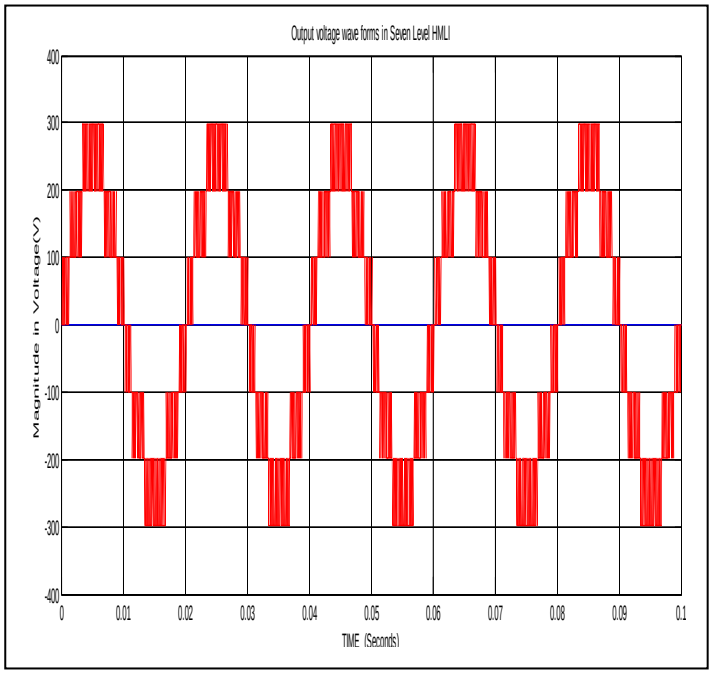

Figure-4.2 Output voltage waveform for seven levelsHybrid Cascaded Multilevel Inverter.

The output voltage waveform of a seven level shown in figure-4.2 is designed using a MATLAB. My proposed work has a seven level hybrid cascaded multilevel inverter. These seven level cascaded multilevel inverter uses only eight switches for a seven levels.

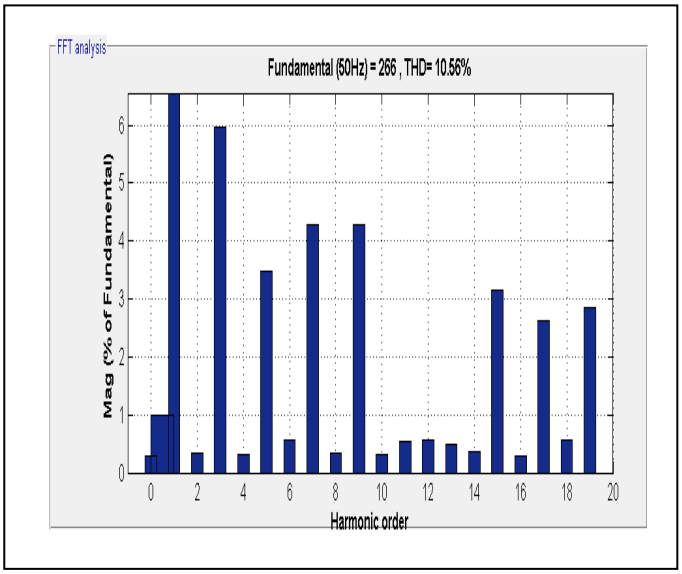

Figure-4.3 FFT analysis for seven level hybrid cascaded multilevel inverter.

Figure 4.3 shows in THD (total harmonics distortion) value for a proposed H-bridge cascaded multilevel inverter circuit in a seven level. This proposed circuit has THD-10.59% for a seven level output voltage waveform.

The topology of an inverter circuit is based on the requirement and range. All topologies have both advantages and disadvantages. The two level inverters cost is very low as compared to other conventional inverter topologies. But very high value of THD. Then to reduce THD levels of a inverter voltage waveforms should be increase. And the number of level increases in a inverter then switching losses increased. Theses all above problems can be avoided by hybrid multilevel inverter.

5. CONCLUTION-

This proposed inverter circuit the numbers of switches and their switching losses are reduced as compared to other seven level conventional inverter circuit. This inverter topologies uses a new pulse width modulation scheme hence this inverter circuit is less complicated as compared to other seven level conventional inverter circuit. This inverter topology has less harmonics and the total harmonics distortion can be verified through a powerful /FFT toolbox.

REFERENCES

[1] AyoubKavousi, BehroozVahidi, Reza Salehi,MohammadKazemBakhshizadeh senior IEEEmember," Application of the Bee Algorithm forSelective Harmonic Elimination Strategy inMultilevel Inverters" IEEE Transactions On Power Electronics, Vol. 27, No. 4, April 2012

[2] Jose Rodriguez, Jih-sheng lai, Fan zheng peng, senior member IEEE,"Multilevel inverter: A survey oftopologies, controls, and applications"IEEEtransactions on industrial electronics, vol. 49,no.4,aug 2002.

[3] Haiwen Liu, Leon M, SurinKhomfoi,"HybridCascaded multilevel inverter with PWM controlMethod"978-1-4244-1668-4/08,2008IEEE.

[4] SurinKhomfoi, NattapatPraisuwanna, LeonM.Tolbert,"A hybrid multilevel inverter applicationfor renewable energy resources including arecofiguration technique" 978-1-4244-5287-3/10/2010 IEEE

[5] S.Khomofi, AChatrchai,"A 5-level cascaded hybridmultilevel inverter for interfacing with renewableenergy resources,"proceedings of the 2009 electricalengineering/electronics, computer telecommunications,and information technology,Chonburi May 6-9, 2009, pp.284-287.

[6] N.Praisuwanna, S.Khomfoi,"A hybrid cascadedMultilevelinverter, "proceedings of the 2010 electricalengineering/electronics, computer telecommunications, and information technology,Chonburi May 19-21,2010,pp.1041-1044.

[7] M. Thirumalai, V. Prakash, "Design and Implementation of Hybrid Multilevel Inverter for High Output Efficiency," International Conference on Smart Structures & System (ICSSS-2013), March 28-29, 2013, Chennai, India.