I-CDPK Scheme in Chaotic Communication with Calculative Synchronization Delay

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Abstract:

This paper presents effect of synchronization delay in chaotic communication based system as well as secures communication system using Interleaved Chaotic Differential Peaks Keying (I-CDPK) algorithm. The proposed communication system consists of four major modules: I-CDPK modulator (ICM), frequency modulation (FM) transmitter, FM receiver and I-CDPK demodulator (ICDM). In the ICM module, there are four components: a chaotic circuit to generate the chaotic signals, A/D converter, D/A converter and a digital processing mechanism to control all signal flows and performs I-CDPK modulation corresponding to the input digital bits. Furthermore, the performance of bit error rate of the proposed system is analyzed and compared with those of the correlator-based communication systems adopting coherent BPSK, and non-coherent I-CDPK simulated (Synchronization delay =1000), ½ I-CDPK (Synchronization delay =100) schemes. Synchronization delay is a much effective factor during the communication. So, its deep study before designing a chaotic system is essential.

***Key words**:* I-CDPK algorithm, Synchronisation delay, chaotic system, MACT, MACR, I-CDPK, ½ I-CDPK.

1. Introduction:

In digital communication systems, it is very useful for several users communicate with each other through the public channel simultaneously. The technique usually known as Multiple Access. Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA) and Code Division Multiple Access (CDMA) are three major ways used to achieve Multiple Access. Recently, many previous works [1] [2] have shown the effectiveness in applying chaotic systems to Multiple Access digital communication systems by using the chaotic signals/sequences generated from the chaotic systems to replace the quasi-orthogonal binary code sequences used in CDMA scheme. In this study, base on Interleaved Chaotic Differential Peaks Keying (I-CDPK [3]) modulations and chaotic synchronization techniques, a novel Chaotic Multiple Access Digital Communication system is proposed [4].

Synchronization delay is a parameter by which we can control bit error rate and time duration of bit transmission. In this paper, I have shows the calculative synchronization delay that's gives better

response and results of bit error rate between theoretical and proposed method .this proposed method shows low BER than theoretical method.

2. Chaos-based digital communication system:

In fig.1 shows a block diagram of the proposed chaos-based digital communication system in which there are four major modules, i.e. the interleaved chaotic differential peaks keying modulator (ICM), frequency modulation (FM) transmitter, and frequency modulation (FM) receiver and interleaved chaotic differential peak keying demodulator (ICDM). Before the transmitting period, the ICM executes an off-lined self-learning process, to establish analog chaotic patterns corresponding to the input bit sets. Certain parameters of these chaotic patterns (i.e. the initial peak value and samples) are digitized by A/D converter and are stored into the ICM's memory. [3]

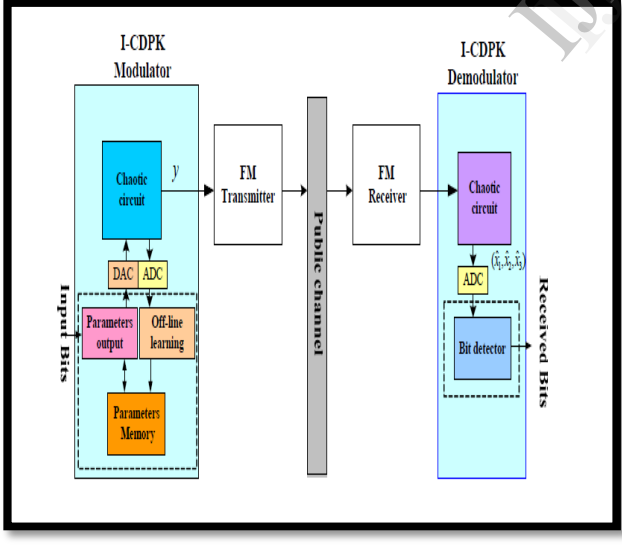

Fig. 1: The block diagram of the proposed non-correlator-based chaotic digital

At the beginning of the transmitting period, reading the digitalized parameters corresponding to the input bits desired to be transmitted from the ICM_s memory and the D/a converter transforms them from digital data to analog signals used to perturb the signals of the ICM_s chaotic circuit (Rössler-like system). The certain pieces of a perturb chaotic signal (i.e. the system output) homologizing to the original input bits are then fed to the FM transmitter, which sends the transmitted chaotic signal to the public channel by using the frequency modulation. The ICDM receives the transmitted chaotic signal from the output of FM receiver dedicated to demodulating the FM signals to the transmitted chaotic signal. Synchronization between the chaotic circuits in the ICM and ICDM modules is maintained through the observer with the appropriately designed observer gain. In ICDM, through the A/D converter, the bit detector samples the signals of the ICDM_s chaotic circuit and translates to the corresponding transmitted bit sets [3].

3. Architecture of the proposed communication system:

In this system, there are total three Links, which are Link 1, Link 2 and Link 3. Every three serial input bits from each Link will be combined to nine parallel bits as the input bits to the MACT. As mentioned above, every Link is assigned to a system state of the transmitter's chaotic circuit. Then, the output of the MACT is fed into FM transmitter. From the public channel, FM receiver extracts the transmitted chaotic signal as the input of the MACR. Finally, the every three bits transmitted from each Link in a transmission, will be received by demodulating the corresponding recovered system state of the chaotic circuit in the MACR. [4]

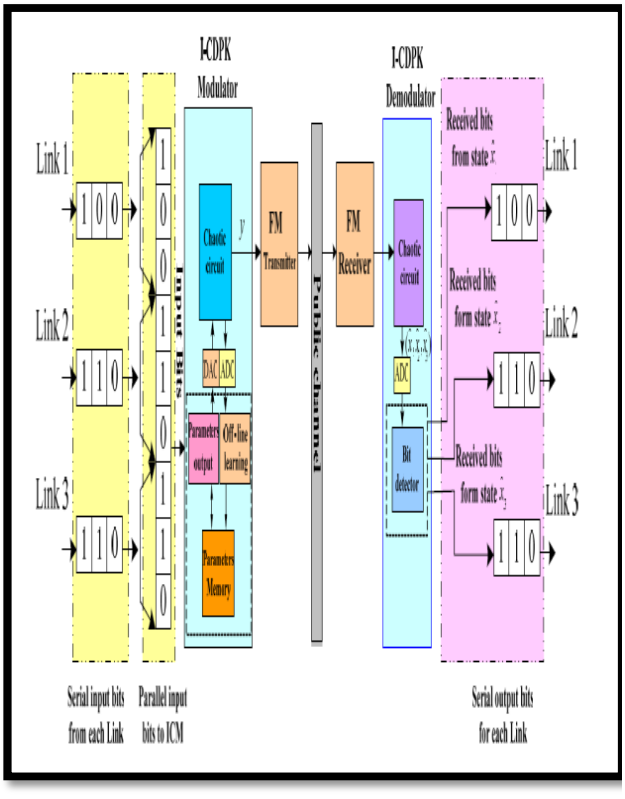

Fig. 2: The proposed Multiple Access Chaotic Digital Communication system

4. I-CDPK scheme:

As shown in Fig.2, there are three individual Links in the proposed system. In order to perform transmission at the same time among these Links, the encoding/decoding rule used in I-CDPK scheme [2] is described as in Fig.3.

Implement I-CDPK modulation technique in our dissertation. Because of it resist the overlapping of peaks. By which we can easily detect the peaks at receiver end. Transmitted data bits are coded by extracting the consecutive peak values from all the system states of transmitter's chaotic circuit and decoded by all the recovered system state of receiver's chaotic circuit. For achieving Multiple Access, every Link is represented by a specified system state pair in the chaotic circuits of transmitter and receiver. The Synchronization Bits, every three bits input from each Link will be coded or decoded from the corresponding system state of transmitter's chaotic circuit or the corresponding recovered system state of receiver's chaotic circuit, as a result, these three Links can transmit and receive every three bits in every transmission at the same time on the same frequency band. That is why Multiple Access can be performed. In order to explain how this system works in detail, the complete operations of the multiple-accessing transmitter and receiver will be introduced in the following two subsections [4].

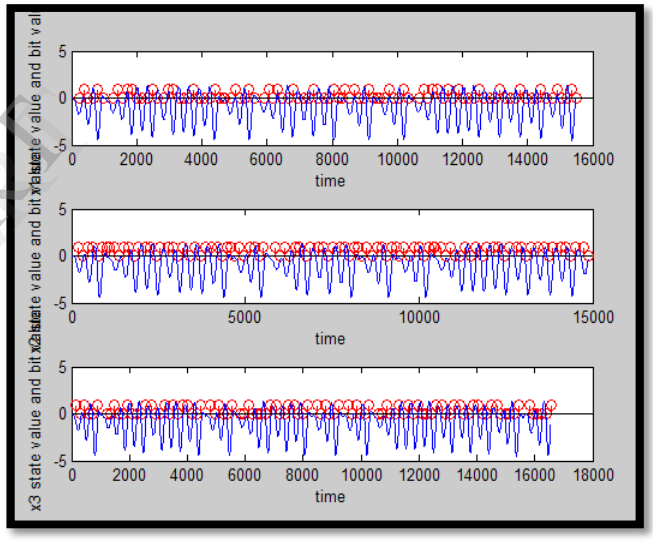

Fig. 3: Proposed I-CDPK scheme

MACT*:*

As shown in Fig.2, since each Link can transmit and receive three data bits in a transmission, there are total data bits transmitted during this transmission. Before this multiple access system enters transmitting period, the MACT must carry out a self-learning process to find out the chaotic parameters corresponding to every bit binary code and store these digitalized found chaotic parameters into MACT's

memory. After that, these three Links are ready to transmit data bits. [4]

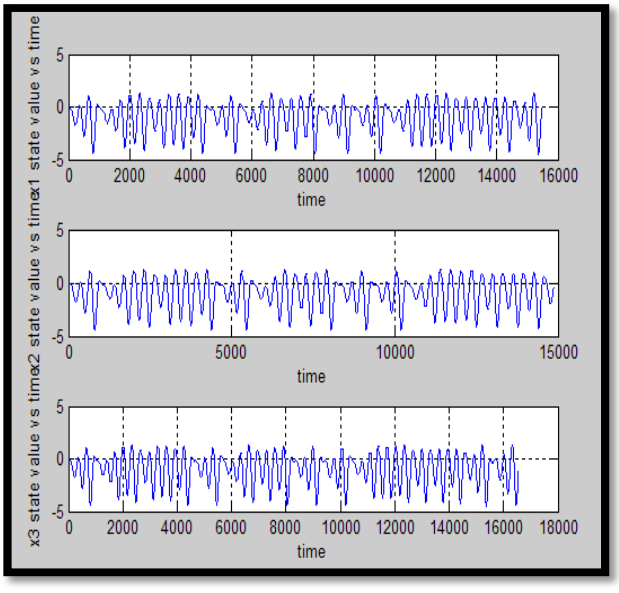

Fig.4: Input signal in MACT

MACR:

Link at Receiver Output of the proposed Multiple Access Chaotic Digital Communication system. In this example, the synchronization bits are same and the transmitted input bits are "100", "100" and "100" from Link 1, Link 2 and Link 3, respectively. As shown in Fig.4, all the transmitted input bits of each Link can be correctly recovered from the corresponding state of the MACR's chaotic circuit. [4]

5. Synchronization type:

In this paper we have used 'S' type chaotic flow. Cases D-S all have similar structure and topologically resemble the Rössler attractor in that they are dominated by a single folded band. There are 19 types of chaotic flows (A-S). [5]

$\dot{x}_1 = -x_1 - 4x_2;\ \dot{x}_2 = x_1 + x_3^2;$

$\dot{x}_3 = 1+x_1,$

$y = x_3.$ ..... (1)

Equ. (1) Has one positive Lyapunov exponent of 0.188 and fractal dimension of 2.151. Then the MACT's chaotic circuit can be rewritten by the matrix form:

$$x = \begin{bmatrix} -1 & -4 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} x + \begin{bmatrix} 0 \\ y^2 \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} (d),$$

$$\equiv Ax + f(y) + Bd.$$

$$y = x_3 = [0 \quad 0 \quad 1]x,$$

$$\equiv C^T x.$$

..... (2)

Observer gain is L^T = [54.*01* - *13.0075 14*]

6. Effect of Synchronisation delay:

Synchronization of chaos is a phenomenon that may occur when two, or more, dissipative chaotic systems are coupled. Because of the exponential divergence of the nearby trajectories of chaotic system, having two chaotic systems evolving in synchrony might appear surprising. However, synchronization of coupled or driven chaotic oscillators is a phenomenon well established experimentally and reasonably well understood theoretically. Synchronization of chaos is a rich phenomenon and a multi-disciplinary discipline with broad range applications.

Synchronization delay is an effective parameter in communication studies." *Synchronization delay is delay between groups of bit synchronize during the transmission".* Synchronization delay will minimize in this paper to reduce the length of bit train and the reducing the bit error rate.

7. Result:

In the graph shown in a Fig.5, I have compared the BPSK, I-CDPK simulated (Synchronization delay =1000), ½ I-CDPK (Synchronization delay =100). I-CDPK simulated shows the lower bit error rate then BPSK with respect to corresponding SNR but ½ I-CDPK shows approximate half bit error rate then I-CDPK. ½ I-CDPK reduces 50% bit error rate then I-CDPK show calculative amount of synchronization delay is better for chaotic communication.

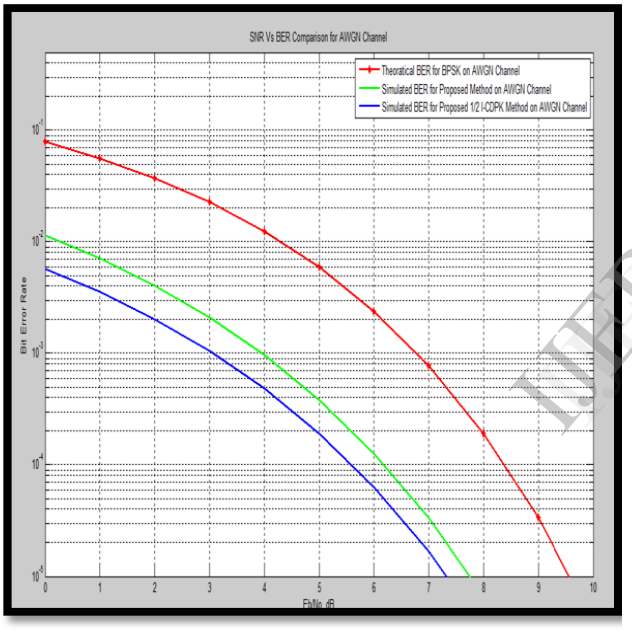

Fig. 5: The BER curves of I-CDPK simulated (synchronization delay=1000), ½ I-CDPK (Synchronization delay=100).

8. Conclusion:

½ I-CDPK shows the result then I-CDPK and BPSK due to calculative amount of synchronization delay so synchronization is an important factor for the further study in communication field. The chaotic circuits in the ICM and the observer-based chaotic circuits in the ICDM can be synchronized by adopting the proposed observer-based chaotic synchronization. An illustrative system has been presented to demonstrate the effectiveness of the proposed system and its bit error performance has been analyzed. The simulation results show that the error performance of the proposed system lies between the error performance of coherent BPSK, and non-coherent I-CDPK simulated (Synchronization delay =1000), ½ I-CDPK (Synchronization delay =100). Chaotic communication is a very important and interesting research area in secure communication so all parameters related to it, is deeply studies by designing engineers.

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