Implementation and Analysis of Symmetrical and Asymmetrical Configurations of Series Connected Sub-Multilevel Inverter with Nearest Level Control Modulation

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***Abstract*— Multilevel Inverters are the emerging research area since last decade and in this duration so many configurations of Multilevel Inverters are introduced, Some of those are application oriented and some configurations are generalized and combinational in nature. In this paper a configuration with Symmetrical and Asymmetrical types of Series connected Sub-Multilevel Inverter is analyzed with the Nearest Level Control Modulation. In general view of preferred configuration gives the more levels in output signal with the reference of Basic Multilevel Inverters. The article discuss about the implementation of Nearest Level Control Modulation to the referred configuration of Multilevel Inverter and its operation and performance by the indication of Total Harmonic Distortion of output signal for the both Symmetrical and Asymmetrical topologies.**

Keywords—Sub-Multilevel Inverter; Nearest Level Control Modulation; Symmetrical and Asymmetrical Topology; Optimal Configurations; Generalized structure.

I. INTRODUCTION

The Multilevel Inverters are introduced to improve the sinusoidal nature in output signal of inverter, over the basic conventional three types of multilevel inverters, the Cascaded H-Bridge multilevel inverter takes the major part of influence in commercial and research activities. Because Cascaded H-Bridge multilevel inverter's configuration adopts the traditional structure of basic inverter. This type of topology will give the more voltage withstanding capacity to the cells in multi-level stages. In this paper a configuration of multilevel inverter is referred to analyze the operation and performance, because it has also consists of basic H-Bridge. This configuration is structured like Series connected Sub-Multilevel DC sources are connected to the basic cell inverter.

Even though the topology structure is optimized, the performance is mainly depends on the modulation strategy. Selection of modulation strategy involves into so many aspects like switching frequency, switching losses, type of reference and pattern of output signal. For general and simple applications like normal UPS, Backup Powers, FACTS and domestic inverters have no need of complex modulation to operate the circuit. So a simple and best modulation is used to analyze the preferred configuration like Nearest Level Control Modulation.

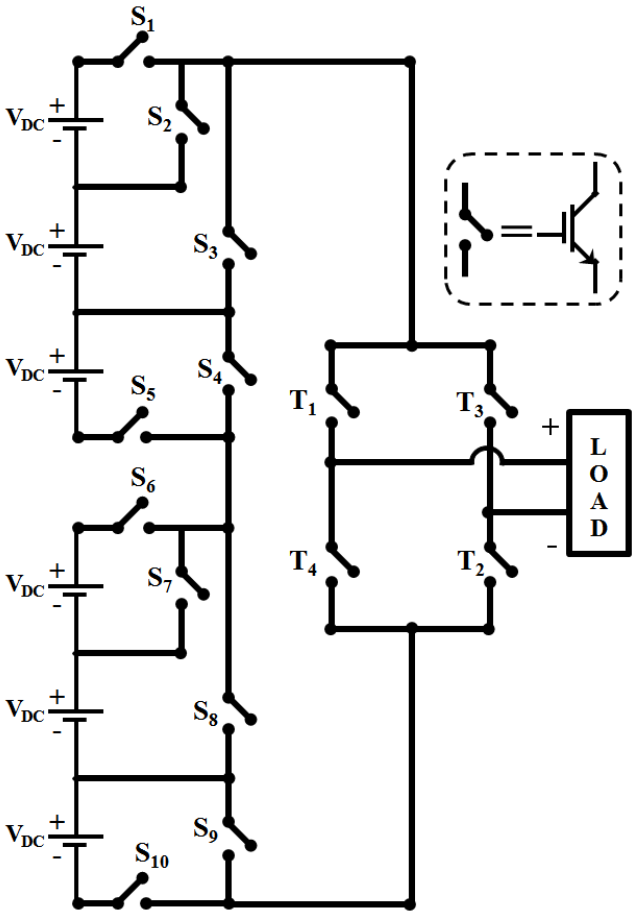

Fig. 1. Symmetrical Configuration of Series connected Sub-Multilevel Inverter [1].

A. Prefered Configuration of Multilevel Inverter

Series connected Sub-Multilevel Inverter configuration [1] is preferred, because of subsequent nature of structure with the basic cell inverter and the configuration has Symmetrical and Asymmetrical type of structures and they are shown in Fig. 1 and 2 respectively.

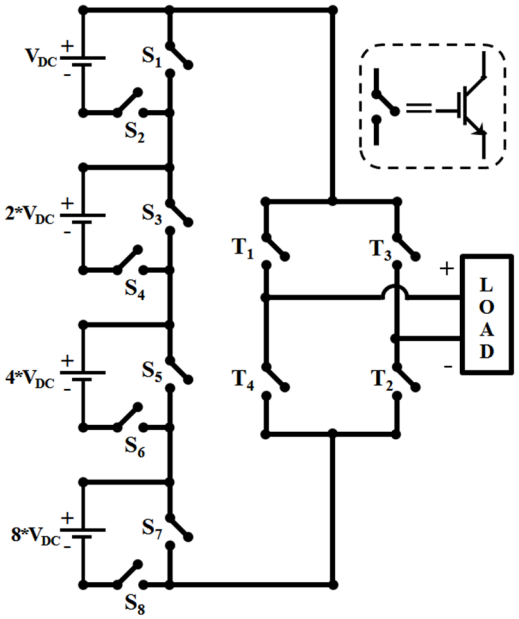

Fig. 2. Asymmetrical Configuration of Series connected Sub-Multilevel Inverter [1].

All the switches indicated with S_x are used to provide the specified voltage level on output and the switches with T_x are used for inversion processes, overall configuration generates the required improved inverter output. In both symmetrical and asymmetrical configuration a basic inverter cell is used for the basic inversion processes, and the remaining circuit has provided to supply the required DC voltage by changing the state of switches with a specified logic. The logical circuit path selection of the topology is simple when the modulation strategy specifies the level and states of inversion cycle of output signal.

For simple operation like to get the $3*V_{DC}$ level in the inversion, S_1, S_5, S_8 and S_9 are the active switches to get the required level in symmetrical configuration as shown in Fig. 1, and the switches S_2, S_4, S_5 and S_7 are in ON state to provide the required level in Asymmetrical configuration as in Fig. 2. If T_1 and T_2 switches are in active then the output signal is +ve, then T_3 and T_4 switches gives the –ve cycle in inversion processes. The total operating and switching states of the symmetrical and asymmetrical topologies in +ve cycle are tabulated in Table 1 and 2 respectively.

TABLE 1. SWITCHING STATES OF SYMMETRICAL PREFERRED MULTILEVEL INVERTER.

Voltage Level	Switching States of Switches													
	T_1	T_2	T_3	T_4	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+1	1	1	0	0	0	0	1	1	0	0	0	1	0	1
+2	1	1	0	0	0	0	1	1	0	0	1	0	0	1
+3	1	1	0	0	0	0	1	1	0	1	0	0	0	1
+4	1	1	0	0	0	0	1	0	1	1	0	0	0	1
+5	1	1	0	0	0	1	0	0	1	1	0	0	0	1
+6	1	1	0	0	1	0	0	0	1	1	0	0	0	1

TABLE 2. SWITCHING STATES OF ASYMMETRICAL PREFERRED MULTILEVEL INVERTER.

Voltage Level	Switching States of Switches											
	T_1	T_2	T_3	T_4	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0	0	0	0	0	0	0	0	0	0	0	0	0
+1	1	1	0	0	0	1	1	0	1	0	1	0
+2	1	1	0	0	1	0	0	1	1	0	1	0
+3	1	1	0	0	0	1	0	1	1	0	1	0
+4	1	1	0	0	1	0	1	0	0	1	1	0
+5	1	1	0	0	0	1	1	0	0	1	1	0
+6	1	1	0	0	1	0	0	1	0	1	1	0
+7	1	1	0	0	0	1	0	1	0	1	1	0
+8	1	1	0	0	1	0	1	0	1	0	0	1
+9	1	1	0	0	0	1	1	0	1	0	0	1
+10	1	1	0	0	1	0	0	1	1	0	0	1
+11	1	1	0	0	0	1	0	1	1	0	0	1
+12	1	1	0	0	1	0	1	0	0	1	0	1
+13	1	1	0	0	0	1	1	0	0	1	0	1
+14	1	1	0	0	1	0	0	1	0	1	0	1
+15	1	1	0	0	0	1	0	1	0	1	0	1

These Tables 1 & 2 are provides the all generatable levels respective switching states. But the time based operation of the inverter needs the specified modulation to select a required states on a particular time. Next section present basic concept and the logical approach of the Nearest Level Control Modulation.

B. *Nearest Level Control Modulation*

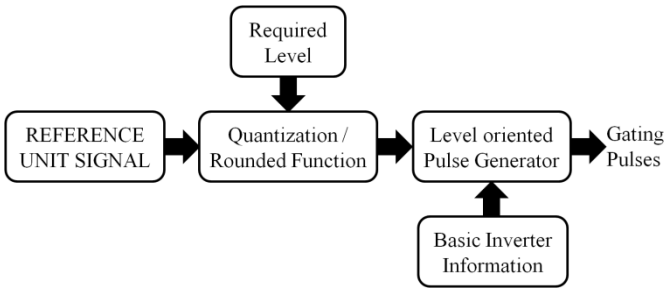

Fig. 3. Logical approach of NLC Modulation.

Generally the reference signal is the sinusoidal, because the power signal and the load requirement is also sine wave. This sine signal is quantized with the reference of required levels, *i.e.,* the level of multilevel inverter is N then the reference signal is quantized or rounded to amplitude division of N. Then the rounded signal is transferred to the pulse generator to generate the Pulses with the knowledge of the parameters of inverter. All these operational approach is illustrated in Fig. 3.

II. SIMULATION RESULTS AND ANALYSIS

With the knowledge of the circuit description as in [1] and about the Nearest Level Inverter as in [2,3] and also with literature review from the [4-10], the preferred configuration of multilevel inverter is simulated as symmetrical and asymmetrical types with the help of NLC modulation and the simulation diagrams are illustrated in Fig. 4 and 5 respectively.

The simulated results and the FFT analysis for the harmonic order of both Symmetrical and Asymmetrical Configurations are shown in Figs. 6-13.

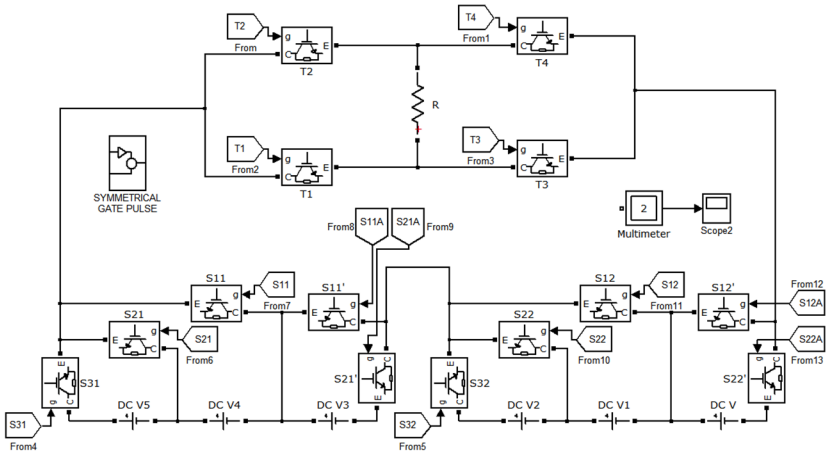

Fig. 4. Simulation Diagram of Symmetrical Series Connected Sub-Multilevel Inverter.

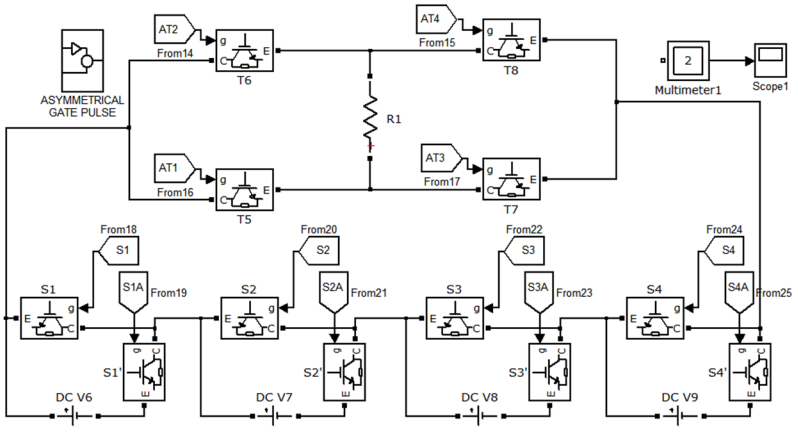

Fig. 5. Simulation Diagram of Asymmetrical Series Connected Sub-Multilevel Inverter.

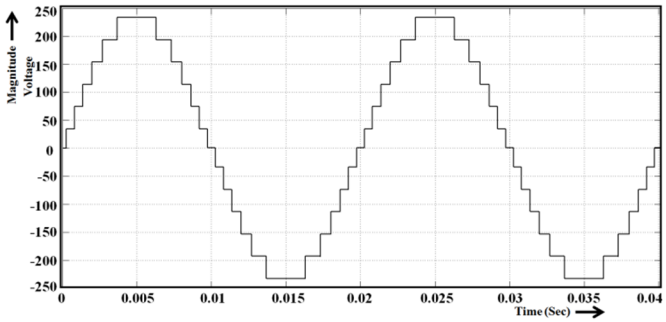

Fig. 6. Symmetrical topology Output voltage with NLC.

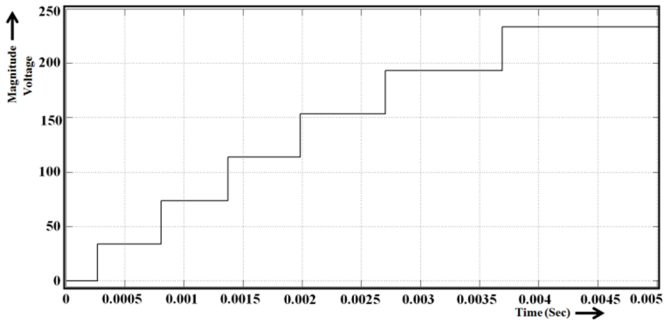

Fig. 7. Symmetrical topology Output voltage Level Pattern.

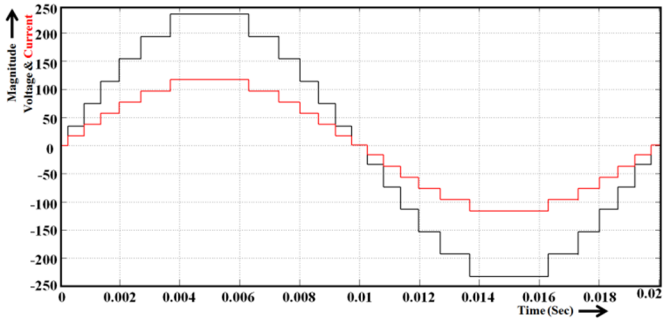

Fig. 8. Current (red) and Voltage (black) signals of Symmetrical topology with NLC.

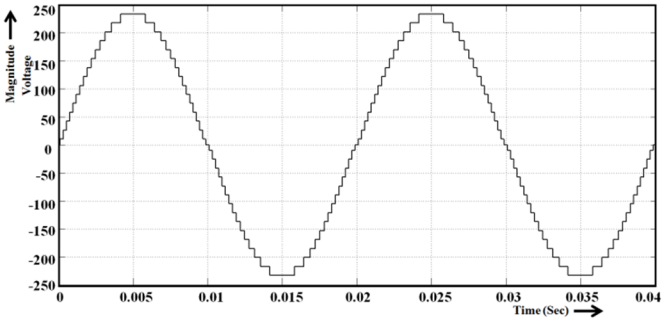

Fig. 9. Asymmetrical topology Output voltage with NLC.

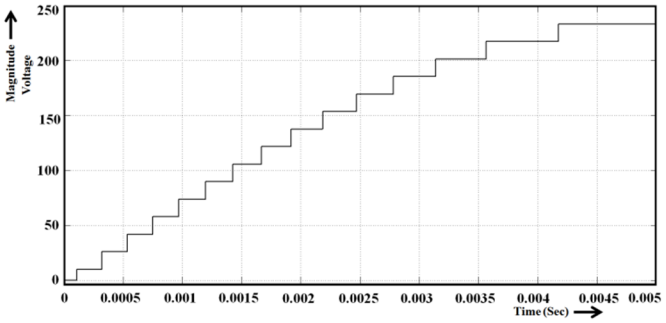

Fig. 10. Asymmetrical topology Output voltage Level Pattern.

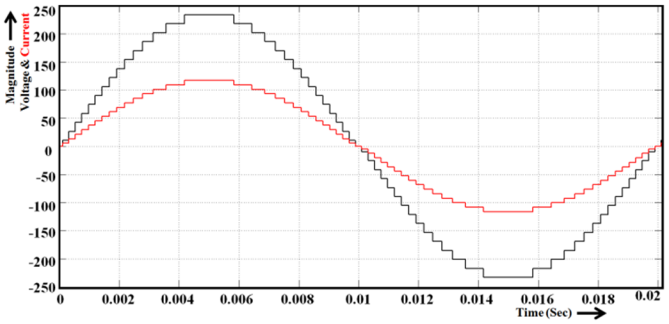

Fig. 11. Current (red) and Voltage (black) signals of Asymmetrical topology with NLC.

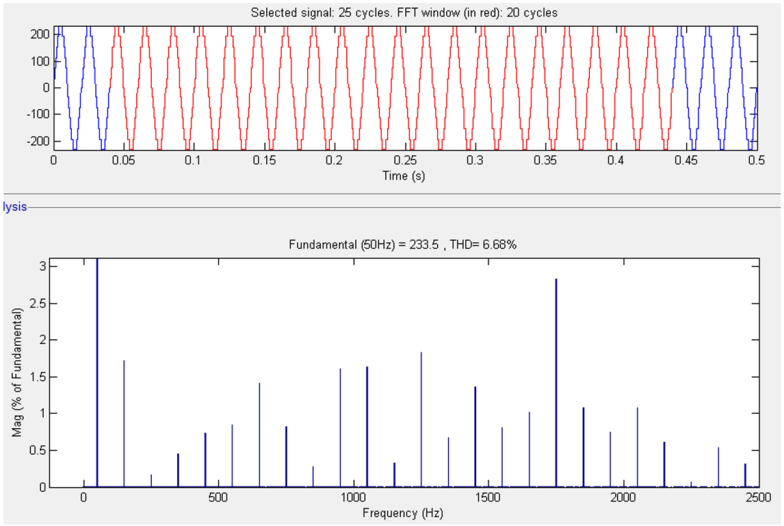

Fig. 12. FFT Harmonic analysis of Voltage signal of Symmetrical inverter topology.

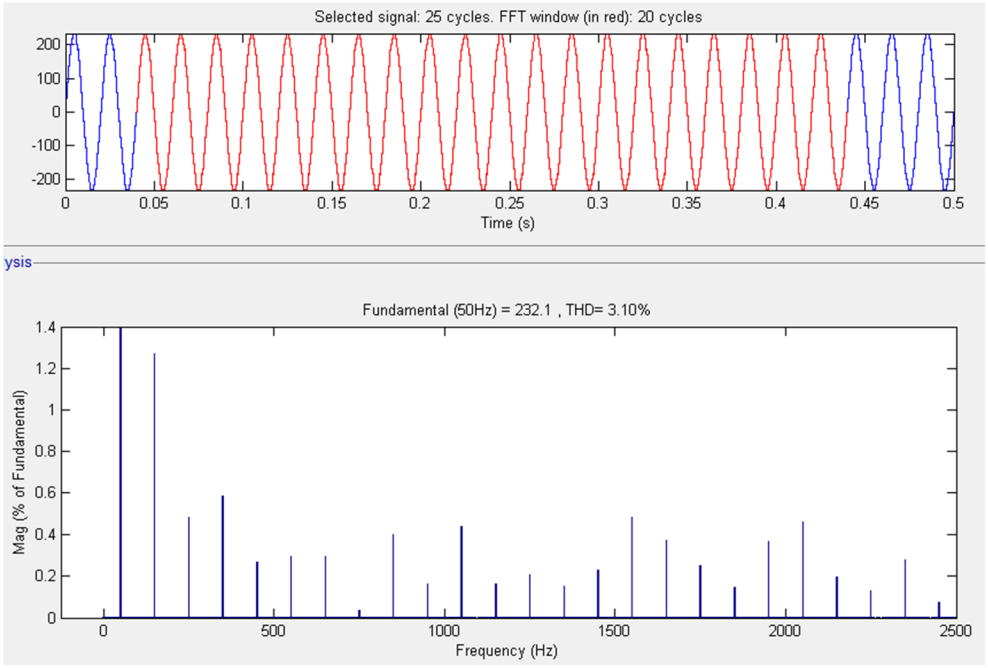

Fig. 13. FFT Harmonic analysis of Voltage signal of Asymmetrical inverter topology.

By observing the comparative waveforms and the data related to the performance parameters, normally the asymmetrical multilevel inverter is used to get the more number of levels but the NLC modulation is used to get the lower harmonic distortions and the implementation flexibility of the configuration as preferred. Form the Figs. 6 - 8 describes the symmetrical multilevel inverter related NLC patterned output voltage waveforms. Fig. 7 will provides the clear view of symmetrical levels and more over the Table 1 shows the switching pattern of NLC switching logic, by observing those switching states of switches S_9 and S_{10} both have no changes in states of operation. So two switches of the symmetrical configuration is can be eliminated and it does nit effects the output and operation. Asymmetrical configuration of multilevel inverter with NLC modulation output waveforms and the level pattern are shown from Figs. 9 – 11. The one of the way to evaluate the performance of the system is by the THD, the FFT harmonic analysis of voltage signals of symmetrical multilevel inverter is shown in Fig. 12 and asymmetrical multilevel inverter is shown in Fig. 13.

III. CONCLUSION

The simulation results mainly shows the implementation feasibility of preferred configuration of Series connected Sub-Multilevel Inverter with the Nearest Level Control modulation. By the analysis of the simulation results the symmetrical topology will provides the 13 level and the asymmetrical topology gives the 31 levels in the inversion processes of inverter. The FFT analysis for the THD of voltage signal for the symmetrical and asymmetrical are 6.68% and 3.10% respectively.

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