

Implementation of Carry Select Adder using CMOS Full Adder

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Abstract— In the recent year, many other new circuits are proposed using less number of transistors with less delay and very low power requirement. An adder with 10 transistors an adder with 8 transistors do not give full swing outputs for all input combinations and there is difference in output level for different combinations and these circuits have very low driving capabilities. Some other circuits are also proposed in but they do not give full swing output for all input combinations and power requirement is more. And these adders are not considered due to they do not provide full swing output. The Full Adder is designed using hybrid CMOS logic style by dividing it in three modules so that it can be optimized at various levels.[1] First module is an XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously and have a good driving capability. It also consumes minimum power and provides better delay performance. Second module is sum circuit which is also a XOR circuit and uses carry input and the output of the first module as input to generate sum output. Third module is a carry circuit which uses the output of the first stage and other inputs to generate carry output. In the new full adder design new full adder circuit is proposed which reduce the power consumption, delay between carry out to carry in and PDP by 12 to 100%. Simulations are carried out on HSPICE using TSMC 0.12 μ m CMOS technology. So far designing the high performance arithmetic circuits minimization of the power and delay of the full adder circuit is required. This gives a new carry select full adder using this cmos full adder.

Keywords: HSPICE, TSMC, CMOS FullAdder, XOR, XNOR Modules.

I. INTRODUCTION

The new design of low power CMOS Full Adder has been designed and XOR and XNOR modules are playing the vital role for designing the carry select full adder. Several logic styles for designing the Full adder have been proposed. In classical design of full adder normally single CMOS structure is used for the whole design, Such as the standard static CMOS full adder is based on regular CMOS structure with conventional pull-up and pull-down [5] transistors providing full swing output and good driving capabilities but the main drawback of this circuit is high input capacitance and use of large no. of PMOS, due to which the speed of this structure is degraded. The speed of dynamic CMOS logic style adder is higher. It has several demerits such as charge sharing, high clock load, higher switching activities and lower noise immunity and it requires high power for driving the clock

lines. Another logic styles are transmission-gate full adder (TGA) and transmission function full adder (TFA) based upon transmission gates and transmission function theory. These full adders are very low power consuming, but have very low driving capabilities. Full adder is a basic building block for various arithmetic circuits such as multipliers, compressors, comparators and so on. The power requirement and output delay of these circuits is greatly depending upon the power requirement and delay of the full adder circuits. So for designing the high performance arithmetic circuits, minimization of the power and delay of the full adder circuit is required.

II HYBRID –CMOS LOGIC DESIGN

In hybrid-CMOS architecture,[3] the XOR and XNOR A of and B inputs as the intermediate signal at the output of module I. These input signals and C_{in} are available for the input of module II and module III. So a new expression for sum and carry using XOR output H and XNOR output H_q . Let us discuss in detail about the 3 Modules.

i).Module-I

This circuit is widely used in hybrid CMOS logic style. This circuit requires low power and provides low delay and due to the feedback transistors at the output connected with supply voltage and ground provide good driving capability. But some combination of inputs such as “00” and “11” it provides little bit higher delay. When H will be at logic 0 H' will be at logic 1, both transistors will be on and output will be connected to C_{in} . So when C_{in} will be at logic ‘1’ output will be connected to logic ‘1’ and when it will be at logic ‘0’ output will also be connected to logic ‘0’.

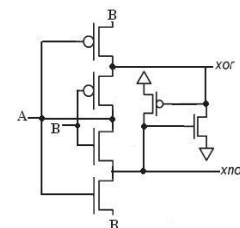


Fig.1 Module I circuit (a)

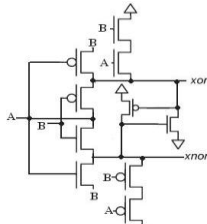


Fig.2 Module I circuit (b)

Both the transistors will be in off state for H to be at logic '1'. When the inputs H and C_{in} will be at logic '1', then the output is low, it is implemented by connecting two NMOS in series with their gate terminals connected to H and C_{in}, source terminal of one of the NMOS is connected to the grounded and the source terminal of other is connected to the output . Similarly, when H is at logic '1' and C_{in} is at logic '0', the output is at logic 1 so we use two PMOS in series with source terminal of one of the PMOS at logic high, drain terminal of other PMOS at output and the gate terminals are connected with H and C_{in} respectively.

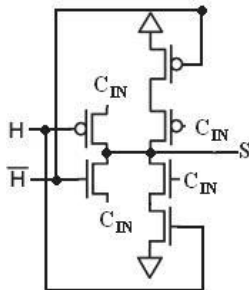


Fig.3 Module I circuit (c)

When both inputs will be at logic '1' then output will be connected to ground and the output will be at logic '0', when H will be at logic '1' and C_{in} will be at logic '0' both inputs H₀ and C_{in} will be at logic '0' and both transistor will be on and output will be connected to power supply and we get logic '1' at the output.

ii).Module-II

In the designing of circuit we try to avoid the use of inverters to reduce the power consumption and the logic high passes by PMOS while Logic low passes by NMOS to get the minimum delay .

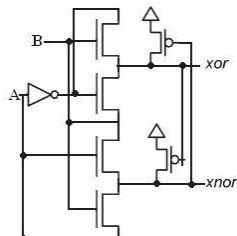


Fig.4 Module II Proposed circuit (c)

iii).Module-III

Module III circuit is a multiplexer which select C_{in} if H is at logic '1' else selects A or B as the output C_{out} . In the proposed circuit we use transmission gate with H and H'at the gate terminals of NMOS and PMOS[2] respectively to pass the C_{in} to C_{out} for H at logic high or when other inputs A and B are at different logic level. When the H is at logic '0' or

both inputs A and B are at same logic level we have to pass any of these inputs to the output. So we use one PMOS and one NMOS to pass input A by one transistor and other input B by another transistor. By the use of these two inputs from two sides it improves the performance of the circuit.

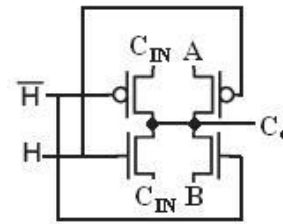


Fig.5 Module III Proposed circuit

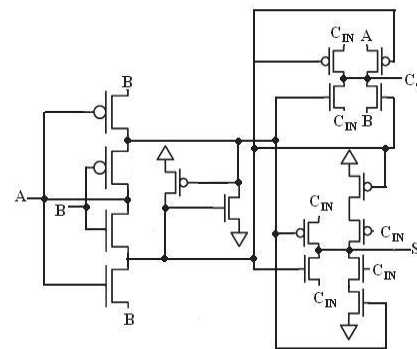


Fig . 6 Proposed Full Adder Circuit

III PASS TRANSISTOR BASED FULL ADDER

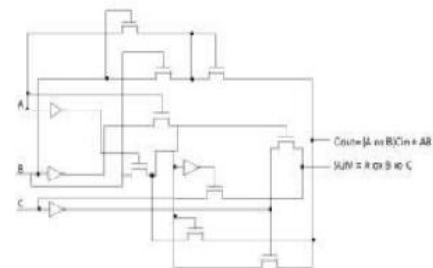


Fig. 7 Full Adder

A basic full adder has three inputs and two outputs which are sum and carry. Full adder cell is designed with CPL and Multiplexing Control Input technique for both sum and carry operations. The Sum and Carry operations are based on the equations 1 & 2 mentioned below:

$$\text{Sum} = A \oplus B \oplus C \quad (1)$$

$$\text{Carry} = (A \oplus B)C + AB \quad (2)$$

Sum equation contains XOR gates whose design using CPL logic is desired for low power system, whereas the Carry is designed as per equation.The inputs A, A's complement (A'), B, and B's complement (B') are fed to the pass transistors and forms an XOR logic gate. These four inputs construct an XOR logic operation at the transistor level, which is designed using two transistors.

To reduce the number of transistors, the output of the XOR gate ($A \oplus B$) is fed through a NOT gate from the differential node to the pass transistors as a control input. Whereas, C_{in} is treated as variable input, that is fed through the pass transistor source terminal. At this point, the functionality performed by the circuit is equivalent to the sum operation, $sum\ A \oplus B \oplus C$, and six transistors have been used. As mentioned earlier, the number of transistors in the carry operation can be reduced by taking $A \oplus B$ as the input from the sum operation circuit AND with C_{in} in order to produce the operation equivalent to $(A \oplus B)C_{in}$, which only uses another two transistors. Meanwhile, the inputs $A, A', B,$ and B' are fed into pass transistors in order to produce an AND logic gate, that represents the AB operation. The dissipation of power which occurs during the active mode of the circuit is active power. This active power consists of dynamic power as well as the static power. It is measured by giving input vectors to the circuit, then calculating the average power dissipation and comparing the result with the base adder i.e. conventional 1-bit CMOS

IV CARRY SELECT ADDER

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n -bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known [8]. The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $\lfloor \sqrt{n} \rfloor$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

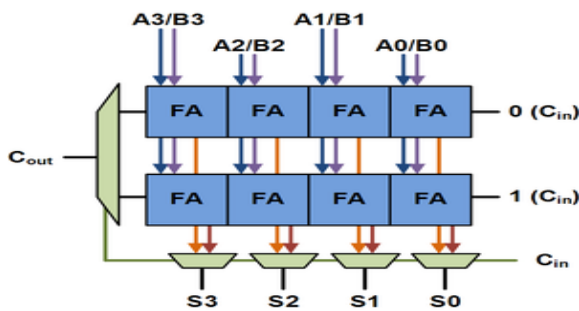


Fig.8 4-bit Carry Select Adder

V THE NEW FULL ADDER

The new improved 14T adder cell requires only 14 transistors to realize the adder function shown in figure 4.10. It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell. Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem, which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate.

The newly proposed adder implement the Sum using XNOR-XNOR and C_{out} using PMOS – NMOS. We can also build to produce C_{out} using NMOS-NMOS and PMOS-PMOS. But the delay and power dissipation of PMOS-NMOS is better than other two kinds of producing C_{out} . The proposed XNOR gate is designed by putting inverter at the output of the XOR gate in order to improve the threshold loss problem, which exists in the SERF adder. Out of the three methods, PMOS-NMOS based C_{out} gives the better result in power, speed and threshold loss problem.

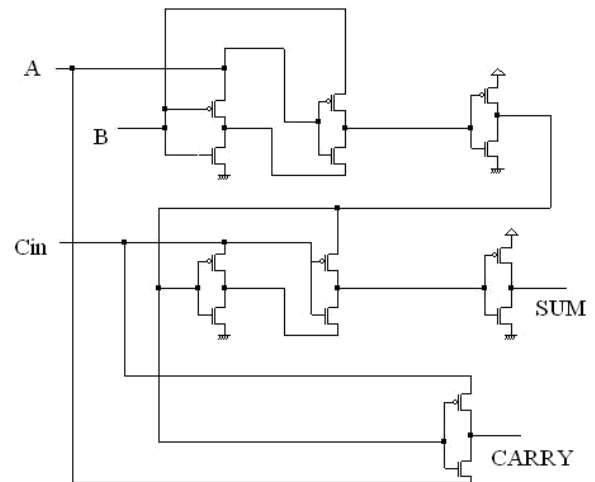


Fig 9. Structure Of New Full Adder

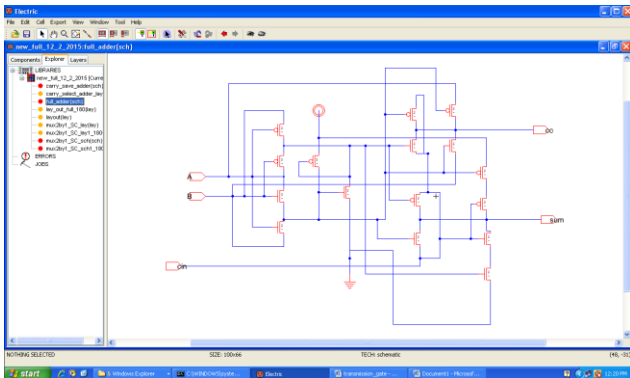
Totally eight adders including the SERF adder are taken for comparison with the newly proposed adder. These adders are compared with respect to their power consumption and total delay by providing all the possible input vector combinations. The results proved that the newly proposed adder is efficient as it consumed the least power and eliminated the threshold loss problem. The present research work has presented a new improved 14T adder cell to construct full adders using only 14 transistors. Based on our extensive simulations, the new improved 14T adder cell consume considerably less power in the order of micro watts and has 48% higher speed and reduces 50% threshold loss problem compared to the previous different types of transistor adders.

VI LTSPICE TOOL

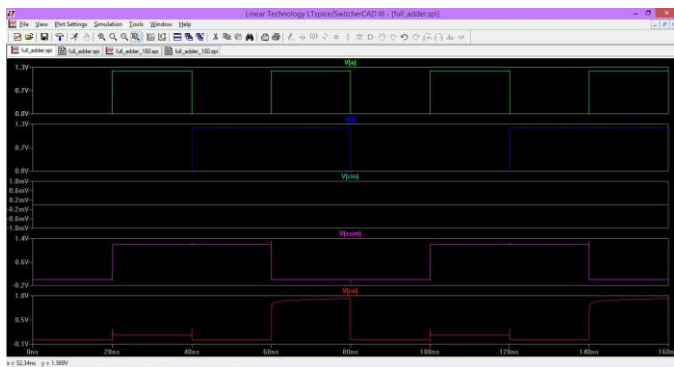
The simulation and synthesis are carried out for all the designs. The performance evaluation of existing adder designs and the proposed adder designs is carried out using LT SPICE tool in 180 nm and 130 nm technology. All the parameters such as delay, area, total power, and power-delay product are tabulated.

LTspice is a high performance SPICE simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulators. Our enhancements to SPICE have made simulating switching regulators extremely fast compared to normal SPICE simulators, allowing the user to view waveforms for most switching regulators in just a few minutes. Included in this download are LTspice , Macro Models for 80% of Linear Technology's switching regulators, over 200 op amp models, as well as resistors, transistors and MOSFET models.

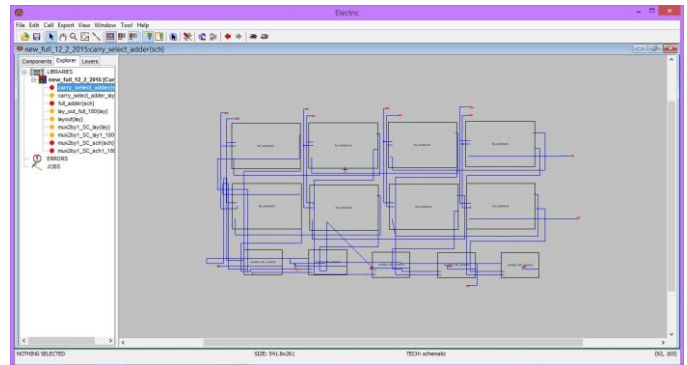
VII SIMULATION RESULTS



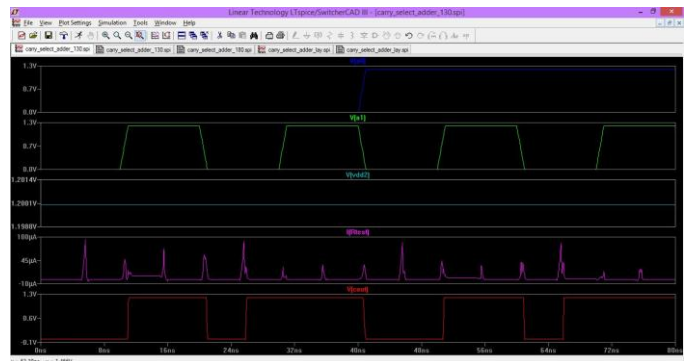
Full adder Schematic



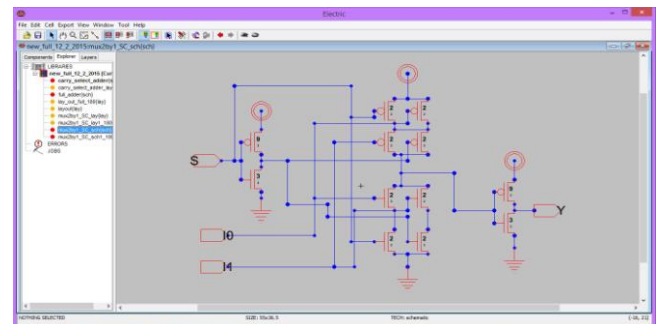
Simulation Result of Fulladder



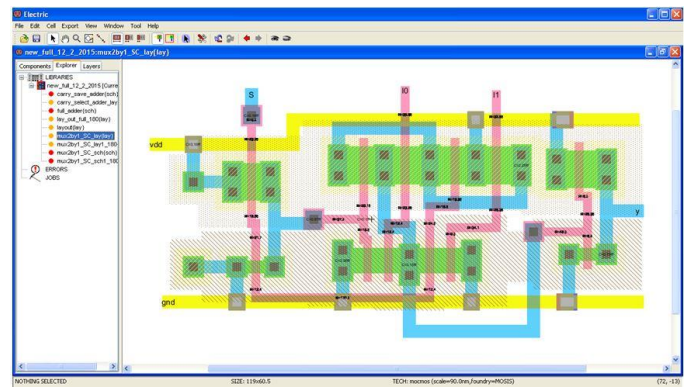
Carry select adder Schematic



Simulation Result of carry select adder



Final Schematic Of Mux 2_1



Final Layout Of Mux 2_1

VIII TABLE

	FULL ADDER OF 180 NM	FULL ADDER OF 130NM
POWER(uw)	1.5168	0.036
DELAY SUM	0.1025	0.075
DELAY CARRY	0.115	0.094
PDP SUM	0.155472	0.027
PDP CARRY	0.174432	0.03384

VIII CONCLUSION

Hybrid-CMOS design style gives more freedom to the designer to select different modules in a circuit depending upon the application. Using the adder categorization and hybrid-CMOS design style, many full adders can be designed. For example, a novel full adder designed using hybrid-CMOS design style is presented in this paper that targets low PDP. The proposed hybrid-CMOS full adder has better performance than most of the standard full-adder cells owing to the novel design modules proposed in this paper. It performs well with supply voltage ranging from 1.2V to 2.4V. When embedded in a parallel adder chain, it outperforms all the other adders making it suitable for larger arithmetic circuits.

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