Implementation of Cascade Amplifier in 180nm CMOS Technology

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Abstract

This paper described about the complete analysis and design of common source amplifier designed for application in a capacitive-micro machined-ultrasonic-transducer (CMUT) based intravenous imaging system. These CMUTs have recently gained much interest due to their numerous advantages as ultrasound transducers that can be integrated with electronics on silicon and are compact. In this paper the workability of the feedback biasing cascade amplifier circuit configurations has been analysed and tested experimentally using PSPICE and MATLAB simulation tool. It has been found that the new propositions have improved performance such as gain and bandwidth. The results have been taken on 180nm technology. It gives the derivations of all the equations described in the paper like, closed loop gain of negative feedback amplifier, transfer function, drain current equation, stability factor, FOM etc. The Simulation result of the CS amplifier with feedback biasing in 180nm CMOS technology using PSPICE and compared this with the MATLAB plot of the transfer function of the same.

Keywords-Cascade amplifier, CMUT, CLOSED loop gain and bandwidth, stability factor, CS amplifier, 180nm CMOS technology.

1. Introduction

The Nanoscale technologies can be a viable option for the analog circuitry as well. Some of the features of Nanoscale technologies that are otherwise not desirable to an analog designer may actually be useful in some circuit techniques, as we will show in this brief for the case of feedback biasing. Even though a feedback-biasing scheme is simple and ensures that the input MOSFET remains in saturation, irrespective of the process and temperature variations, its biggest disadvantage has been the limited voltage swing. We show that this disadvantage vanishes as one move to Nanoscale technologies [1]. Simulation and experimental results [1], presented therein for validation of the ideas, were for Feedback biased Cascade amplifier designed for application in a capacitive-micro machined-ultrasonic-transducer (CMUT) based intravenous imaging system. A number of works on CMUT operation and applications are available. Application of ultrasonic imaging fields such as dermatology,ophthalmology and cardiovascular medicine require very high frequency resolution. CMUTs can be made for high frequency operation. CMUT is an appropriate technology for building very high frequency arrays. A linear array of high voltage pulsar and amplifier circuits has also been designed for use with an array of CMUTs to enable real time imaging applications [7]. Due to the requirement of having an array of several transducers with local signal conditioning on a catheter tip for performing imaging inside the human arteries, the compactness of the circuitry is of utmost importance, followed by the constraint on the power consumption of the system. It is for this reason that a cascade amplifier topology is designed for this application, as the cascade amplifier is one of the most efficient amplifier stages that can be realized in CMOS technology [6]. To realize the biasing within a very small area sub threshold MOSFETs as high-value resistors have been employed to bias amplifiers [1]. The article rediscovers the attractiveness of feedback biasing when applied to circuits designed in Nanoscale CMOS technologies. It is shown that very compact amplifiers can be obtained by utilizing a type of biasing that imposes minimal area overhead. It presents measurement results of common-source (CS) amplifiers using feedback biasing designed for application in a capacitive micro machined ultrasonic transducer 30MHz (CMUT). The proposed feedback biasing is also suitable for amplifying signals from high impedance sources that pose challenges on maintaining high input impedance for the voltage amplifiers while maintaining a very low input capacitance value. Here CMUTs can be integrated with electronics on silicon and are compact.

The basic idea behind the cascade amplifier is it can be designed to increase the DC gain and the gain-bandwidth. We have presented feedback biased cascade amplifier, to increase the overall gain and bandwidth simultaneously. The paper discovers the attractiveness of feedback biasing when applied to circuits designed in NanoscaleCMOS technologies. Utilizing a type of biasing very compact amplifiers can be obtained that cover minimum area in the NanoscaleCMOS technologies where the biasing point has found to be more stable

The proposed feedback biasing is also suitable for amplifying signals from high impedance sources that pose challenges on maintaining high input impedance for the voltage amplifiers while maintaining a very low input capacitance

value. The amplifiers were fabricated in 180-nm CMOS technology and measured to be just 20µm x 10µm.

2. FEEDBACK BIASING IN NANOSCALE CMOS TECHNOLOGIES

The four basic feedback topologies

1. **Voltage amplifiers**: - It amplifies an input voltage signal and provides an output voltage signal. A suitable feedback topology for the voltage amplifier is the voltage-mixing
2. **Current amplifiers**: - It amplifies an input current signal and provides an output current signal. A suitable feedback topology for the current amplifier is the current-mixing current sampling.
3. **Trans conductance amplifiers:** - It amplifies an input voltage signal and provides an output current signal. A suitable feedback topology for the Trans conductance amplifier is the voltage-mixing current sampling. It is also called as series-series feedback. We have used Tran conductance amplifier for our amplifier.
4. **Trans resistance amplifiers:** - It amplifies an input current signal and provides an output voltage signal. A suitable feedback topology for the Trans resistance amplifier is the current-mixing voltage sampling. It is also called as shunt-shunt feedback

3. BASIC ANALYSIS OF FEEDBACK BIASING

A) DC Analysis

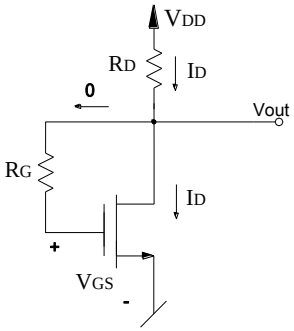

Fig.1NMOS with feedback biasing

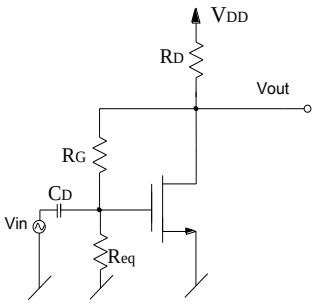

Fig.2 when used as a voltage amplifier with a low impedance source.

- DC Analysis Equations

$V_{DD} - I_D R_D - V_{DS} = 0$ (1)

$V_{DD} = I_D R_D + V_{DS}$

$V_{DD} - I_D R_D - V_{GS} = 0$ (2)

$V_{DD} = I_D R_D + V_{GS}$

After comparing equation (1) & (2)

$I_D R_D + V_{DS} = I_D R_D + V_{GS}$

$V_{DS} = V_{GS}$ (3)

i.e. Output voltage is controlled by Input voltage.

In above fig.1, the voltage drop across R_G is zero & $I_G = 0$.

Output is taken across V_{DS},

So V_{DS} = Vout i.e. Vout = V_{GS} (4)

We know $V_{DS} = V_{GS}$ so put it in equation no. (1)

$V_{DD} = I_D R_D + V_{DS}$

$V_{DD} = I_D R_D + V_{GS}$

$V_{DD} = V_{GS} + I_D R_D$ (5)

Next we have to drive the equation:-

$V_{OUT\_MIN} \equiv V_{DS\_MIN} \approx V_{GS\_MAX} - V_T$

As we know V_T = Threshold voltage.

The value of V_{GS} at which a sufficient no. of mobile electrons accumulates in the channel region to form a conducting channel is called the "Threshold Voltage". Its value varied between 0.5 to 1.0 V.

When $V_{GS} = V_T$(induced channel), but at this point I_D (drain current) is usually very small.

As $V_{GS} > V_T$, increased conductance, & reduce resistance.

In fact the conductance of channel is proportional to the "excess gate voltage ($V_{GS} - V_T$)" also known as the "Effective voltage or the Overdrive voltage."

It follows that the current I_D will be proportional to $V_{GS} - V_T$ and of course to the voltage V_{DS} that causes I_D to flow.

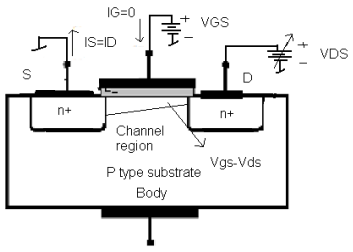

Fig.3 Operation of enhancement NMOS Tr.

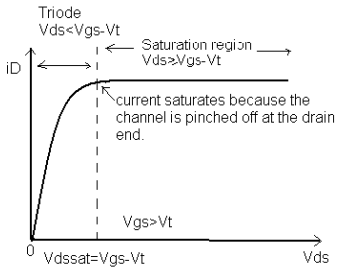

Fig.4 I_D versus V_{DS} plot for enhancement type NMOS Tr.

When V_{DS} increased that reduces the voltage between gate and drain end to V_T,

I.e. $V_{GD} = V_T$

Or

$V_{GS} - V_{DS} = V_T$

$V_{DS} = V_{GS} - V_T$

The channel depth at the drain end decreased to almost zero, and the channel is said to be "Pinched off" at this point it enters the saturation region of operation. The voltage V_{DS} at which saturation occurs is denoted V_{DSsat},

$V_{DSsat} = V_{GS} - V_T$

Or

$$V_{OUT\_MIN} \equiv V_{DS\_MIN} \approx V_{GS\_MAX} - V_T \quad (6)$$

Bias Point calculation

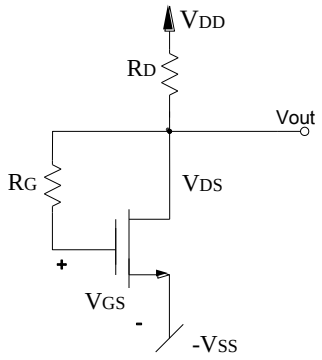

Fig. 5 NMOS with feedback biasing

$$V_{DD} - I_D R_D - V_{DS} - V_{SS} = 0$$
$$V_{DD} = I_D R_D + V_{DS} + V_{SS} \quad (7)$$

Put $V_{DS} = V_{GS}$

$$V_{DD} - I_D R_D - V_{GS} - V_{SS} = 0$$
$$V_{DD} = I_D R_D + V_{GS} + V_{SS} \quad (8)$$

From equ.no.(7) plot DC load line to obtain the given equation:-

$$V_{OUT\_MIN} = \frac{V_{DD}-V_{SS}}{2} - V_T$$

Put $I_D = 0$

$V_{DD} = V_{DS} + V_{SS}$

$$I_D = \frac{V_{DD}-V_{SS}}{R_D}$$

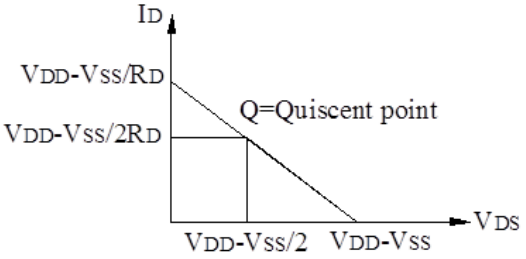

Fig.6 DC load line

For faithful amplification the quiescent point Q will be on the middle of the load line.

$$\text{So } V_{OUT\_MIN} = \frac{V_{DD}-V_{SS}}{2} - V_T \quad (9)$$

$$\text{Where } \frac{V_{DD}-V_{SS}}{2} = V_{GS\_MAX}$$

Equ.no. (9) is the minimum output voltage to give the faithful amplification.

Assume amplifier gain is high i.e. $A_V = \frac{V_2}{V_1}$ is high.

It means that the value of V_1 should be kept low in order to not clip off the input voltage.

When Q shifted towards the y-axis i.e. I_D side, the positive peaks of the output signal would be clipped off, because the MOSFET would turn off for part of the cycle. It is called as the circuit not having sufficient headroom.

When Q shifted towards the x-axis i.e. V_{DS} side, the output signal is distorted. It is called as the circuit not having sufficient legroom.

B) HIGH FREQUENCY ANALYSIS OF FEDDBACK BIASING

At high frequency we include the internal MOSFET capacitance also.

And at high frequency the feedback biasing figure is also improved

Here, $C_{GD}=C_G$; $C_{GS}=C_{IN}$; $C_{DS}= C_L$

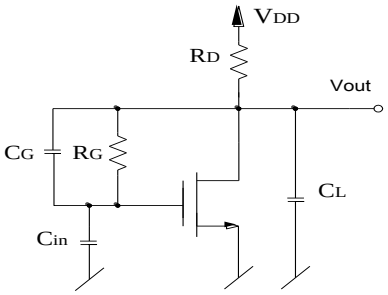

Fig.7(a) Schematic showing a feedback biased amplifier, with important impedances shown

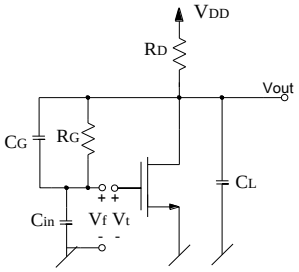

Fig. 7(b) Feedback loop is broken to calculate the loop gain

MOSFET CAPACITANCES

Based on their physical origins, the parasitic device capacitance can be classified into two major groups:

(1) Oxide related capacitances: - The two overlap capacitances that arise as a result of this structural arrangement as shown in figure (8) are called C_{GD} (overlap) and C_{GS} (overlap). They are voltage independent.

(2) Junction capacitances: - The voltage dependent source-substrate and drain-substrate junction capacitance are, C_{SB} and C_{DB}.

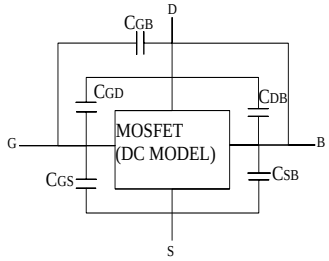

Fig. 8 Lumped representation of the parasitic MOSFET capacitances

Here, $C_{GD}=C_G$; $C_{GS}=C_{IN}$; $C_{DS}= C_L$

In order to obtain this loop gain response we have to make the high frequency model of this feedback biasing method.

High frequency analysis (equivalent circuit)

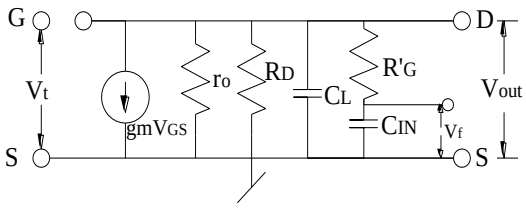

Fig. 9 (a) High frequency model of the circuit

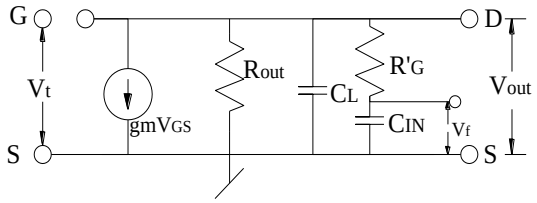

Fig. 9(b) High frequency model of the circuit

Gm = Transconductance of the MOSFET. The control that the V_{GS} has over the I_D is measured by

$$Gm = \frac{I_D}{V_{GS}} \text{ constant } V_{DS}.$$

Fig. 2.9(b) is used to calculate the loop gain response of the feedback, as expressed in [1].

$$LG(s) = -\frac{V_f(s)}{V_t(s)}$$

$$= -gm\left(R_{out}\|\frac{1}{sC_L}\right)\left(\frac{\frac{1}{sC_{IN}}}{R_G\|\frac{1}{sC_G}+\frac{1}{sC_{IN}}}\right)$$

$$LG(s)= -gm\frac{R_{out}}{1+sR_{out}C_L}\frac{\frac{1}{sR_GC_G}}{1+sR_G\left(C_G+C_{IN}\right)} \quad (10)$$

Apply KCL

$$Vout\left[\frac{1}{R_{out}}+sC_L+\frac{1}{Z}\right]= -gmV_{GS}$$

Where $$Z= R'_{G+}\frac{1}{sC_{IN}}$$

$$Z= \frac{sR'_GC_{IN}+1}{sC_{IN}}$$

& R`G = RG‖CG & Rout = ro‖RD

$$Vout\left[\frac{1}{R_{out}}+sC_L+\frac{sC_{IN}}{sR'_GC_{IN}+1}\right]=-gmV_{GS}$$

$$Vout\left[\frac{1(sR'_GC_{IN}+1)+sC_LR_{out}(1+R'_GC_{IN})+sC_{IN}R_{out}}{R_{out}(sR'_GC_{IN}+1)}\right]=-gmV_{GS}$$

$$Vout\left[(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}\right]=-gmV_{GS}R_{out}(sR'_GC_{IN}+1)$$

$$Vout=\frac{-gmV_{GS}R_{out}(sR'_GC_{IN}+1)}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}$$

$$\frac{Vout}{Vin}=\frac{-gmV_{GS}R_{out}(sR'_GC_{IN}+1)}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}$$

$$R'G=RG\|CG=\frac{R_G}{sR_GC_G+1}$$

$$\frac{Vout}{Vin}=\frac{-gmRout\left(1+\frac{sR_GC_{IN}}{sR_GC_G+1}\right)}{\left(1+\frac{sR_GC_{IN}}{sR_GC_G+1}\right)(1+sC_LRout)+sC_{IN}Rout}$$

$$\frac{Vout}{Vin}=\frac{-gmRout\left(\frac{sR_GC_{IN}+sR_GC_G+1}{sR_GC_G+1}\right)}{\left(\frac{sR_GC_{IN}+sR_GC_G+1}{sR_GC_G+1}\right)(1+sC_LRout)+sC_{IN}Rout}$$

$$\frac{Vout}{Vin}=\frac{-gmRout\left(\frac{sR_GC_{IN}+sR_GC_G+1}{sR_GC_G+1}\right)}{\frac{(sR_GC_{IN}+sR_GC_G+1)(1+sC_LRout)+sC_{IN}Rout(sR_GC_G+1)}{(sR_GC_G+1)}}$$

$$\frac{Vout}{Vin}=\frac{-gmRout(sR_GC_{IN}+sR_GC_G+1)}{(sR_GC_{IN}+sR_GC_G+1)(1+sC_LRout)+sC_{IN}Rout(sR_GC_G+1)}$$

$$\frac{Vout}{Vin}=\frac{-gmRout-sgmRoutR_GC_{IN}-sgmRoutR_GC_G}{s^2(R_GC_{IN}C_LRout+R_GC_GC_LRout+C_{IN}RoutR_GC_G)+s(R_GC_{IN}+R_GC_G+C_LRout+C_{IN}Rout)+1}$$

$$\frac{Vout}{Vin}=\frac{-gmRout-sgmRout(R_GC_{IN}+R_GC_G)}{s^2(R_GC_{IN}C_LRout+R_GC_GC_LRout+C_{IN}RoutR_GC_G)+s(R_GC_{IN}+R_GC_G+C_LRout+C_{IN}Rout)+1}$$

(3.19)

Vf(s) = Feedback voltage

Vt(s) = Input voltage

$$\frac{Vf(s)}{Vt(s)}=\frac{-gmR_{out}(1+sC_GR_G)}{(sR_G(C_{IN}+C_G)+1)(1+sC_LR_{out})}$$

& VOUT = $Io\left(R'_G+\frac{1}{sC_{IN}}\right)$

$$Io\left(R'_G+\frac{1}{sC_{IN}}\right)=\frac{-gmV_{GS}R_{out}(1+sC_{IN}R'_G)}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}$$

$$Io\frac{(sR'_GC_{IN}+1)}{sC_{IN}}=\frac{-gmV_{GS}R_{out}(1+sC_{IN}R'_G)}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}$$

$$Io=\frac{-gmV_{GS}R_{out}(1+sC_{IN}R'_G)}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}\times\frac{sC_{IN}}{(sR'_GC_{IN}+1)}$$

$$Io=\frac{-gmV_{GS}R_{out}sC_{IN}}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}$$

&Vf = IO × $\frac{1}{sC_{IN}}$

$$Vf(s)=\frac{-gmV_{GS}R_{out}sC_{IN}}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}\times\frac{1}{sC_{IN}}$$

Where $V_{GS}=V_t$

$$Io=\frac{-gmV_{GS}R_{out}(1+sC_{IN}R'_G)}{(sR'_GC_{IN}+1)(1+sC_LR_{out})+sC_{IN}R_{out}}\times\frac{sC_{IN}}{(sR'_GC_{IN}+1)}$$

We know R`G = $R_G \| C_G$

$$=\frac{R_G\times 1/sC_G}{R_G+1/sC_G}=\frac{R_G}{sR_GC_G+1}$$

$$\frac{Vf(s)}{Vt(s)}=\frac{-gmRout}{\left(\frac{sR_GC_{IN}}{sR_GC_G+1}+1\right)(1+sC_LRout)+sC_{IN}Rout}$$

$$\frac{Vf(s)}{Vt(s)}=\frac{-gmRout}{\left(\frac{(sR_GC_{IN}+sR_GC_G+1)(1+sC_LRout)+sC_{IN}Rout(sR_GC_G+1)}{(sR_GC_G+1)}\right)}$$

$$\frac{Vf(s)}{Vt(s)}=\frac{-gmRout(sR_GC_G+1)}{(sR_GC_{IN}+sR_GC_G+1)(1+sC_LRout)+sC_{IN}Rout(sR_GC_G+1)}$$

Now divide numerator and denominator by $sC_{IN}R_{out}(1+sR_GC_G)$

$$\frac{Vf(s)}{Vt(s)} = \frac{-gmR_{out}(1+sR_GC_G)\Big/(sC_{IN}R_{out}(1+sR_GC_G))}{\frac{(1+sR_GC_G+sC_{IN}R_G)(1+sR_{out}C_L)}{sC_{IN}R_{out}(1+sR_GC_G)}+\frac{sC_{IN}R_{out}(1+sR_GC_G)}{sC_{IN}R_{out}(1+sR_GC_G)}}$$

$$\frac{Vf(s)}{Vt(s)} = \frac{-\left(\frac{gm}{sC_{IN}}\right)(sC_{IN}R_{out}(1+sR_GC_G))}{(1+sR_GC_G+s^2C_{IN}R_G)(1+sR_{out}C_L)}$$

$$\frac{Vf(s)}{Vt(s)} = \frac{-gmR_{out}(1+sR_GC_G)}{(1+sR_G(C_G+C_{IN}))(1+sR_{out}C_L)}$$

$$\frac{Vf(s)}{Vt(s)} = \frac{-gmR_{out}}{(1+sR_{out}C_L)} \times \frac{1+sR_GC_G}{1+sR_G(C_G+C_{IN})} \quad (11)$$

$$\frac{Vf(s)}{Vt(s)} = \frac{-gmR_{out}-sgmR_{out}R_GC_G}{s^2(R_GR_{out}C_GC_L+R_GR_{out}C_LC_{IN})+s(R_{out}C_L+R_GC_G+R_GC_{IN})+1}$$

or

$$\frac{Vf(s)}{Vt(s)} = \frac{-gmRout}{\left(\frac{sR_GC_{IN}}{sR_GC_G+1}+1\right)(1+sC_LRout)+sC_{IN}Rout}$$

$$\frac{Vf(s)}{Vt(s)} = \frac{-gmR_{out}-sgmR_{out}R_GC_G}{s^2R_GR_{out}(C_GC_L+C_LC_{IN}+C_{IN}C_G)+s(R_{out}C_L+R_GC_G+R_GC_{IN}+R_{out}C_{IN})+1}$$

(12)

Rechecking the above equation no. (12) from bottom to top,

$$LG(s) = -\frac{Vf(s)}{Vt(s)}$$

$$= gm\left(R_{out}\|\frac{1}{sC_L}\right)\frac{\frac{1}{sC_{IN}}}{R_G\|\frac{1}{sC_G}+\frac{1}{sC_{IN}}}$$

$$= gm\left(\frac{R_{out}\times\frac{1}{sC_L}}{R_{out}+\frac{1}{sC_L}}\right)\frac{\frac{1}{sC_{IN}}}{R_G\times\frac{\frac{1}{sC_G}}{R_{out}+1/sC_G}+\frac{1}{sC_{IN}}}$$

$$= gm\left(\frac{R_{out}\times\frac{1}{sC_L}}{R_{out}+\frac{1}{sC_L}}\right)\frac{\frac{1}{sC_{IN}}}{R_G\times\frac{\frac{1}{sC_G}}{R_{out}+1/sC_G}+\frac{1}{sC_{IN}}}$$

$$= gm\left(\frac{R_{out}}{1+sR_{out}C_L}\right)\frac{\frac{1}{sCIN}}{\frac{sR_GC_{IN}+(1+sR_GC_G)}{sC_{IN}(1+sR_GC_G)}}$$

$$= gm\left(\frac{R_{out}}{1+sR_{out}C_L}\right)\frac{(1+sR_GC_G)}{1+sR_G(C_G+C_{IN})}$$

$$LG(s) = \frac{Vf(s)}{Vt(s)} = -gm\left(\frac{R_{out}}{1+sR_{out}C_L}\right)\frac{(1+sR_GC_G)}{1+sR_G(C_G+C_{IN})} \quad (13)$$

The loop gain response has a dc gain (gmRout)

When $R_G >>$ Rout & C_L&C_{IN} are of the same order the dominant pole of the loop gain response is set by the RC product at the input node i.e. R_G (C_G + C_{IN}).

$$LG(s) = -gm\left(\frac{R_{out}}{1+sR_{out}C_L}\right)\frac{(1+sR_GC_G)}{1+sR_G(C_G+C_{IN})} = \frac{Zeros}{Poles}$$

Ist pole:

$1 + sR_G(C_G + C_{IN}) = 0$

$sR_G(C_G + C_{IN}) = -1$

$$s = \frac{-1}{R_G(C_G+C_{IN})} \quad (14)$$

IInd pole:

$(1 + sC_L\,Rout) = 0$

$sC_L\,Rout = -1$, $s = \frac{-1}{R_{out}C_L}$ (15)

Zeros:

$-g_m\,Rout(1+ sR_GC_G) = 0$

$1+sR_GC_G = 0$

$sR_GC_G = -1$

$$s = \frac{-1}{R_GC_G} \quad (16)$$

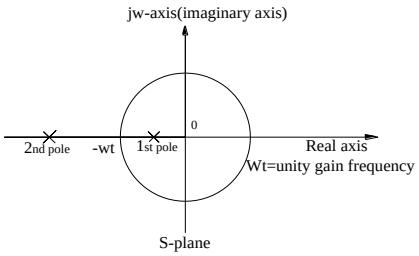

Fig. 10 Poles & Zero

Assuming that C_{IN}>> C_G, it lies at much higher frequencies than the dominant pole.So Ist pole is the dominant pole.Assuming the IInd pole is lies far beyond its unity gain frequency ft.One can estimate wt as the product of the dc gain & the frequency of the dominant pole i.e.

$$Wt = \frac{gmR_{out}}{R_G(C_G+C_{IN})} \approx \frac{gmR_{out}}{R_GC_{IN}} \qquad (17)$$

Where C_{IN}>>C_G

Ft = unity gain frequency

Dominant pole = It is the pole which is near to zero (origin) so that it dominate the amplifier frequency response; it is called a "Dominant pole".Check the stability of the system using Routh Hurwitz criterion:-

Let the equation $a_os^m + a_1s^{m-1} + \ldots\ldots\ldots\ldots + a_m = 0$

(1). All the coefficients of the equation should have same sign.

(2). There should be no missing term.

These two conditions are necessary to make the system stable.

Apply this criterion to our loop gain response LG(s):

$$LG(s) = -gm\left(\frac{R_{out}}{1+sR_{out}C_L}\right)\frac{(1+sR_GC_G)}{1+sR_G(C_G+C_{IN})}$$

$(1 + sC_L\ Rout)(1 + sR_GC_G + sR_GC_{IN}) = 0$

$S^2R_GRoutC_L\ (C_G + C_{IN}) + sR_G(C_G + C_{IN}) + 1 = 0$

S^2	$R_GRoutC_L(C_G + C_{IN})$	1
S^1	$R_G\ (C_G + C_{IN})$	0
S^0	1	

$$B1 = \frac{-1}{a1}\begin{vmatrix} a0 & a2 \\ a1 & a3 \end{vmatrix}$$

$$\text{So } B1 = \frac{-1}{R_G(C_G+C_{IN})}\begin{vmatrix} R_GR_{out}C_L(C_G+C_{IN}) & 1 \\ RG(C_G+C_{IN}) & 0 \end{vmatrix}$$

$$B1 = \frac{-1}{R_G(C_G+C_{IN})} \times \left[-R_G(C_G+C_{IN})\right]$$

B1 = 1

So all the coefficients in the first column are of the same sign (positive), the given equation has no roots with positive real part. Hence the system is stable. Since the input signal V_{IN} to the amplifier shown in Figure (3.13) (a) is capacitive coupled (By C_D) to the gate of the MOSFET. C_D forms a HPF (High pass filter) with R_{EQ}.

The loop gain is less than unity beyond the 3-dB frequency hence the feedback loop is disabled beyond this frequency and the amplifier operates effectively in open loop. Therefore the feedback loop while biasing the MOSFET does not interfere with the signals beyond W3dB.

Resistance R_{EQ} appears due to the miller effect at the gate of the MOSFET i.e.

$$R_{EQ} = \frac{R_G}{1-A_V} \qquad (18)$$

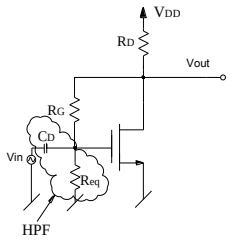

Fig. 11(a) When used as a voltage amplifier with a low impedance source.

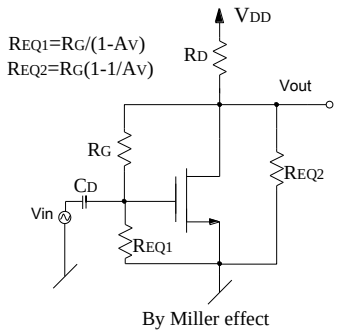

Fig.11(b) When used as a voltage amplifier with a low impedance source.

4. FIGURE OF MERIT DEFINITION

Next to drive the equation:

$$FOM = \left(\frac{Gm}{I_{DS}}\right)\times\left(\frac{Gm}{2\pi C_{GS}}\right)$$

FOM: Figure of merit= $A_V \times BW$

A_V = Voltage gain = $\frac{Vout}{Vin}$

BW = Bandwidth = $f_H - f_L$

fH = Higher cut off frequency

fL = Lower cut off frequency

At higher frequency analysis we take fH only

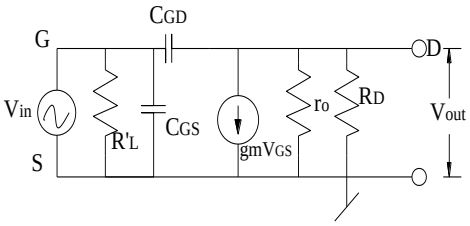

Fig. 12 Equivalent circuit to find the FOM

$$V_{out}\left[\frac{1}{R'L}\right] - V_{GS}(sC_{GD}) = -g_m V_{GS}$$

I_{GD} = small (so neglect it)

$V_{out} = -g_m V_{GS} R'D$

$R'D = rd||R_D$

$$I_{GD} = \frac{V_{GS}-V_{out}}{1/sC_{GD}} = sC_{GD}(V_{GS}-Vout)$$

$$=sC_{GD}[V_{GS}+gmR'LV_{GS}]$$

$$=sC_{GD}V_{GS}(1+gmR'L)$$

$Ceq = C_{GD}(1+gmR'L)$

By miller effect replace C_{GD}

$C_{IN} = C_{GS} + Ceq$

$C_{IN} = C_{GS} + C_{GD}(1+gmR'L)$

R'L occurs due to miller effect

$$R'L = \frac{R_G}{1-A_V}, \quad V_{out} = \frac{Vin\times\frac{1}{sC}}{R+\frac{1}{sC}}$$

$$V_{out} = \frac{Vin}{1+sCR}, \quad W_H = \frac{1}{CR}, \quad 2\pi f_H = \frac{1}{CR}$$

$$f_H = \left(\frac{1}{2\pi CR}\right), \quad A_V = \frac{Vout}{Vin}, \quad AV = -gmR'D$$

$$FOM = -gmR'D\times\frac{1}{2\pi C_{IN}R'_G}$$

$$\frac{R'_D}{C_{IN}R'_G} = \left(\frac{Gm}{2\pi C_{GS}}\right)$$

$$FOM = \left(\frac{Gm}{I_{DS}}\right)\times\left(\frac{Gm}{2\pi C_{GS}}\right)$$

5. FEEDBACK BIASED CASCADED CS AMPLIFIER

In Figure (9), we show the schematic of a voltage amplifier that has been implemented in a 90nm CMOS technology. To achieve sufficient gain, two stages were required due to the relatively low intrinsic gain in 90nm. The amplifier employs feedback-biasing to allow for the use of small transistor area and, hence large mismatch. This requires each stage to have different bias points. Therefore a decoupling capacitor is added between the two stages. This techniques result in a very small input capacitance [5].

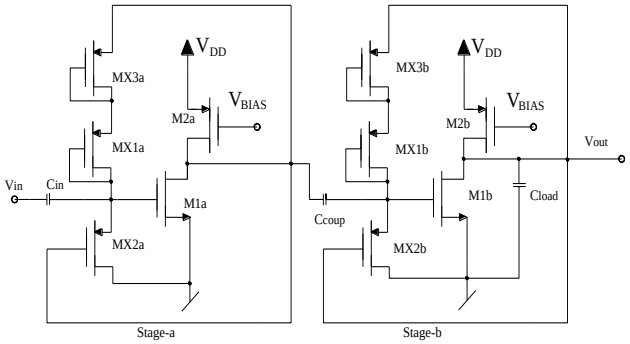

Fig.13 Schematic of a feedback biased Cascaded CS amplifier

Diode-connected devices MX1 and MX3, which are connected in series across input device M1, form the feedback biasing resistance. Using two devices in series ensures that the voltage across them is not sufficient to turn

them both "on" during large voltage swings. Hence, a high-resistance path is guaranteed at all voltage levels.

Device MX2 is optional in the design for the feedback biasing to work. It typically exhibits a much higher resistance, compared to the feedback-resistive path (series combination of MX1 and MX3), and forms a direct high-resistance path to ground for the gate node of M1. It also acts as a voltage dependent resistance that forms a weak feedback loop that keeps M1 from entering deep into the linear region during higher-than-rated input voltages. It was also observed that MX2 helped improve the linearity performance of the amplifier by compensating for the nonlinear behavior of the main feedback path. Under normal operation of the amplifier, the input resistance (at the gate of M1) is dominated by the equivalent resistance decided by devices MX1 and MX3 [1].

6. SIMULATION RESULTS AND TRANSFER FUNCTION PLOTS USING PSPICE & MATLAB

There is a simulation result of transfer function given in equ.no. (11) and their relevant codes are given in Appendix-I.

.AC Analysis (Gain vs Frequency plot)

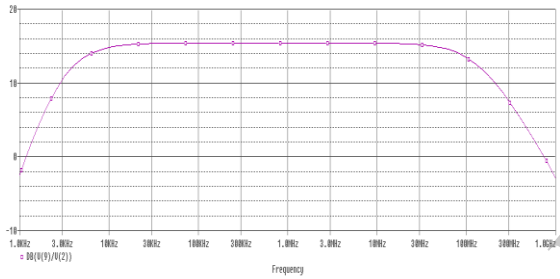

Fig.14 Simulated gain plots for the amplifier using PSPICE.

Gain = 15.417DB

Bandwidth = 132.56MHz.

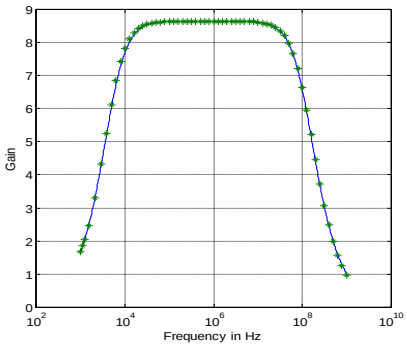

Fig.15 PSpice Simulation and MATLAB transfer function plots for the amplifiers.

Green Dots: PSPICE simulation result

Blue Line: MATLAB transfer function plot result

Figure (15) shows the comparison and agreement between PSPICE simulations results and MATLAB plot of the respective transfer function.

7. CONCLUSION

This paper described about the complete analysis and design of common source amplifier which is used in medical ultrasound imaging system. It gives the derivations of all the equations like, closed loop gain of negative feedback amplifier, transfer function, stability factor, FOM etc. The presented the simulation result of the CS amplifier with feedback biasing in 180nm CMOS technology using PSPICE and compared this with the MATLAB plot of the transfer function of the same.

8. REFERENCES

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