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Implementation of CMOS Full Adder with Less Number of Transistors for Full Swing Output

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***Abstract*- Full adder is a basic building block for various arithmetic circuits such as multipliers, compressors, comparators and so on. Hybrid-CMOS design style gives more freedom to the designer to select different modules in a circuit depending upon the application. In this the Full adder is designed with 180nm technology. Here the full adder is designed with minimum number of transistors. Thus the design is helpful for area efficient and low power consumption which is well suitable for VLSI applications. The full adder design is implemented using LT spice tool and the simulation results are shown in Xilinx tool and spice tool.**

Keywords-hybrid CMOS, X-NOR , Low power

I.INTRODUCTION

With exponential growth of portable electronic devices like laptops, multimedia and cellular device, research efforts in the field of low power VLSI (very large scale integration) systems have increased many folds. Now a day's low power consumption along with minimum delay and area requirements is one of important design consideration for IC designers. There are three major source of power consumption in CMOS VLSI circuits:1) switching power due to charging and discharging of capacitances 2)short circuit power due to current flow from power supply to ground with simultaneous functioning of p-network and n-networks 3)static power due to leakage currents.

Hybrid CMOS logic styles have a higher degree of design freedom to target a desired performance. Hybrid full adder cell has higher speed, less power consumption and higher performance. Full adders are fundamental cell in various circuits which is used for performing arithmetic operations such as addition, subtraction, multiplication, address calculation and MAC etc. Enhancing the performance of the full adders can significantly affect the whole system performance.

The remainder of the paper is organised as follows. Section II gives a brief survey of previous work in which logic styles are compared. Section III consists of the explanation of proposed work.
Section IV includes the simulation results and section V gives a conclusion.

II PREVIOUS WORK

Several logic styles have been used in the past to design full adder cells. Each design styles have its own merits and demerits. The full adder can be described as follows: Given the three 1-bit inputs A,B and C, it is desired to calculate the two 1-bit outputs SUM and Cout, where

$$SUM = A \oplus B \oplus Cin$$
$$Cout = Cin\ (A \oplus B) + AB$$

These outputs can be expressed in many different logic expressions. Therefore, many full adder circuits can be designed using the different expressions. There are three main components to design a full adder cell [12]. Those are XOR or XNOR, Carry generator and SUM Generator. In [7] different components have been combined to make 41 new 10- transistor full adders. Each full adder that uses more than one logic style is called hybrid full adder [12].

There is a variety of full adders in the literature for example there are 41 full adders only in [7]. Many of them use XOR and XNOR as intermediate signals [13]. There are full adders based on only multiplexers or inverters.

The conventional CMOS [14] adder cell using 28 transistors based on standard CMOS topology is shown in fig.1. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. However, using inverters on the output nodes decreases the rise-time and fall-time and increases the driving ability. It functions well at low power supply voltages because it does not have threshold loss problem.

III PROPOSED WORK

In this design style full adder structure is designed by breaking the full adder into three modules. Module 1 is an XOR-XNOR circuit which drives the other modules, so it must have good driving capability and provides full swing outputs simultaneously.

Module II and module III are the sum and carry circuits which use the output of first module and third input signal as input to produce the sum and carry outputs respectively. General structure of hybrid CMOS design style is shown in fig 1

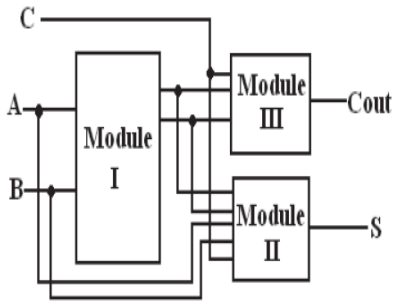

Fig 1: Hybrid CMOS Structure.

(A)MODULE I

Module I circuit is an XOR-XNOR circuit. Circuit shown in fig 2 use only 6 transistors and provide full output swing. This circuit requires low power and provides low delay and due to the feedback transistors at the output connected with supply voltage and ground provide good driving capability. But some combinations of inputs such as "00" and "11" it provides little bit higher delay.

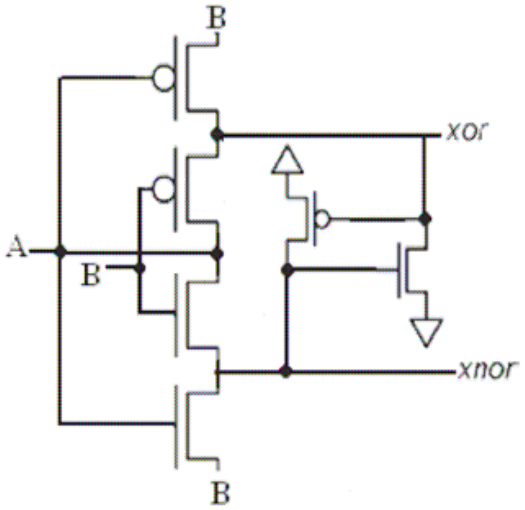

Fig 2 : XOR-XNOR Circuit

(B)MODULE II CIRCUIT

For an XOR gate when input h will be at logic '0' by then output will follow the other input, it can be implemented by using one NMOS to pass logic '0' by connecting the gate terminal with H', source terminal with Cin and drain terminal at the output, and one PMOS to pass the logic '1' by connecting the source terminal with Cin, gate terminal with H and drain with the output. When H will be at logic '0' H' will be at logic 1, both transistors will be on and output will be connected to Cin, so when Cin will be at logic '1' output will be connected to logic '1' and when it will be at logic '0' and when it will be at logic '0' output will also be connected to logic '0'. Both the transistors will be in off state for H to be at logic '1'.

When the inputs H and Cin will be at logic '1', then the output is low, it is implemented by connecting two NMOS in series with their gate terminals connected to H and Cin, source terminal of one of the NMOS is connected to the grounded and the source terminal of other is connected to the output .

Similarly, when H is at logic '1' and Cin is at logic '0', the output is at logic 1 so we use two PMOS in series with source terminal of one of the PMOS at logic high, drain terminal of other PMOS at output and the gate terminals are connected with H and Cin respectively. When both inputs will be at logic '1' then output will be connected to ground and the output will be at logic '0', when H will be at logic '1' and Cin will be at logic '0' both inputs H' and Cin will be at logic '0' and both transistor will be on and output will be connected to power supply and we get logic '1' at the output.

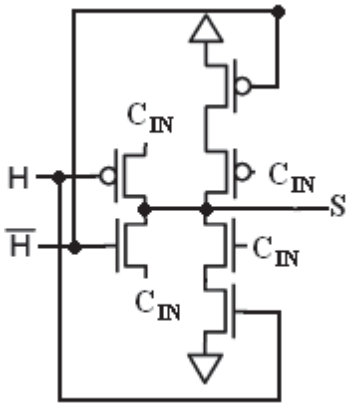

Fig 3:Module II Circuit

(C)MODULE III CIRCUIT

Module III circuit is a multiplexer which select Cin if H is at logic '1' else selects A or B as the ouput Cout. We use transmission gate with H and H' at the gate terminal of NMOS and PMOS respectively to pass the Cin to Cout for H at logic high or when other inputs A and B are at different logic level. When the H is at logic '0' or both inputs A and B are at same logic level we have to pass any of these inputs to the output. So we use one PMOS and one NMOS to pass input A by one transistor and other input B by another transistor. By the use of these two inputs from two sides it improves the performance of the circuit.

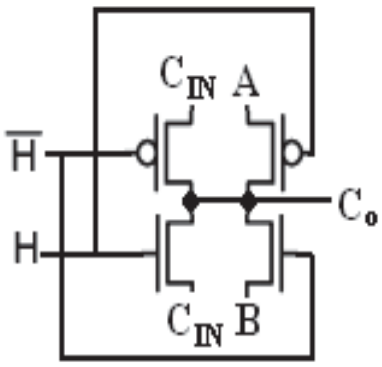

Fig 4: Module III Circuit

(D) CMOS FULL ADDER

By using the three modules mentioned above full adder is designed to get the sum and carry outputs.

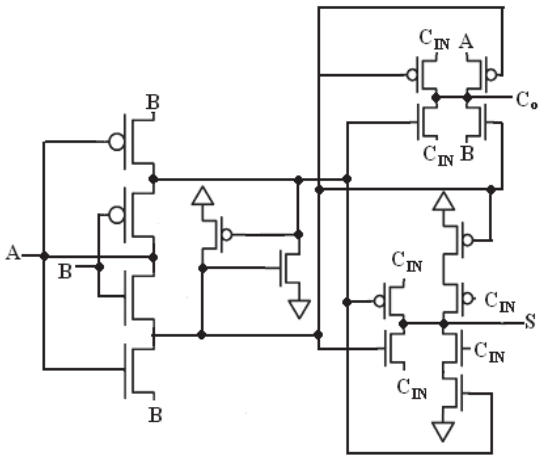

Fig 5: Hybrid CMOS Full Adder

III SIMULATION RESULTS

The full adder is implemented by using LT spice tool using 180 nm technology and compared with the 130 nm technology. Here the power consumption has been reduced for 130 nm technology. The results are shown below.

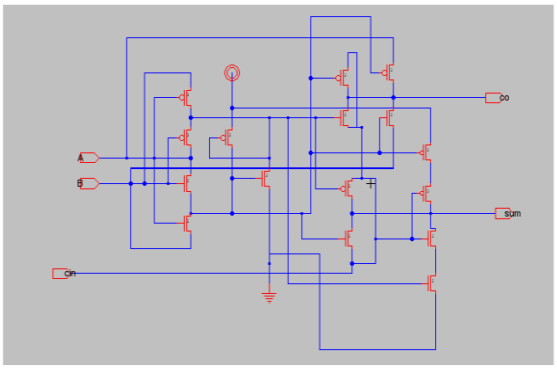

Fig 6: Schematic of Full Adder

(E) LAYOUT OF FULL ADDER

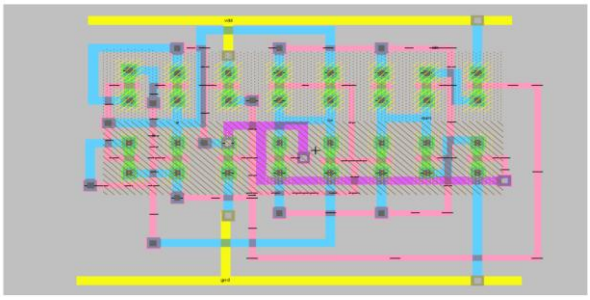

Fig 7: Layout Of Full Adder

(F) SIMULATION RESULTS OF FULL ADDER

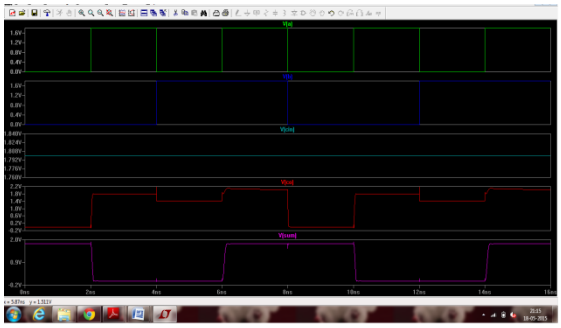

Fig 8 : Simulation Results Of Full Adder

(G) LAYOUT OF CARRY SELECT ADDER

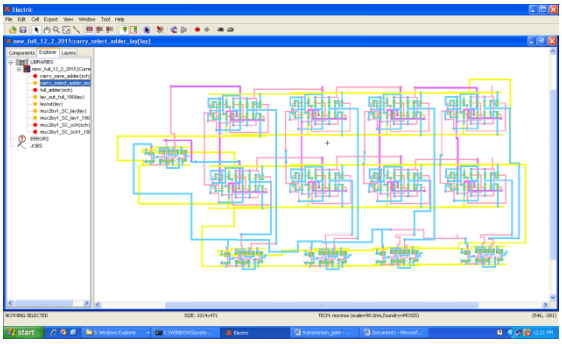

Fig 9:Full adder based carry select adder layout

V CONCLUSION

Hybrid-CMOS design style gives more freedom to the designer to select different modules in a circuit depending upon the application. Using the adder categorization and hybrid-CMOS design style, many full adders can be designed. The proposed hybrid-CMOS full adder has better performance than most of the standard full-adder cells owing to the novels design modules proposed. This is implemented on 180nm technology using LT spice tool and power consumption has been calculated. Full adder based carry select adder is also implemented.

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