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Implementation Of High Seed Router For High Altitude Platforms

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Abstract

In this paper we propose to Implement High Speed Router (HSR) for High Altitude Platform (HAP), provides high speed communication in surrounded places from satellite to terrestrial and from terrestrial to satellite. People want a communication "without wires". At earlier radios can provided wireless communication, But in the terrestrial environment, radio signals are scattering and multipath effects that limit the quantity of communication. In Cellular systems, radio coverage is deliberately restricted to allow for frequency reuse. As a consequence, terrestrial wireless networks comprise numerous antenna towers, base stations (BS) and mobile switching centres, all dispersed over wide geographical areas. Satellites can provide best wireless coverage with less terrestrial Infrastructure. When a data is travels from one place to another at that time it is in terms of stream of bytes. Whole data is divided into packets as per the size of data frame. Router provides route facility for data transfer. Packets are transfer one by one from source to destination as per their sequence number. Speed factor matters for data transfer. Low Speed Router provides 1Mbps-5Mbps data transfer rate for HAP while High Speed Router provides 10Mbps-15Mbps data transfer rate for HAP. High Altitude Platform provides a wireless communication facility from satellite to terrestrial and vice versa at the altitude of 17~22km above the earth surface.

Keywords: High Speed Router (HSR), High Altitude Platforms (HAPs), IP Stack, Wireless communications, Protocols for wireless communications, Cyclone III EP3C25F324C6N kit.

1. Introduction

HAP has advantages of both terrestrial as well as satellite. Here for implementing high speed router we used concept of IP Stack. Fig-1 shows Block diagram of HSR. It includes different modules. Each Module having its own functionality, every module depends on each other. Programming of HSR developed in VHDL (Very High Speed Hardware Development Language) language using concepts of FPGA (Field Programming Array).

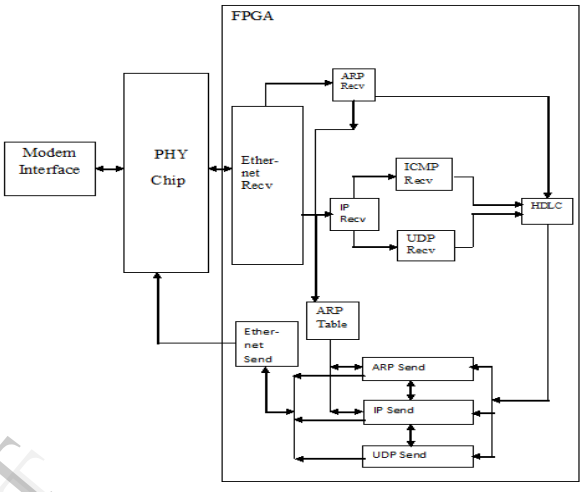

Figure 1. Block diagram of high speed router

As shown in Figure 1. first of all data travels form modem interface to PHY chip and then it interact with FPGA. Here we included main two different modules – sender side as well as receiver side. Each module having its own sender and receiver sides, interact to each other when needed. HDLC (High Level Data Link Control) gathered all data and transfer it to a sender side. All modules of HSR programmed in VHDL. Here we taken output on the cyclone III board as well as transfer our data from one PC to another PC (Figure 2).

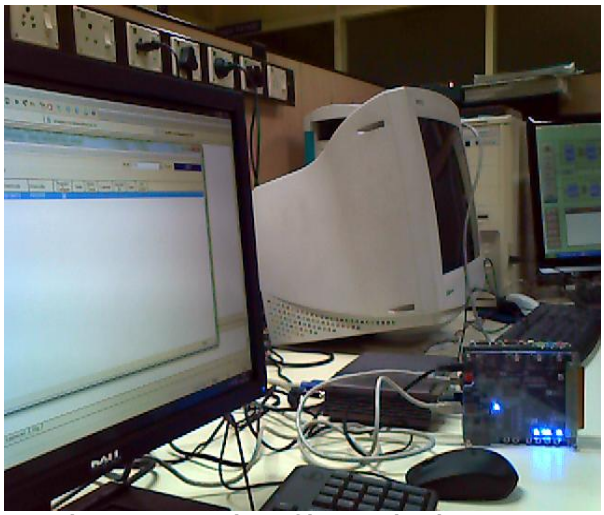

Figure 2. Snapshot of interaction between PC to Board to another PC

2. Modules of HSR

In HSR when data reached at Ethernet receiver side it's in form of 4 nibble byte streams. At Ethernet receiver level First it checks a data header have either 0(zero) or 1bit. If the data header is set to 0 than data moves to ARP receive module else it goes with IP(Internet Protocol) receive module. The Ethernet receiver is connected to the PHY via an MII, with a 4 bit (nibble) wide data bus (rxdata), a receive data valid signal (rx_dv), a receive error signal (rx_er) and a receive clock (rx_clk). When the PHY receives a frame, rx_dv is asserted for the entirety of the frame. Figure 3. shows simulation results of Ethernet Receiver.

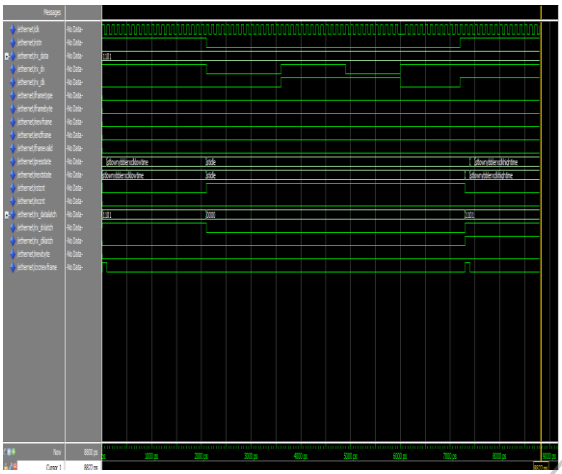

Figure 3. Simulation of Ethernet Receiver

The Ethernet sender is connected to the PHY via a similar interface as the Ethernet receiver. From the PHY to the Ethernet sender there is the transmit clock (tx_clk) which is the clock used to synchronise the data between the two devices. The Ethernet sender can transmit either ARP or IP frames, as specified by the frame type input. Figure 4. shows simulation results of Ethernet sender.[3]

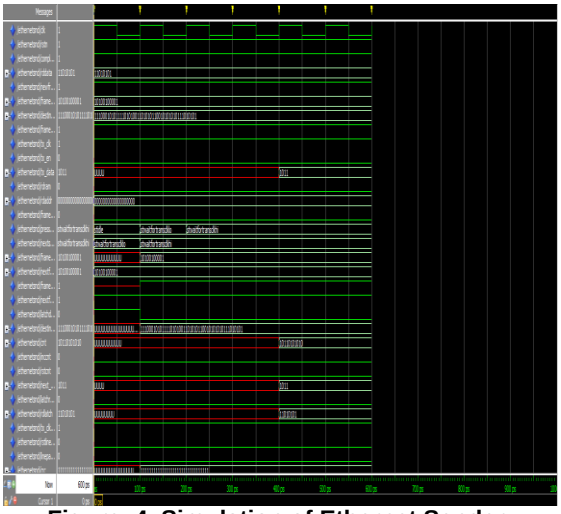

Figure 4. Simulation of Ethernet Sender

At ARP Receive module first it checks entry in ARP Table.ARP table contains two fields: IP address and MAC address. If DHCP Server is installed in your computer than it automatically provides IP address to connected computers. Else its checks either IP address or MAC address of current request. If this request come for first time than it makes entry in the ARP table and send it to the ARP sender, else it updates its entry, already stored into ARP table than send it to ARP sender to Ethernet receiver to PHY chip to modem interface.ARP receiver includes all fields as a input from their standard ARP Frame Format. The ARP layer handles ARP replies and ARP requests and manages the ARP table and receives ARP table lookups. It informs ARP Sender to generate ARP replies when needed. When an Ethernet frame is received with an Ethernet type field of 0806h, then the ARP receives an ARP frame from the Ethernet Receiver via a byte stream. It also uses a concept of two way handshaking. Figure 5. shows Simulation of ARP receiver.[3]

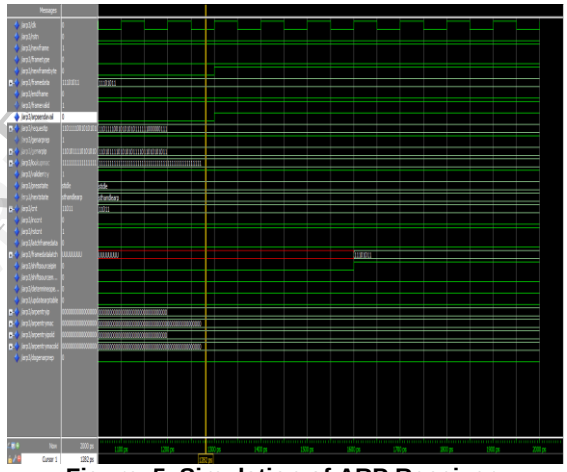

Figure 5. Simulation of ARP Receiver

The ARP sender is intermediate between the Ethernet Send and the Internet Send layers and constructs ARP requests and replies; handles ARP table lookups; and passes frames from the Internet Send layer to the Ethernet Send layer. The ARP Sender will always be unavailable while the Ethernet Sender is sending a frame. Figure 6. shows simulation of ARP sender.

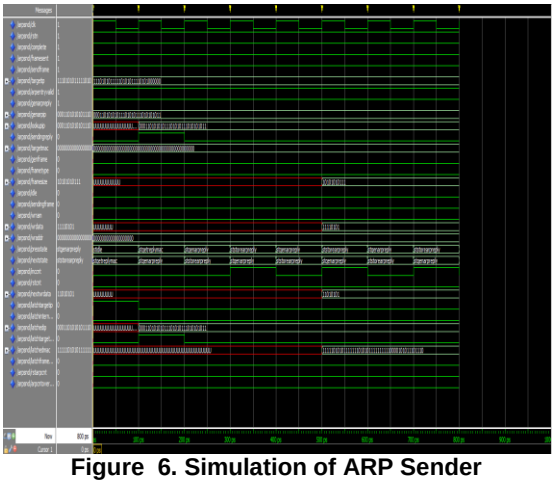

Figure 6. Simulation of ARP Sender

The Internet layer receives datagram from the Ethernet Receiver. If no more fragments are coming, then passes the datagram to the required protocol on the above transport layer. Each datagram is received from the Ethernet Receiver via a byte stream. When header bit of a data frame is set to 1 at that time data transfer to IP receiver again it checks inner header of frame whether its 0 or 1 if its set to 0 means there is an error or some packet missing from frame so it send it to ICMP (Internet Control Message Protocol) module. The Internet Sender handles the creation of IP datagram and the fragmentation of the Frame if they are too large. Once it forms the correct header and creates the datagram, it passes the nearly formed IP datagram down to the ARP Sender if it is available. Figure 7. shows simulation results of IP module.

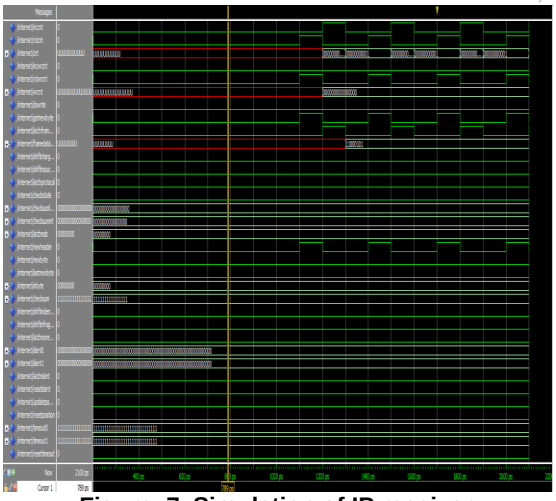

Figure 7. Simulation of IP receiver

In ICMP module is worked at network layer of OSI layer. ICMP messages are divided into error-reporting messages and query messages. The error-reporting messages report problems that a router or a host (destination) may encounter. The query messages get specific information from a router or another host. A query message includes Destination Unreachable, Source Quench, Time Exceeded, Redirection etc. ICMP reports error message to the original source. ICMP can also diagnose some network problems through the query messages, a group of 4 different pairs of messages. In this type of ICMP message, a node sends a message that is answered in a specific format by the destination node. It includes Echo Request and Reply, Timestamp Request and Reply, Address-Mask Request and Reply, Router Solicitation and Advertisement. In our project ICMP is intermediate module between UDP and IP modules (UDO-ICMP-IP).than data is transfer to HDLC (High Speed Data Link Control) Figure 5. Shows simulation results of ICMP. Figure 8. Shows simulation of ICMP.[3]

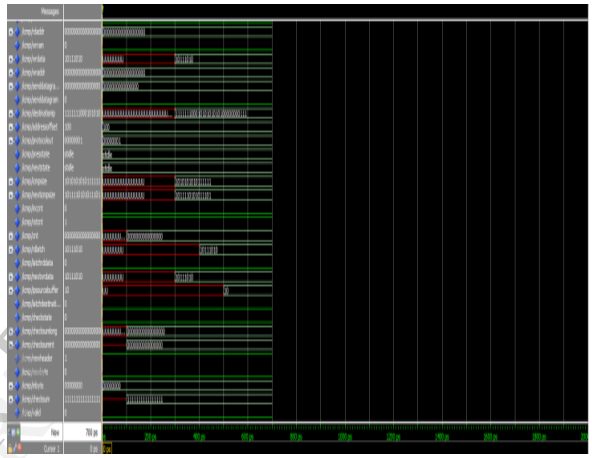

Figure 8. Simulation of ICMP

UDP catches UDP messages on a specified port and stores them in RAM. Once an IP datagram arrives with the protocol field set to UDP. Here checksum is ignored. Figure 9. shows simulation results of UDP.

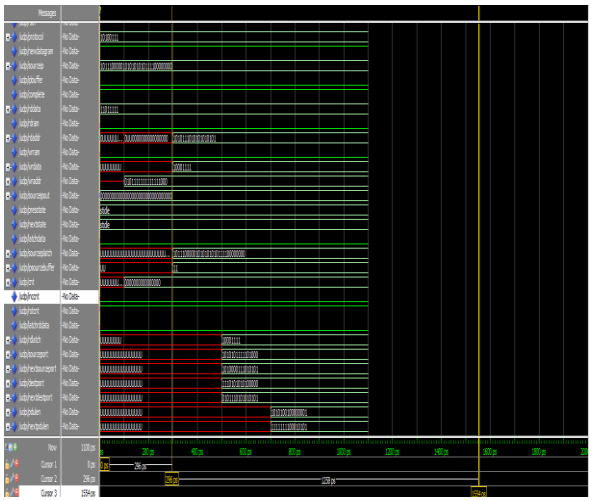

Figure 9. Simulation of UDP receiver

3. Interfaces of High Speed Router

Interface modules of HSR are as follows:

Memory multiplexor: Allows either the PC to access RAM (Figure 10).

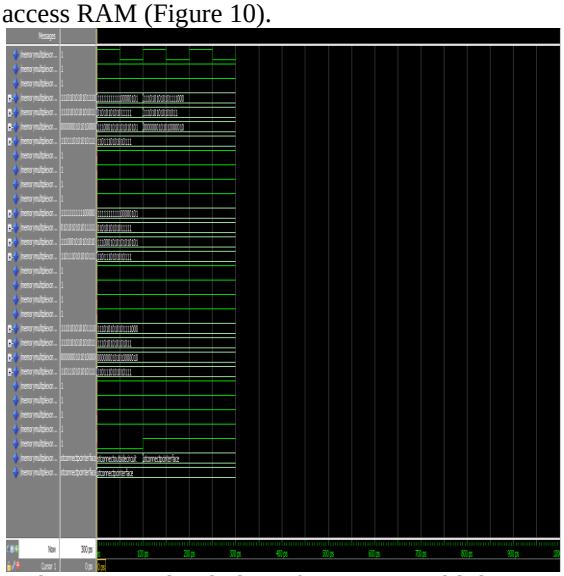

Figure 10. Simulation of Memory Multiplexor

Pc_to_sraminterface: Handles the protocol for the communication between the PC and the cycloneIII kit (Figure 11.)

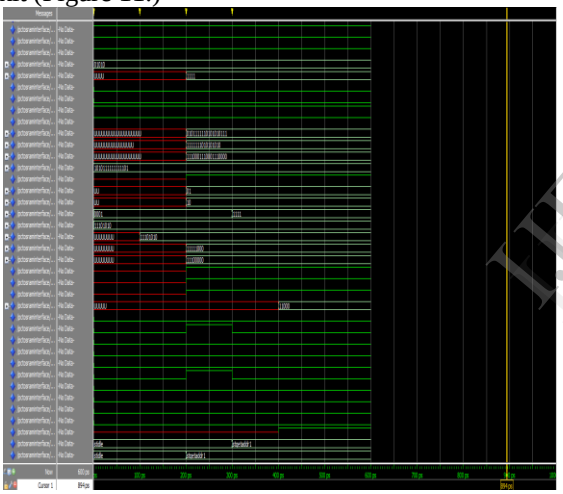

Figure 11. Simulation of PC-to-SRAM interface

Stack: Top level for the design, also contains a RAM and to share RAM usage between the different layers (Figure 12.)[3]

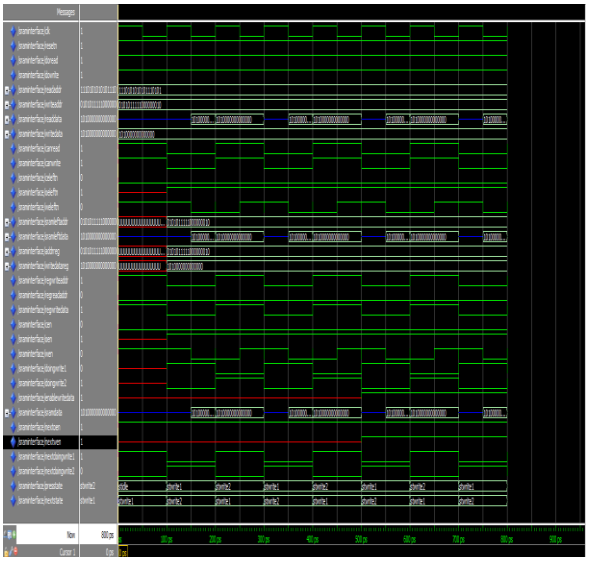

Figure 12. Simulation of RAM and other layers

Table 1. Performance details of high speed router

Specification	Parameters
Power	0.042w
Worst Case Delay	8.266ns
Number of LUTs used	1897(1713 as logic Gates remain as I/Os)
Number of Registers used	1517(all Filp Flops)

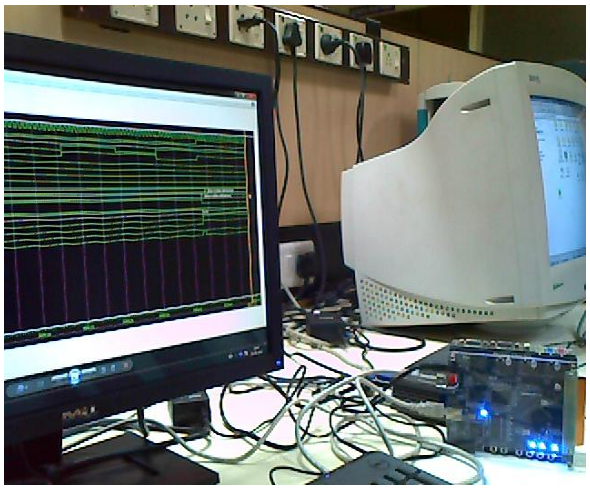

Figure 13. Snapshot of simulation result while data transfer

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