

# Implementation of Soft Decision Viterbi Decoder Based on a Digital Signal Processor

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**Abstract**—This paper describes the implementation of soft decision Viterbi channel decoding algorithm using a digital signal processor. This was done through a computer simulation and also through using a dsp56f807evm digital signal processor (DSP). The dsp56f807evm DSP can achieve the performance of up to 40 million instructions per second (MIPS) at 80MHz core frequency and consequently has gained more and more popularity in many applications. Moreover, the implemented Viterbi decoder was tested against an additive white Gaussian noise channel (AWGN) at different signal to noise ratios ( $S/N$ ) and different convolutional code constraint lengths.

**Keywords**—Convolutional Encoder, Viterbi Algorithm, Viterbi Convolutional Decoding Algorithm

## I. INTRODUCTION

The convolutional coding first introduced by Elias in 1955 [5]. Convolutional coding and Viterbi decoding are powerful forward error correction (FEC) techniques for additive white Gaussian noise (AWGN) channels. It is operating on data streams and has memory that uses previous bits to encode, and has good performance with low implementation cost [1]. Convolutional coding has been used in communication systems including deep space communications and wireless communications to improve the bit error rate (BER) performance. The Viterbi decoding algorithm (VA) proposed in 1967 by Andrew Viterbi was a decoding process for convolutional codes [5]. It is used for decoding a bit stream that has been encoded using FEC code. The convolutional encoder adds idleness to a continuous stream of input data by using a linear shift register. The Convolutional Encoder and Viterbi Decoder used in the Digital Communications System is shown in "Fig.1," [1].

In this paper, we concern with designing and implementing a convolutional encoder and soft decision Viterbi decoder which are the essential blocks in digital communication systems using DSP hardware kits.

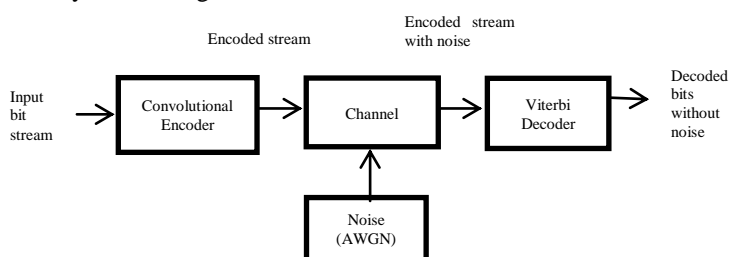


Fig.1. Convolutional encoder and Viterbi decoder [1]

## II. CONVOLUTIONAL ENCODER

Convolutional coding is a channel coding method [2]. A general convolutional encoder is shown in "Fig.2," the encoder has a  $kK$ -stage shift register and  $n$  module-2 adders with constraint length  $K$ . The constraint length  $K$  is the number of  $k$ -bit shifts over

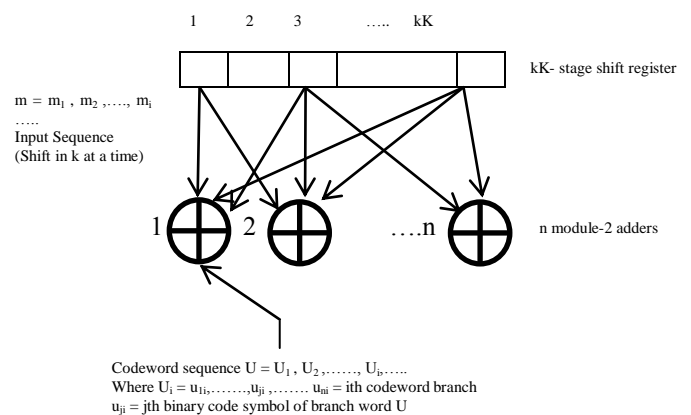
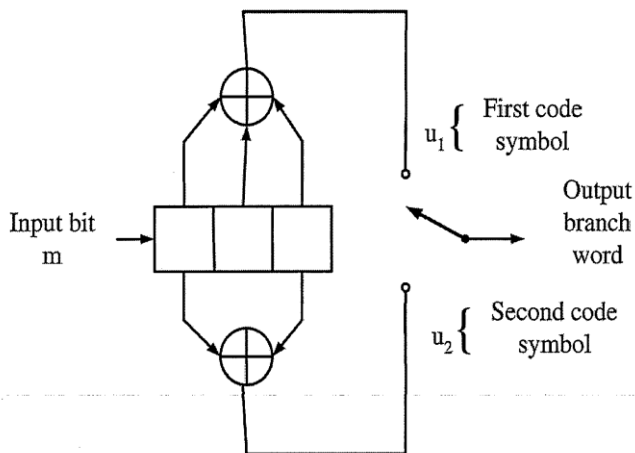


Fig.2. convolutional encoder (rate =  $k/n$ , length  $K$ ) [2]

which a single message bit can affect the encoder output. The encoder is working in the following way. At every time unit,  $k$  bits of data are serially input into the left  $k$  stages of the shift register, while all bits in the register are shifted  $k$  stages to the right. After that, the outputs of  $n$  adders are sampled one after another to generate the coded symbols. These coded symbols are then used by the modulator to generate the signals to be transmitted over the channel. Since at each input unit time, there are  $n$  bits in the encoded signal for  $k$  bits in the input message signal, the code rate is  $k/n$  message bits per code bit, where  $k < n$ . Although  $k$  could be any positive integer, it is generally specified as  $k=1$  in most applications, that is, the input message bits are shifted just one bit at a time into the encoder shift register [2].

To explain the convolutional encoder, an example is shown in "Fig.3," [2]. It is a  $k=1$  and  $n=2$  convolutional encoder with constraint length  $K=3$ .

Fig.3.Convolutional Encoder (rate =  $\frac{1}{2}$ , length  $K = 3$ ) [2]

### III. The Viterbi Algorithm for Decoding of Convolutional Codes

There are different decoding methods for convolutional codes which are threshold decoding, sequential decoding and maximum likelihood decoding.

1. *Threshold decoding*: It is called majority logic decoding. It is the simplest of them, but it successfully applied only to the specific classes of convolutional code. It is applying to channel that having mid to good SNR. Moreover, it is also far away from optimal because of its inferior bit error performance [3].

2. *Sequential decoding*: It was a sub-optimal algorithm. It has better performance than the previous method. The advantage of sequential decoding is its usage for decoding long constraint-length convolutional codes. The disadvantage of sequential decoding was variable decoding time and required large memory [3].

3. *Viterbi decoding*: It is an optimal (in a maximum likelihood sense) algorithm for decoding of convolutional code. It is dominant technique for convolutional codes. The advantage of Viterbi decoder is to satisfy bit error performance, low cost, fixed decoding time [3]. But its computational necessities grow exponentially as a function of the constraint length, so it is generally limited in practice to constraint lengths of  $K = 9$  or less [1]. Its main drawback is that the decoding complexity grows exponentially with the code length. So, it is used for short codes.

#### A. The Viterbi Convolutional Decoding Algorithm

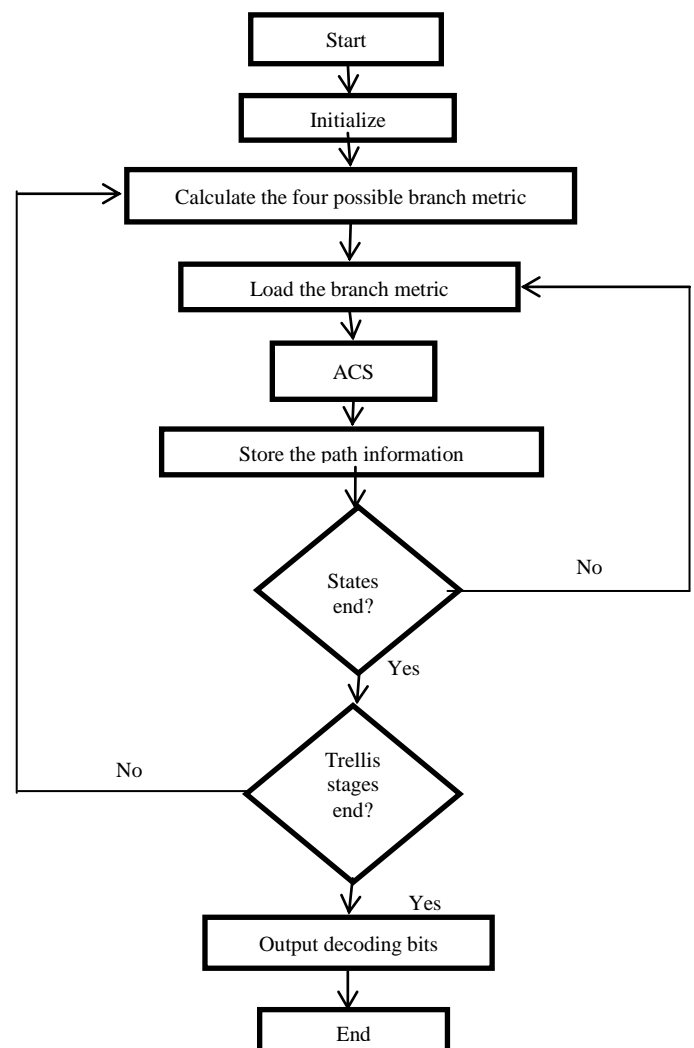
The Viterbi algorithm (VA) was proposed by Viterbi in 1967 as a technique of decoding convolutional codes. Later, Omura showed that the Viterbi algorithm was equivalent to finding the shortest path through a weighted graph. Forney recognized that it was a maximum likelihood decoding algorithm for convolutional codes because the decoder output selected was the code word that gives the largest value of the log-likelihood function [4].

Basically, the VA is the maximum likelihood decoding method. In other words, it finds the most likely transition sequence in a state diagram from a given set of input codes [2]. The encoder adds redundant information to the original information  $i$ , and the output  $t$  is transmitted through a channel. Input at receiver end ( $r$ ) is the information with redundancy and possibly, noise. The receiver tries to extract the original information through a decoding algorithm and generates an estimate ( $z$ ) of the transmitted code word. A decoding algorithm that maximizes the probability  $p(r|z)$  is a maximum likelihood (ML) algorithm. An algorithm which maximizes the  $p(z|r)$  through the proper selection of the estimate ( $z$ ) is called a maximum a posteriori (MAP) algorithm. The two algorithms have identical results when the source information  $i$  has a uniform distribution. If the distribution of the source bits  $x$  is uniform, the two decoders are identical [5].

By Bayes' law, we can get [5]

$$p(r|z) p(z) = p(z|r) p(r)$$

#### B. Flow Chart of Decoder of Viterbi Algorithm [5]:



IV. 56f807evm 16-Bit Hybrid Processor Hardware

A. Architecture Overview

- Up to 40million instructions per second(MIPS) at 80MHz core frequency
- DSP and MCU functionality in a unified,C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports bothDSP and controller functions: MAC, bitmanipulation unit, 14 addressing modes
- 60K ×16-bit words Program Flash
- 2K ×16-bit words Program RAM
- 8K ×16-bit words Data Flash
- 4K ×16-bit words Data RAM
- 2K ×16-bit words Boot Flash
- Up to 64K ×16- bit words each of externalProgram and Data memory
- Two 6 channel PWM Modules
- Four 4 channel, 12-bit ADCs
- Two Quadrature Decoders
- CAN 2.0 B Module
- Two Serial Communication Interfaces (SCIs)
- Serial Peripheral Interface (SPI)
- Up to four General Purpose Quad Timers
- JTAG/OnCETM port for debugging
- 14 Dedicated and 18 Shared GPIO lines
- 160-pin LQFP or 160 MAPBGA Packages

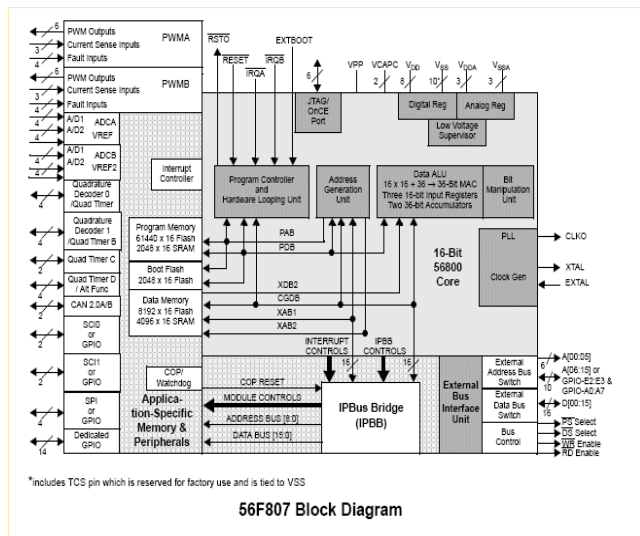


Fig.6.56F807 Block Diagram

B. Overview of the Simulation

The model shown in “Fig.7,” is written in C- language code and simulated using MATLAB. The simulation ends after processing 100 bit errors or 10<sup>6</sup> message bits, whichever comes first.

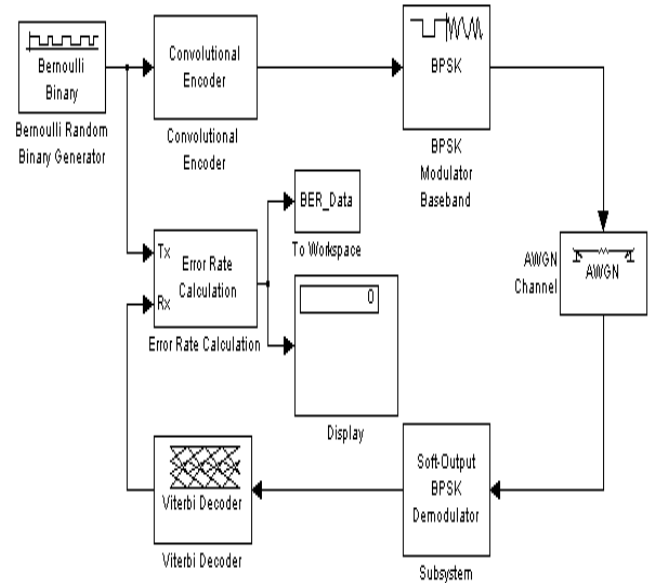


Fig.7. Block Diagram of Soft-Decision Viterbi Decoding

C. Results

The behavior simulation system was looped until 100 data bit errors were detected or 1000000 data bits were transmitted. Simulations were run with an Es/No from 0 dB to 3 dB with step .5 dB. The simulation and implementation of convolutional encoder and soft decision Viterbi decoder is tested against AWGN channel using different signal to noise ratios(S / N) and different generator polynomials(different constraint length). The processor implementation results for rate 1/2 convolutional encoder and Viterbi decoder with different generator polynomials

1) Results from Simulations: This section covers results/simulations done using ‘C’ code and plots the results on matlab. Analysis of performance of the codes is done in terms of BER and Eb/No .This figure covers the BER plots of simulation results for rate 1/2 convolutional coding with soft-decision Viterbi decoding on an AWGN channel with various convolutional code constraint lengths

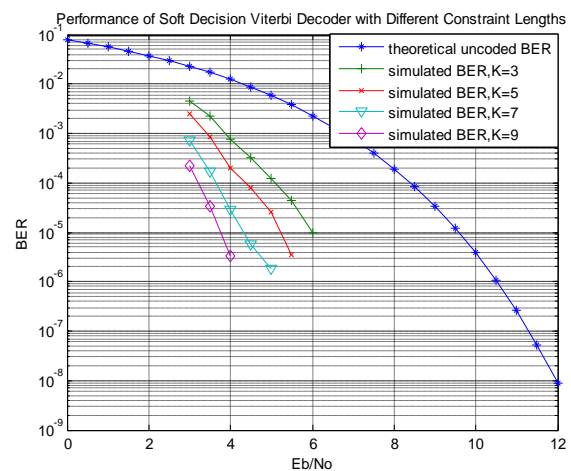


Fig.8. Simulation Results for Rate 1/2 and different constraint length

The results obtained is shown in “Fig.8,” using the simulation code, with the trellis depth set to  $5 \times K$ , using the adaptive quantizer with three-bit channel symbol quantization. For each data point, the simulation ran until 100 errors (or possibly more) occurred. With this number of errors, the confidence index was 95%. This means that the true number of errors for the number of data bits through the simulation lies between 80 and 120.

2) *Results from Implementation:* This section covers results/simulations done on 'code warrior IDE' and implemented on dsp56F807evm-Digital Signal Processing kit and plots the results on matlab. The implementation done until 100 data bit errors were detected or 128 data bits were transmitted.

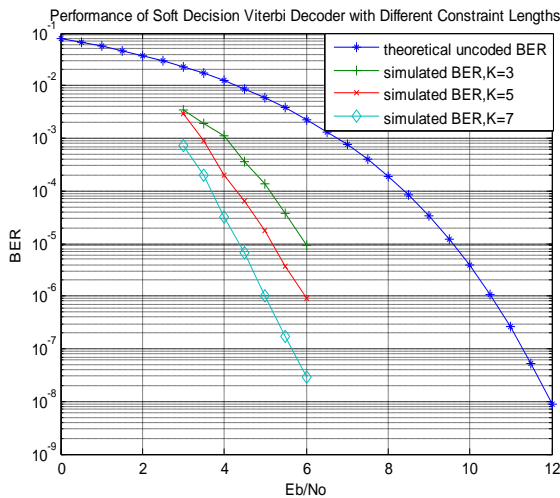


Fig.9. Implementation Results for Rate 1/2 and different constraint length

The simulation and implementation results are matched with the theoretical results.

3) Theoretical Results from Matlab:

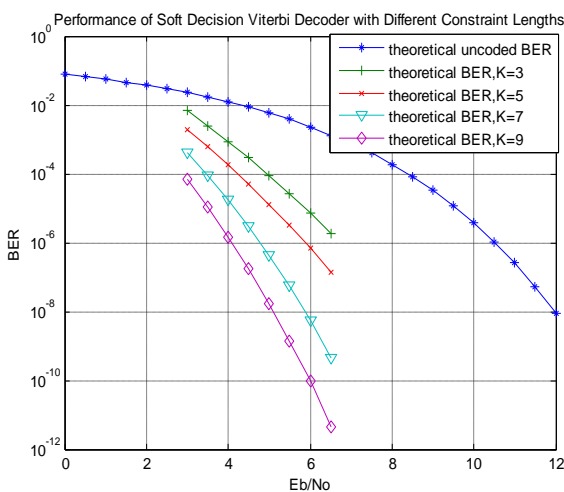


Fig.10. theoretical results with a 1/2 rate and different constraint length

V. COMPARISON BETWEEN SIMULATION AND THEORETICAL RESULTS:

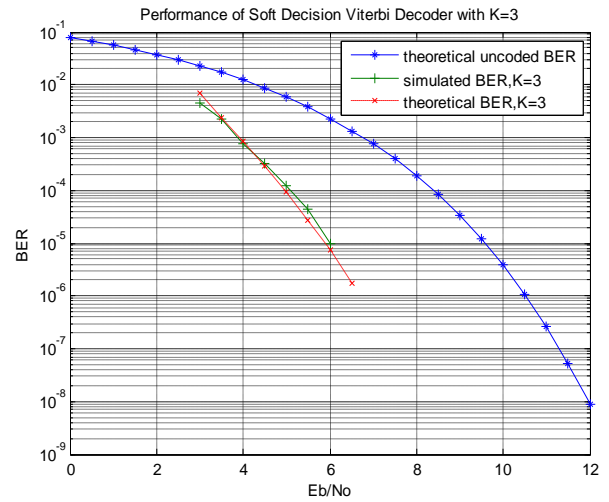


Fig.11. comparison between simulation results and theoretical results with a 1/2 rate and K=3

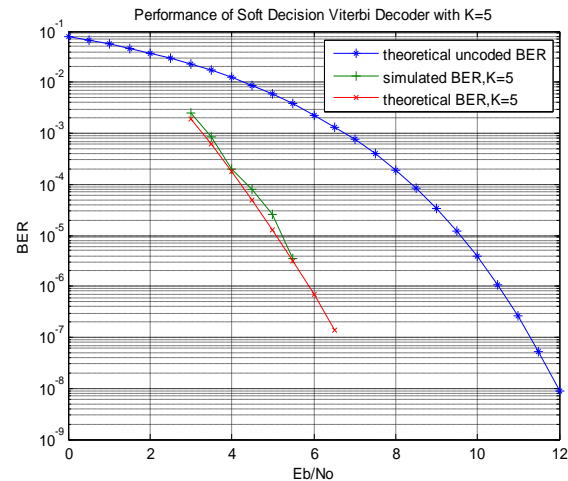


Fig.12. comparison between simulation results and theoretical results with a 1/2 rate and K=5

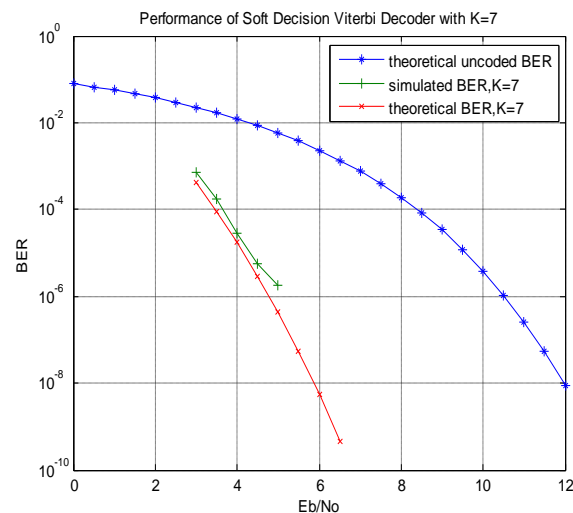


Fig.13. comparison between simulation results and theoretical results with a 1/2 rate and K=7

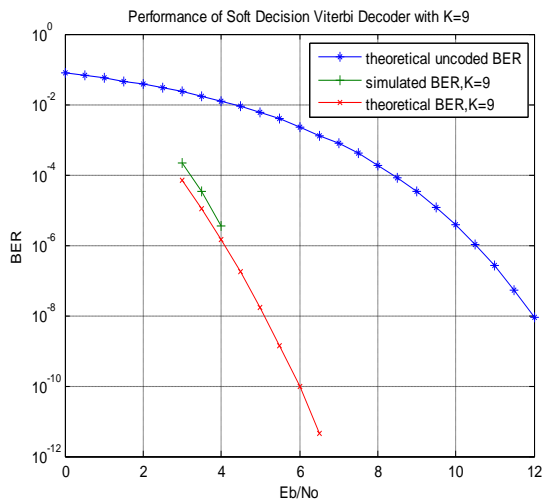


Fig.14. comparison between simulation results and theoretical results with a 1/2 rate and K=9

From the above figures, the simulation and theoretical results approximately with the same values at different constraint lengths.

## VI. CONCLUSION

Convolutional Encoder and soft decision Viterbi decoder for the rate  $\frac{1}{2}$  is simulated and implemented for different constraint lengths for different constraint lengths and for AWGN channel using different signal to noise ratios (S / N). Moreover, the Viterbi decoding algorithm is mature error correct system, which will give us a BER at 2.9E-008 at 6db on an AWGN channel with BPSK modulation and K=7.

Convolutional encoder with soft decision Viterbi decoder is successfully implemented on DSP56f807evm.

## VII. REFERENCES

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